

ABSTRACT

A test chip comprises: at least one signal processing circuit for generating a test signal for an electrical test of a device under test and processing upon receipt of the response signal from the device under test; and a delivery/receipt circuit for delivering and receiving electrical signals to and from the signal processing circuit and outside. The signal processing circuit includes: a formatter which, on the basis of pattern information supplied from outside, generates pulse signal of truth-values 1 and 0; a plurality of drivers which, on the basis of the pulse signal, generates a drive signal for driving the device under test; and a plurality of comparison circuits which, upon receipt of a response signal from the device under test, outputs a defective signal representing that cells in the device under test are defective. The delivery/receipt circuit includes: a rate generator for generating a reference test frequency signal; a fail capture control which, on the basis of the defective signal, specifies defective cells and outputs outside; a timing generator which, on the basis of the reference test frequency signal, outputs a timing signal corresponding to the reference test frequency signal; and a pattern generator for outputting outside an address signal to read the pattern information from outside

Fig. 16

