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TRANSIENT VOLTAGE CLAMPING CIRCUIT

FIELD OF THE INVENTION

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The present invention relates to a circuit for transient voltage clamping. In particular, the circuit is for transient voltage clamping within an ASIC which is a motor driver for a disk drive.

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BACKGROUND OF THE INVENTION

In typical hard disk drive (HDD) applications, specific integrated circuits (ASICs) are used for driving the spindle and voice coil motors. Under certain conditions, inductive loads may dump their stored energy (in the form of large currents) on the power supply of the ASIC causing the voltage in the power supply to rise. Reverse isolation blocking diodes are usually provided to prevent the system power supply from absorbing the excess energy. As a result, the drain voltage of the high side drivers may rise to levels which cause the destruction of the ASIC. Therefore a voltage clamp is required to be placed on the supply voltage of the ASIC for reducing the effects of such transient voltages from the inductive loads.

In order to address the above mentioned problem, prior art solutions provide the following:

- 25 1. A transient voltage suppressor (TVS) can be used externally to the ASIC to clamp the voltage. This increases the cost of the HDD and the voltage tolerance of the TVS is often wide, which can lead to inadequate suppression of transient voltages. For example, if the required TVS operating range is 13.2V (i.e. 12V supply + 10%) to 16V (the absolute rating) and TVS voltage tolerance is wide, it may not be able to effectively clamp in the
30 required range.

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2. An alternative is to put a very large capacitor on the ASIC power supply to absorb the dumped energy. However, such large capacitors are costly.
3. A simple voltage clamp circuit consisting of zener-npn or zener-nmos devices can also be used to absorb the dumped energy. Such a circuit can be integrated into the ASIC or may be external. However, the wide tolerance of activation voltage and long response time makes this circuit unsuitable for use in applications where the operating voltage range and the absolute maximum voltage of the ASIC are relatively close to each other. HDDs of small dimension require lower tolerances in activation voltage than are provided by these circuits.

SUMMARY OF THE INVENTION

- 15 The present invention provides a transient voltage clamping circuit of an integrated circuit for a disk drive, the circuit comprising:
- a power transistor for sinking a power supply voltage subjected to transient variation;
 - a reference circuit for deriving a first reference voltage from a second reference
 - 20 voltage and said power supply voltage; and
 - an amplifier circuit for receiving said first reference voltage as an input and for driving said power transistor.

- Preferably, the transient voltage clamping circuit further comprises a pull down circuit
- 25 connected to a gate terminal of said power transistor and an output of said amplifier circuit for controlling operation of said power transistor. Preferably, the pull down circuit is adapted to sink the gate voltage at said gate terminal when said power supply voltage is less than a first threshold voltage, thereby turning off said power transistor. Preferably, the first threshold voltage is about 5 volts. Preferably, the pull down circuit is adapted to sink
- 30 the gate voltage at said gate terminal when said second reference voltage is less than a second threshold voltage. Preferably, the second threshold voltage is about 0.7 volts.

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Preferably, the amplifier circuit includes a level shift circuit, a voltage multiplier circuit and a buffer circuit.

- 5 Preferably, the first reference voltage is derived from the second reference voltage via coupled n-MOS and p-MOS current mirror circuits.

Advantageously, embodiments of the transient voltage clamping circuit of the invention provide accurate activation, low cost and low tolerance in activation threshold voltage
10 relative to the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an ASIC and motor driver for a hard disk drive;
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Figure 2 shows a circuit for transient voltage clamping according to an embodiment of the invention;

Figures 3A shows a level shift circuit used in the embodiment of the transient voltage
20 clamping circuit shown in Figure 2;

Figure 3B shows the level shift circuit of Figure 3A in combination with a multiplier circuit used in the embodiment of the transient voltage clamping circuit shown in Figure 2;
and
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Figure 3C shows a buffer circuit used in the embodiment of the transient voltage clamping circuit shown in Figure 2.

30 DETAILED DESCRIPTION OF THE EMBODIMENTS

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Referring to Figure 1, a hard disk drive (not shown) includes a motor 20 which receives power through a power ASIC 10. The motor 20 receives power on lines A, B, C from power ASIC 10, each of those lines having an impedance model which includes inductive and resistive impedances. UA, UB and UC are gate drive signals for upper power DMOS transistors for each line A, B and C. LA, LB and LC are for corresponding lower power DMOS transistors. These DMOS transistors provide current to the motor 20.

Power ASIC 10 receives power from an external 12 volt power supply VP12. Power ASIC 10 includes a voltage clamping circuit 12 for clamping transient voltages which are dumped from the inductive loads in the motor 20 and is powered from the power supply rail of the power ASIC 10. The duty cycle of the dumped current is generally small (typically in the order of 3%) and therefore the location of the clamping circuit on the power ASIC 10 does not pose a power dissipation problem if an appropriate package is used.

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Figure 2 shows the voltage clamping circuit 12 in further detail. A reference voltage V_{ref} feeds into an amplifier circuit 13 which drives a power transistor (M0) for sinking dumped current I_d . The reference voltage, V_{ref} , is determined according to the following equation:

$$20 \quad V_{ref} = [V_{pwr} - R2 \cdot I2] = \left[V_{pwr} - \left(R2 \cdot \frac{V_{bg}}{R1} \right) \right] \quad (1)$$

Current I2 is generated at node V_{ref} through p-MOS and n-MOS current mirrors 17, 18 and is driven by an operational amplifier 16 in combination with MOSFET M1. The operational amplifier 16 is supplied with a band gap reference voltage, V_{bg} .

Resistor R2 and capacitor C are compensation components provided for increased circuit stability.

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Coupled p-MOS and n-MOS current mirrors 17,18 allow V_{ref} to be varied with variations in the band gap reference voltage and the power supply voltage V_{pwr} .

Amplifier circuit 13 includes a level shift circuit (LSH), a multiplier circuit (M) and a
 5 buffer circuit (X1). These circuits are shown in Figures 3A, 3B and 3C, respectively. The level shift circuit is also shown in Figure 3B, in combination with the multiplier circuit. The level shift circuit takes the reference voltage V_{ref} and provides a higher operating voltage (by about $1 \times V_{be} = 0.7V$) to the multiplier circuit.

10 The multiplier circuit receives the level shifted voltage and multiplies this by a factor, M , which is determined as the ratio of the resistances of resistors RB and RA shown in Figure 3B. The multiplier circuit is included here in order to provide M times more V_{gs} to the power transistor. This in turn enables the power transistor to handle greater current (by a factor of M^2) for the same gate, width and length without changing the activation voltage
 15 of the clamping circuit 12. The buffer circuit is provided between the multiplier circuit and the gate terminal of the power transistor so as to form a buffer between the power transistor and pull down circuit 14 on the one hand and the driving circuits (including the multiplier, level shift, current mirrors and op-amp, etc.) on the other hand.

20 The equations for the circuit are as follows:

$$V_{gs} = \left[V_{pwr} - \left(R2 \cdot \frac{V_{bg}}{R1} \right) \right] \cdot M + \left(R3 \cdot \frac{V_{bg}}{R1} \right) \quad (2)$$

25 $V_{gs} = V_{TH} + \sqrt{\frac{I_d}{K}} \quad (3)$

Solving (1) and (2), we have

30 $I_d = K \cdot M^2 \cdot (V_{pwr} - V_{clamp})^2 \quad (4)$

Where:

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$$K = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \left(\frac{W}{L} \right) \cdot \lambda \quad (5)$$

- 5 μ is the channel mobility in power transistor M0;
 C_{ox} is the gate capacitance per unit area of power transistor M0;
 W is the gate width for the power transistor M0;
10 L is the gate length for the power transistor M0;
 λ is the channel length modulation effect; and
15 M is the Multiplication Factor defined by the resistor ratio (R_B/R_A) of the multiplier circuit;

V_{clamp} is defined as:

$$V_{clamp} = V_{bg} \cdot \frac{R_2}{R_1} + \frac{\left[V_{TH} + \left(R_3 \cdot \frac{V_{bg}}{R_1} \right) \right]}{M} \quad (6)$$

- 25 V_{TH} is the DMOS Threshold voltage; and
 R_3 is resistor R_B in the multiplier circuit.
30 The most important of the formulae shown above is the formula for determining V_{clamp} , which defines the threshold voltage of V_{pwr} above which the clamp will activate. The clamping activation voltage can be adjusted using different resistor ratios (R_B/R_A) within the multiplier circuit. For example, if V_{pwr} is 5 volts instead of 12 volts then the ratio R_B/R_A must be adjusted accordingly to ensure that the clamping circuit 12 operates
35 properly within the ASIC.

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A further feature of the clamping circuit 12 is the pull down circuit 14. The pull down circuit 14 operates to pull down the gate voltage of the power transistor where V_{pwr} is small (i.e. below 5 volts) or where V_{pwr} rises quickly.

- 5 For the low V_{pwr} cut off function, transistor M3 is designed (along with resistors R5 and R6) so as to be off until V_{pwr} reaches 5 volts or greater. Resistors R5 and R6 form a voltage divider for providing a gate voltage to M3 which is selected so that its turn-on threshold voltage is just below 5 volts. When V_{pwr} is less than 5 volts, M3 is off and consequently transistors M2 and M7 form a current mirror circuit which pulls down the
- 10 gate of the power transistor M0, thereby disabling the clamping function. When M3 is turned on, it pulls the gates of transistors M2 and M7 to ground, thus disabling the current mirror formed by those transistors so that the gate of the power transistor is not pulled to ground. This part of the pull down circuit 14 ensures that the clamping circuit 12 will not operate unless the power supply voltage, V_{pwr} is at a sufficient level to enable correct
- 15 operation of the clamping circuit 12. This is particularly important if the V_{pwr} rises very slowly. For example, if V_{pwr} rises slowly, V_{bg} may have risen to the correct operating level before V_{pwr} reaches a sufficient level to enable the clamping circuit 12 to work.

- On the other hand, if the power supply rises very quickly, the clamping circuit 12 can be
- 20 wrongly activated due to the time that it takes the band gap and operational amplifier to settle to the correct voltage levels. Transistor M4 is turned on or off by the level of the band gap reference voltage V_{bg} . The turn-on threshold of M4 is about 0.7 volts, which is the normal n-MOS operating threshold. M4 will not operate until V_{bg} reaches the n-MOS threshold. The normal operating level of V_{bg} is about 1.3 volts. Where the power supply
- 25 voltage rises quickly and V_{bg} lags behind, M4 will be off, thereby allowing transistors M5 and M6 (which form a current mirror) to operate to pull down the gate terminal of the power transistor. After V_{bg} rises to the correct level, M4 turns on and thereby pulls down the gates of transistors M5 and M6 to disable the current mirror and allow the clamp to operate without the gate of power transistor M0 being pulled down.

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The described clamping circuit 12 is capable of handling large currents while having accurate clamping activation with low tolerance in activation threshold voltage and may be provided at a low cost. These advantages are provided as follows.

5 1. Low Cost

Use of a multiplying circuit reduces the necessary power transistor size by the factor M for the same current. Thus it is very silicon effective.

10 2. Low tolerance in activation threshold voltage

Given that $(R2/R1) \gg [V_{TH} + V_{bg} \cdot (R3/R1)]/M$

15 $V_{clamp} \cong (R2/R1) \cdot V_{bg}$, which is independent of temperature. The tolerance is limited as the resistance matching between $R1$ and $R2$ can be achieved to within 0.5% and the bandgap voltage (V_{bg}) can be trimmed with a trimming facility. This means that a total tolerance between $R1$ and $R2$ of $\pm 2\%$ can be achieved.

20 3. Accuracy of activation

The pull down circuit ensures the correct clamping activation with minimal spurious clamping due to different power supply rise/fall slope.

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CLAIMS:

1. A transient voltage clamping circuit (12) of an integrated circuit (10) for a disk
5 drive, comprising:
a power transistor (M0) for sinking a power supply voltage (V_{pwr}) subjected to transient variation;
a reference circuit for deriving a first reference voltage (V_{ref}) from a second reference voltage (V_{bg}) and said power supply voltage (V_{pwr}); and
10 an amplifier circuit (13) for receiving said first reference voltage (V_{ref}) as input and for driving said power transistor (M0).
2. The circuit of claim 1, further comprising a pull-down circuit (14) connected to a gate terminal of said power transistor (M0) and an output of said amplifier circuit (13) for
15 controlling operation of said power transistor (M0).
3. The circuit of claim 2, wherein the pull-down circuit (14) is adapted to sink the gate voltage at said gate terminal when said power supply voltage (V_{pwr}) is less than a first threshold voltage, to thereby turn off said power transistor (M0).
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4. The circuit of claim 3, wherein the first threshold voltage is about 5 volts.
5. The circuit of claim 2 or claim 3, wherein the pull-down circuit (14) is adapted to sink the gate voltage at said gate terminal when said second reference voltage (V_{bg}) is less
25 than a second threshold voltage, to thereby turn off said power transistor M0.
6. The circuit of claim 5, wherein the second threshold voltage is about 0.7 volts.
7. The circuit of claim 1, wherein said amplifier circuit (13) includes a level shift
30 circuit (LSH), a voltage multiplier circuit (M) and a buffer circuit (X1).

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8. The circuit of claim 7, wherein said level shift circuit (LSH) is adapted to receive said first reference voltage (V_{ref}) as input and to output a level shifted voltage to said multiplier circuit (M), said multiplier circuit is adapted to receive said level shifted voltage as input and to output a multiplied voltage to said buffer circuit (X1) and said buffer circuit
5 is adapted to receive said multiplied voltage as input and to output a driving voltage to a gate terminal of said power transistor (M0).

9. The circuit of claim 1, wherein the first reference voltage (V_{ref}) is derived from the second reference voltage (V_{bg}) via coupled n-MOS and p-MOS current mirror circuits
10 (17,18) of said reference circuit.

10. The circuit of claim 9, wherein in said reference circuit an input current ($V_{bg}/R1$) of said coupled current mirror circuits (17,18) is driven by a current driving transistor (M1) in combination with an operational amplifier (16), said operational amplifier (16) receiving
15 said second reference voltage (V_{bg}) as input.