METHOD FOR REDUCING SILICIDED POLY GATE RESISTANCE FOR VERY SMALL TRANSISTORS

ABSTRACT

A method for reducing resistance in the fabrication of a silicided polysilicon gate for a very small transistor integrated circuit device is described. A polysilicon layer is deposited overlying a gate silicon oxide layer. The polysilicon and gate oxide layers are etched away where they are not covered by a mask to form a gate electrode. Ions are implanted to form source and drain regions within the semiconductor substrate using the gate electrode as a mask. A dielectric layer is deposited overlying the semiconductor substrate and the gate electrode. The dielectric layer is anisotropically etched to leave first spacers on the sidewalls of the gate electrode. The first spacers are isotropically etched back to leave second spacers extending approximately halfway up on the sidewalls of the gate electrode. A layer of titanium is conformally deposited over the surfaces of the substrate. The substrate is annealed whereby the titanium layer is transformed into a titanium silicide layer. The unreacted titanium on the oxide spacers is etched back to leave the titanium silicide layer only on the top surface and the sidewalls of the gate electrode not covered by the second spacers and overlying the source and drain regions. A second annealing transforms the titanium silicide to a phase of lower resistance. An insulating layer is blanket deposited over the substrate. Metallization with electrical connections is provided to complete the fabrication of the integrated circuit device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)