

Programmable Delay Control in a Memory

Abstract

5 A memory (13,14) has sense amplifiers (46) that provide data onto a
global data lines (56,74) that are received by secondary amplifiers (30,76).
The sense amplifiers (46) and the secondary amplifiers (30,76) are enabled
by clocks that are timed by programmable delay circuits (32,40,80). The
programmable delays are programmed by delay selection circuits (100-103)
10 that provide a continuous output to the programmable delay circuits
(32,40,80). There are two delay selection circuits (100-103). One is shared
by all of the programmable delay circuits (40) that enable the sense amplifiers
(46), and one is shared by all of the programmable delay circuits (32,80) that
enable the secondary amplifiers (30,76). The outputs of these two delay
15 selection circuits (100-103) are chosen to provide the output which programs
the programmable delay circuits (32,40,80) for optimizing the worst case of
the access time of the memory.

FIG. 1 to accompany abstract.

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