METHOD TO ENHANCE DEVICE PERFORMANCE WITH SELECTIVE STRESS RELIEF

Abstract

A structure and method of fabrication of a semiconductor device having a stress relief layer under a stress layer in one region of a substrate. In a first example, a stress relief layer is formed over a first region of the substrate (e.g., PFET region) and not over a second region (e.g., NFET region). A stress layer is over the stress relief layer in the first region and over the devices and substrate/silicide in the second region. The NFET transistor performance is enhanced due to the overall tensile stress in the NFET channel while the degradation in the PFET transistor performance is reduced/eliminated due to the inclusion of the stress relief layer. In a second example embodiment, the stress relief layer is formed over the second region, but not the first region and the stress of the stress layer is reversed.

Figure 5