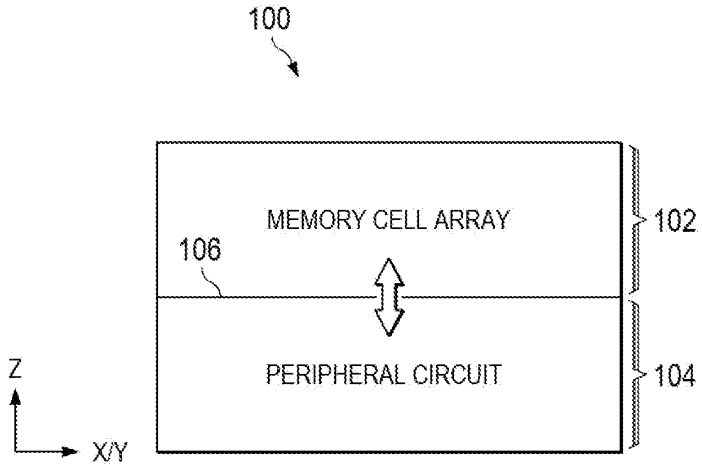

100
MEMORY CELL ARRAY
102
106
PERIPHERAL CIRCUIT
104
Z
X/Y

FIG. 1A

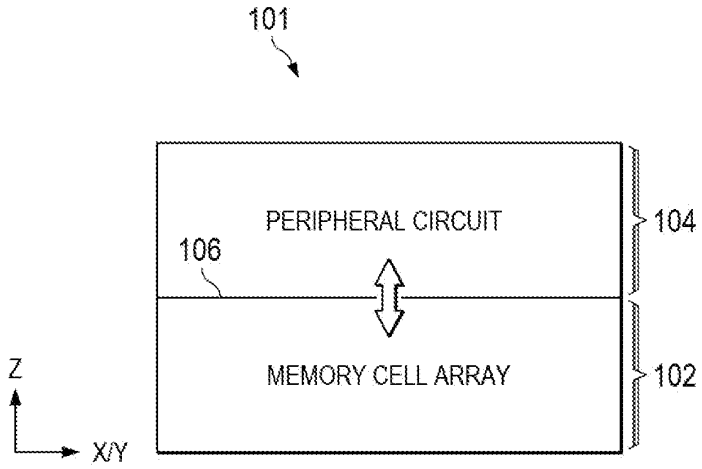

101
PERIPHERAL CIRCUIT
104
106
MEMORY CELL ARRAY
102
Z
X/Y

FIG. 1B

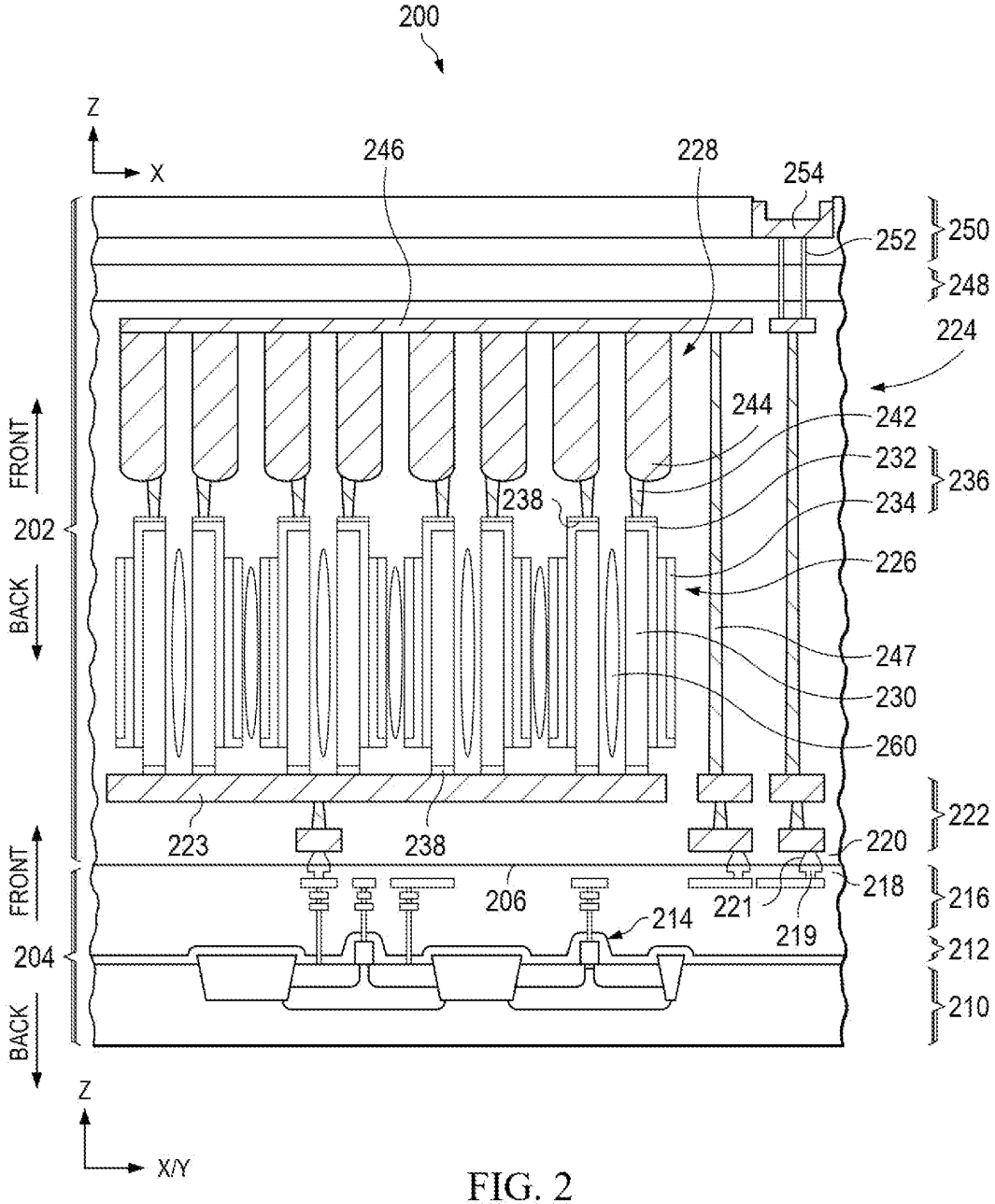

200
Z
X
246
228
254
252
250
248
224
244
242
232
236
238
234
226
247
230
260
222
223
238
220
218
216
206
214
221
219
212
210
FRONT
202
BACK
FRONT
204
BACK
Z
X/Y

FIG. 2

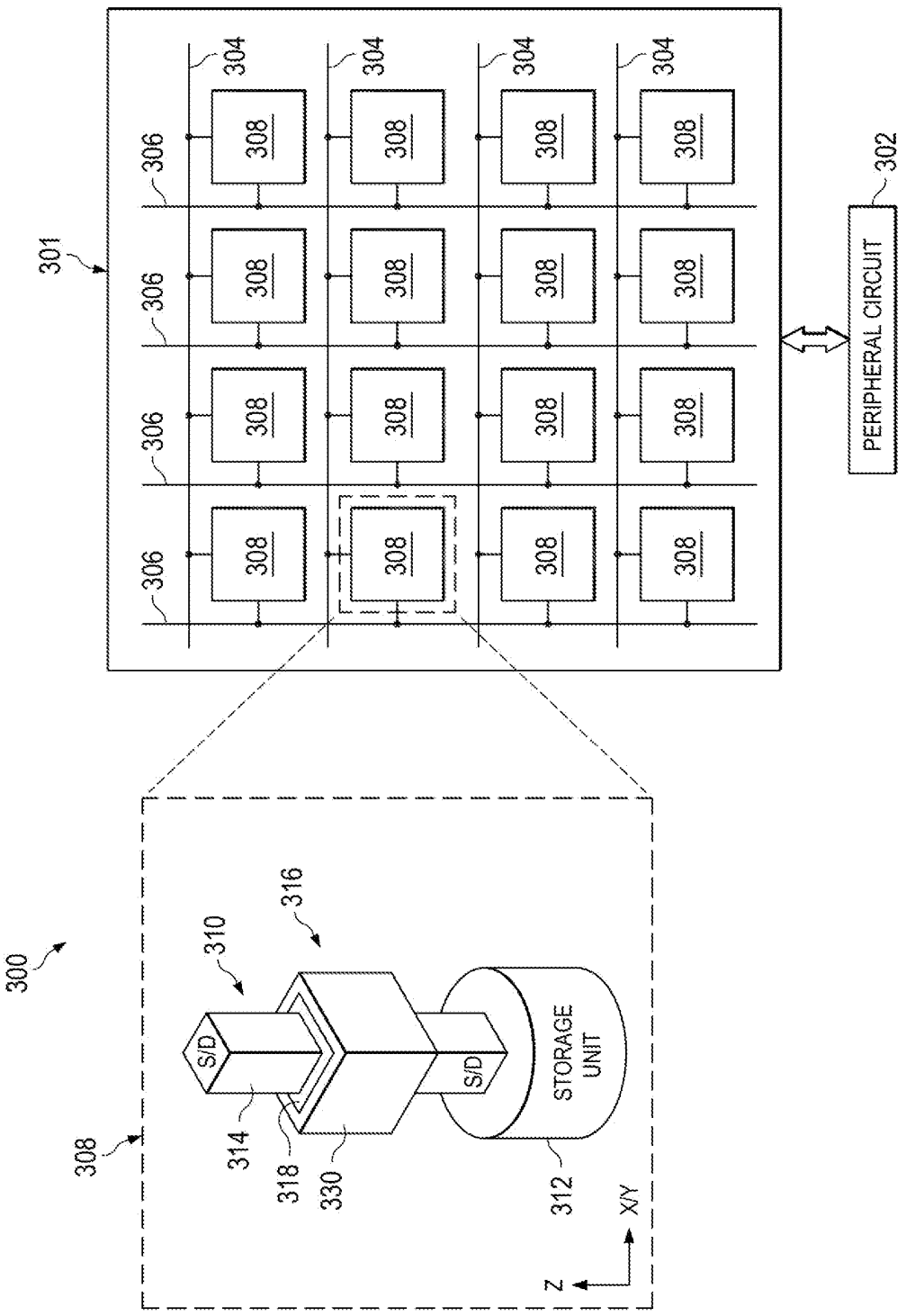

301
304
306
308
302
PERIPHERAL CIRCUIT
300
316
310
S/D
S/D
STORAGE UNIT
308
314
318
330
312
X/Y
Z

FIG. 3

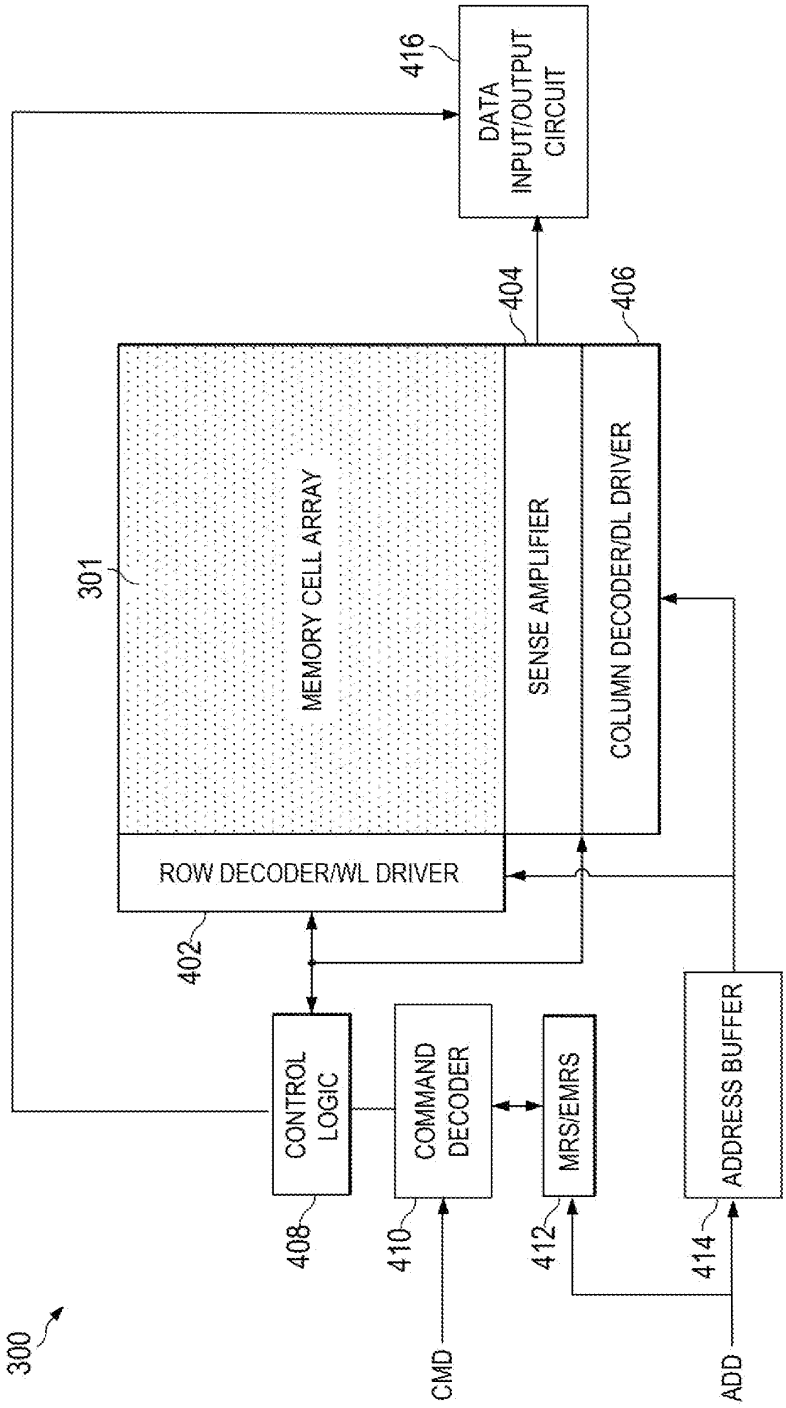

300
301
MEMORY CELL ARRAY
SENSE AMPLIFIER
COLUMN DECODER/DL DRIVER
ROW DECODER/WL DRIVER
DATA INPUT/OUTPUT CIRCUIT
CONTROL LOGIC
COMMAND DECODER
MRS/EMRS
ADDRESS BUFFER
CMD
ADD
402
404
406
408
410
412
414
416

FIG. 4

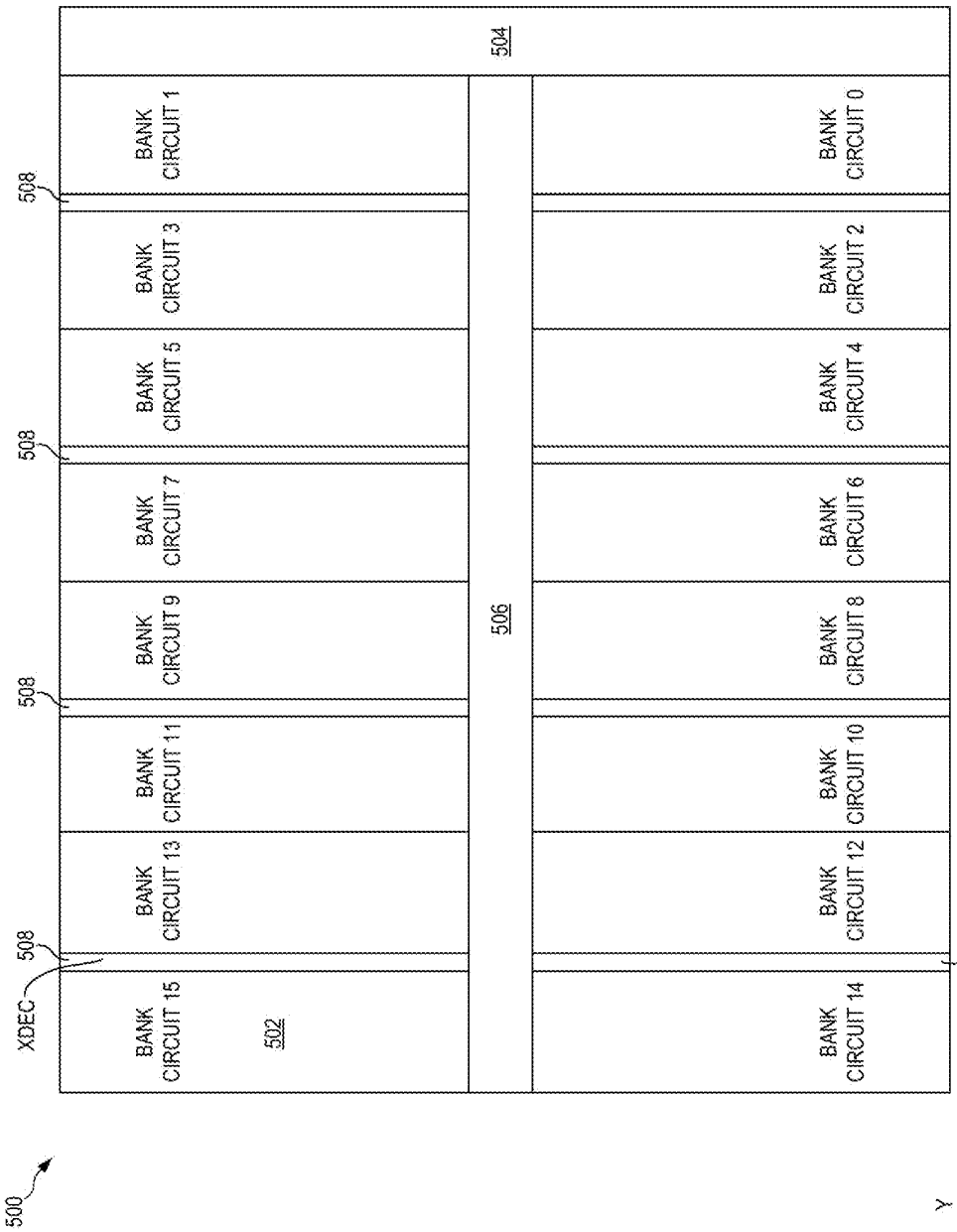

500
504
502
506
508
XDEC
BANK CIRCUIT 15
BANK CIRCUIT 13
BANK CIRCUIT 11
BANK CIRCUIT 9
BANK CIRCUIT 7
BANK CIRCUIT 5
BANK CIRCUIT 3
BANK CIRCUIT 1
BANK CIRCUIT 14
BANK CIRCUIT 12
BANK CIRCUIT 10
BANK CIRCUIT 8
BANK CIRCUIT 6
BANK CIRCUIT 4
BANK CIRCUIT 2
BANK CIRCUIT 0
Y
X

FIG. 5

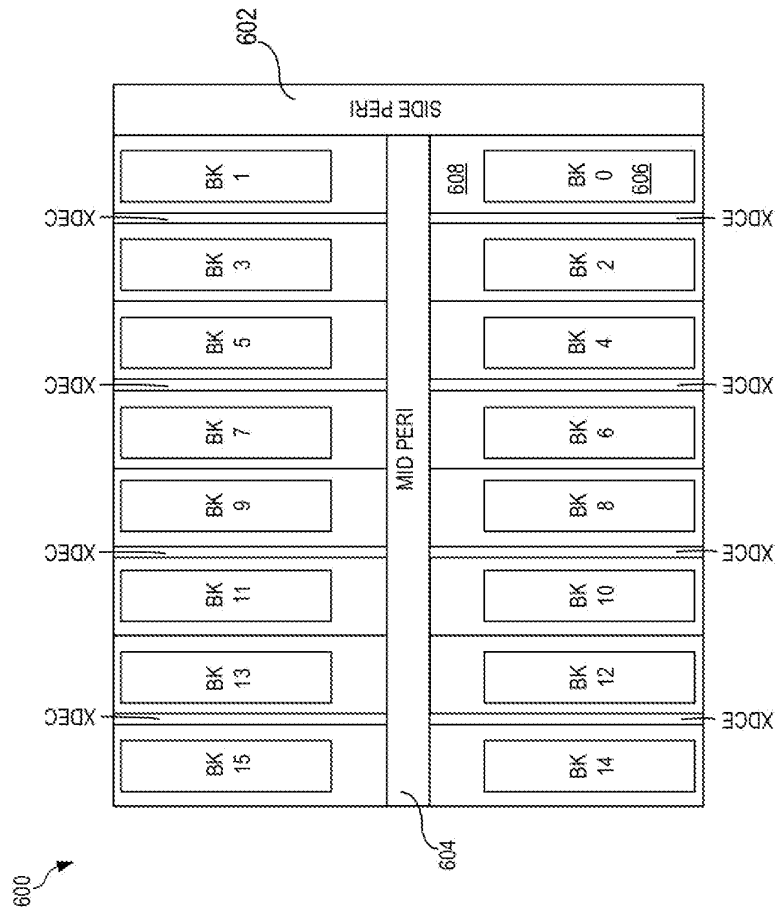

602
SIDE PERI
BK 1
BK 3
BK 5
BK 7
BK 9
BK 11
BK 13
BK 15
608
BK 0
606
BK 2
BK 4
BK 6
BK 8
BK 10
BK 12
BK 14
MID PERI
XDEC
XDEC
XDEC
XDEC
XDCE
XDCE
XDCE
XDCE
604
600

FIG. 6

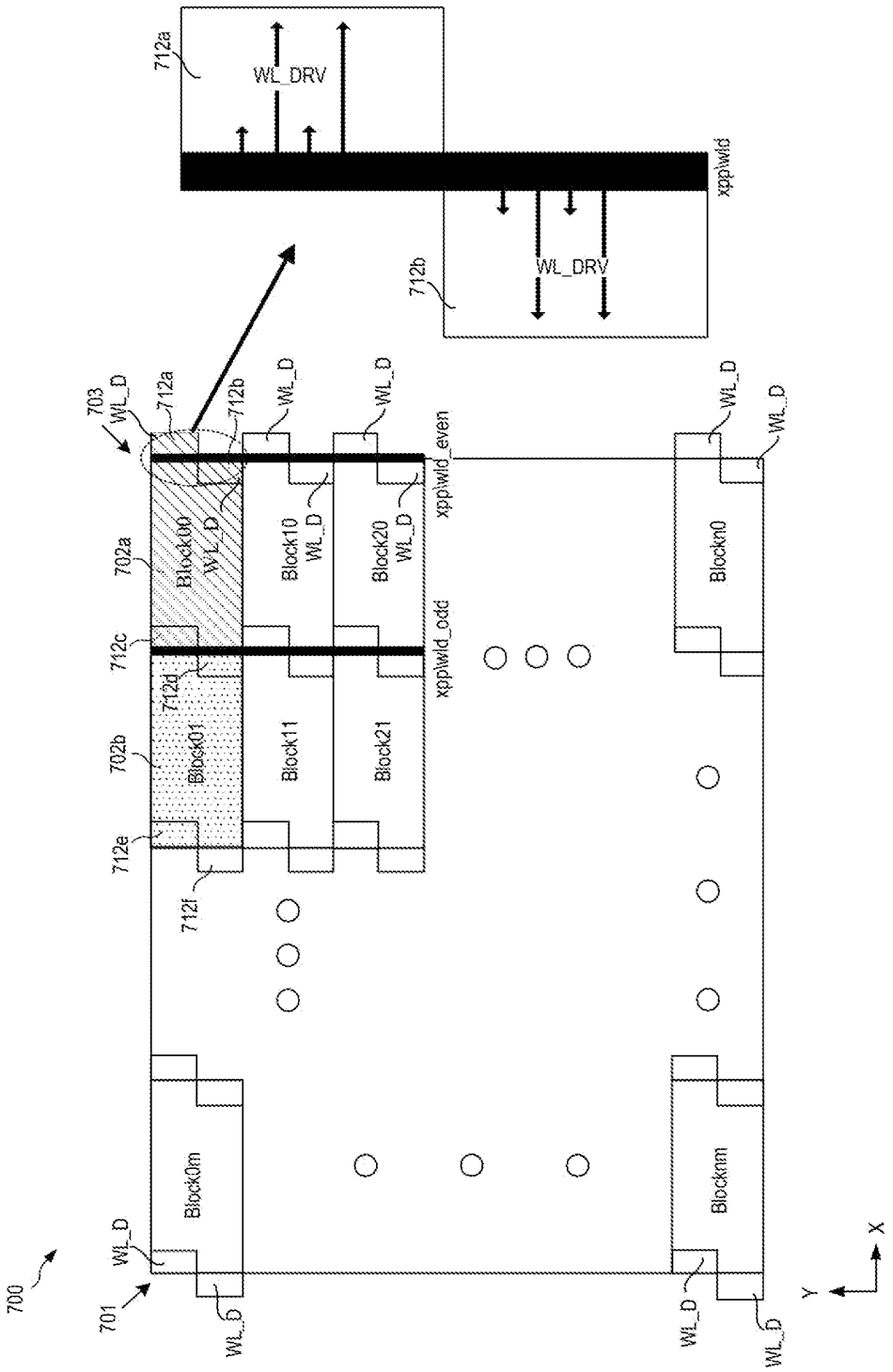

712a
WL_DRV
xppiwld
712b
WL_DRV
703
WL_D
712a
712b
WL_D
WL_D
xppiwld_even
WL_D
WL_D
Block00
WL_D
Block10
WL_D
Block20
WL_D
Blockn0
702a
712c
712d
xppiwld_odd
Block01
Block11
Block21
702b
712e
712f
Block0m
Blocknm
700
701
WL_D
WL_D
WL_D
WL_D
Y
X

FIG. 7

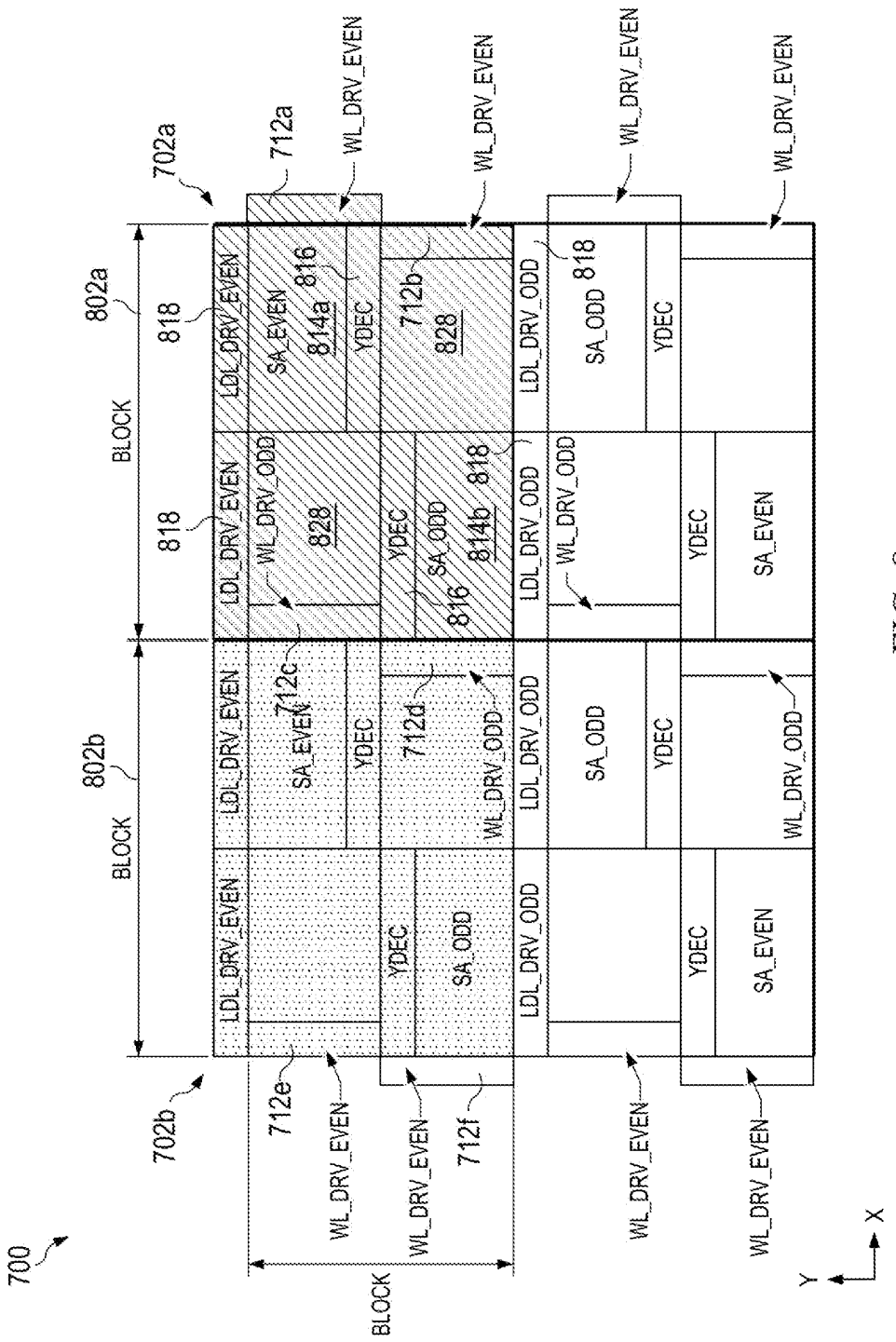

700
702a
712a
WL_DRV_EVEN
802a
BLOCK
818
LDL_DRV_EVEN
SA_EVEN
816
814a
YDEC
712b
828
LDL_DRV_ODD
SA_ODD
818
814b
WL_DRV_ODD
802b
712c
712d
WL_DRV_ODD
702b
712e
712f
X
Y

FIG. 8

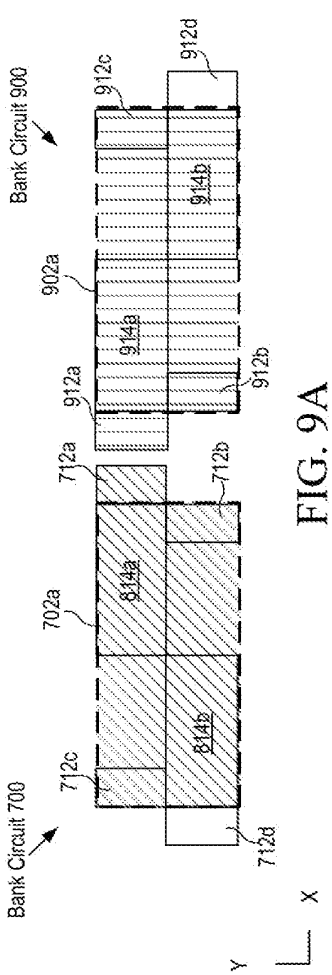

Bank Circuit 900
Bank Circuit 700
902a
912a
912b
912c
912d
712a
712b
712c
712d
702a
814a
814b
914a
914b
X
Y

FIG. 9A

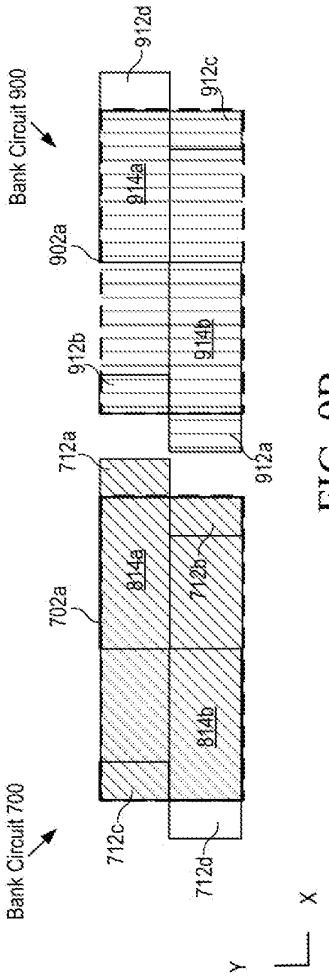

Bank Circuit 900
Bank Circuit 700
902a
912a
912b
912c
912d
712a
712b
712c
712d
702a
814a
814b
914a
914b
X
Y

FIG. 9B

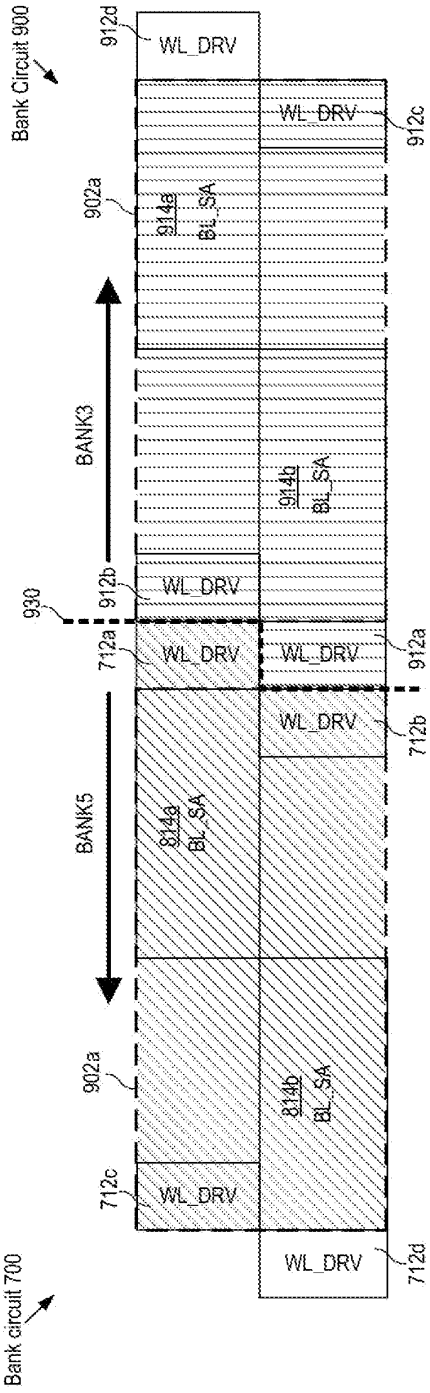

Bank Circuit 900
912d
WL_DRV
WL_DRV
912c
902a
914a
BL_SA
BANK3
914b
BL_SA
930
912b
WL_DRV
712a
WL_DRV
WL_DRV
912a
WL_DRV
712b
BANK5
914a
BL_SA
902a
914b
BL_SA
712c
WL_DRV
WL_DRV
712d
Bank circuit 700

FIG. 9C

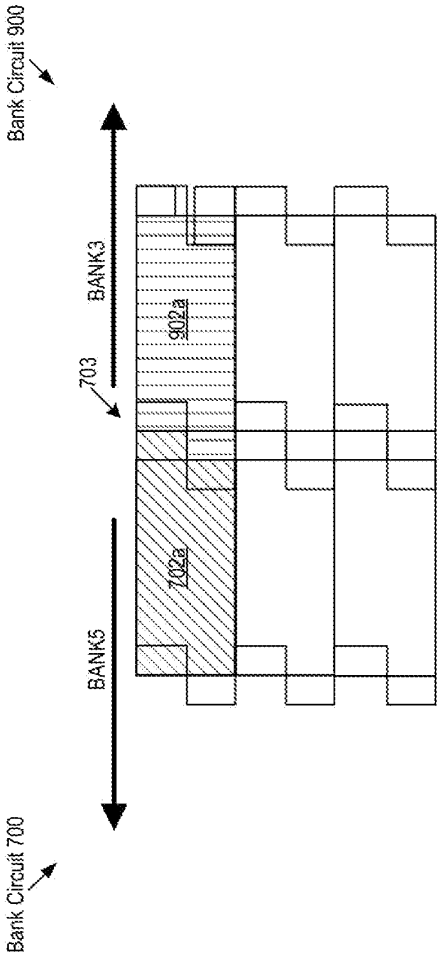

Bank Circuit 900
BANK3
902a
703
702a
BANK5
Bank Circuit 700

FIG. 9D

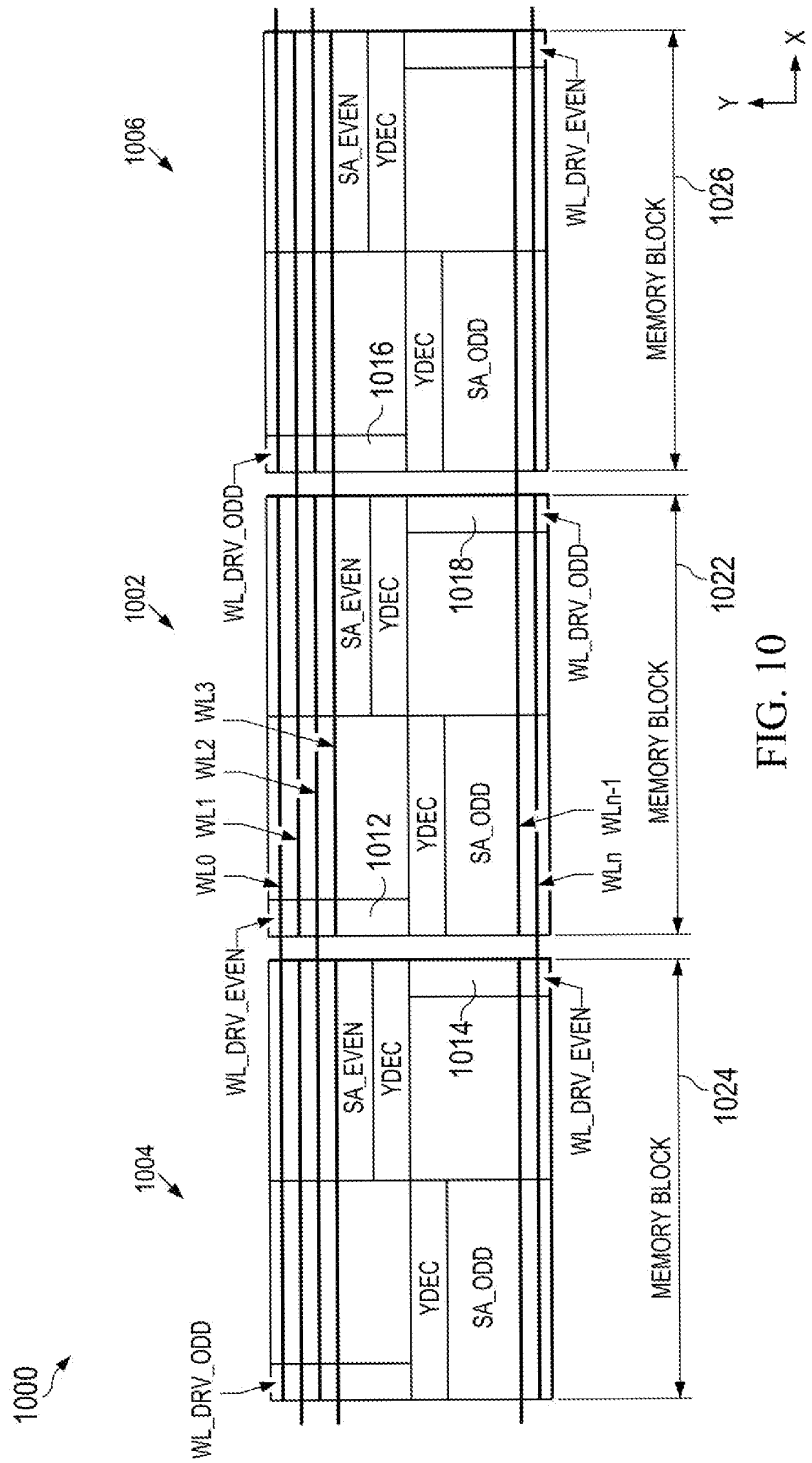

1000
1002
1004
1006
WL_DRV_ODD
WL_DRV_EVEN
WL_DRV_ODD
WL_DRV_EVEN
WL0
WL1
WL2
WL3
WLn-1
WLn
SA_EVEN
YDEC
SA_ODD
1012
1014
1016
1018
MEMORY BLOCK
1022
1024
1026
Y
X

FIG. 10

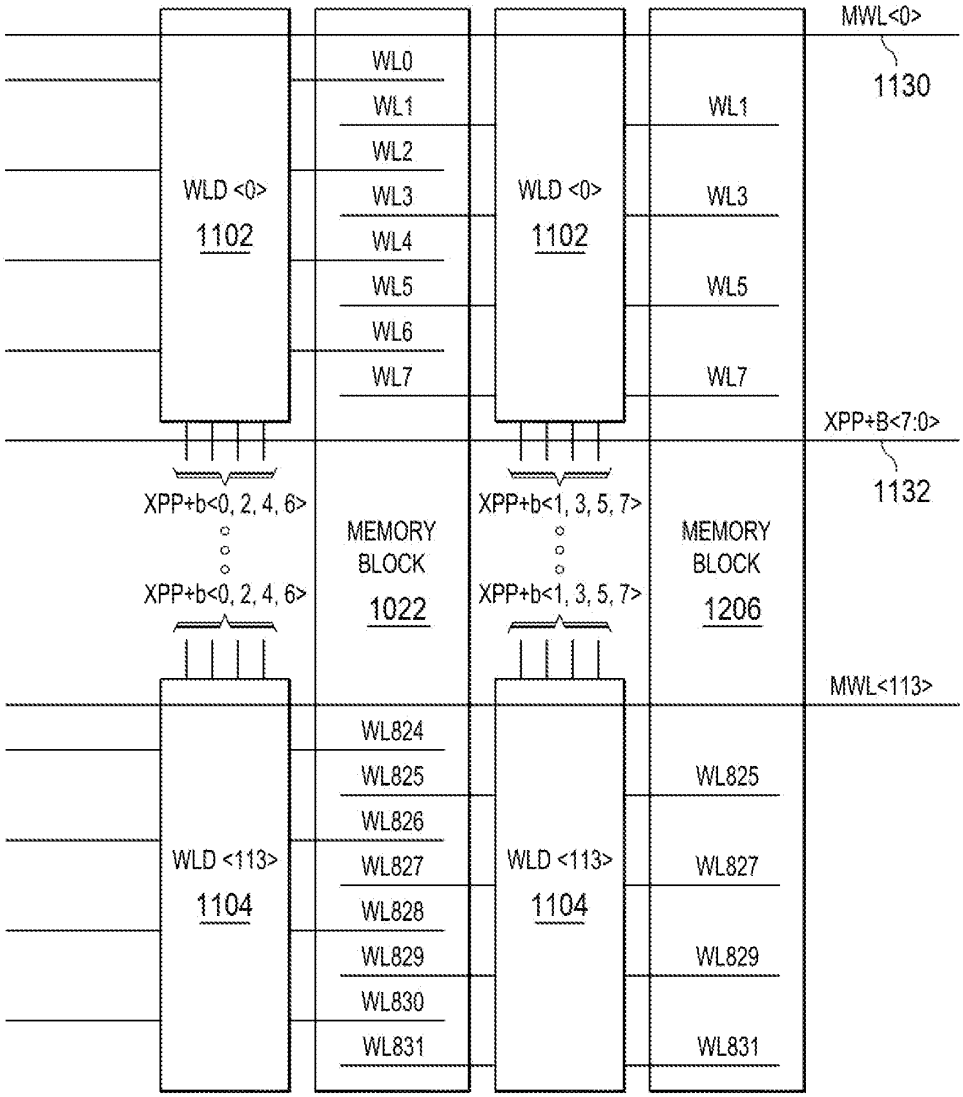

MWL<0>
1130
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WLD <0>
1102
WLD <0>
1102
WL1
WL3
WL5
WL7
XPP+B<7:0>
1132
XPP+b<0, 2, 4, 6>
XPP+b<0, 2, 4, 6>
MEMORY BLOCK
1022
XPP+b<1, 3, 5, 7>
XPP+b<1, 3, 5, 7>
MEMORY BLOCK
1206
MWL<113>
WL824
WL825
WL826
WL827
WL828
WL829
WL830
WL831
WLD <113>
1104
WLD <113>
1104
WL825
WL827
WL829
WL831

FIG. 11

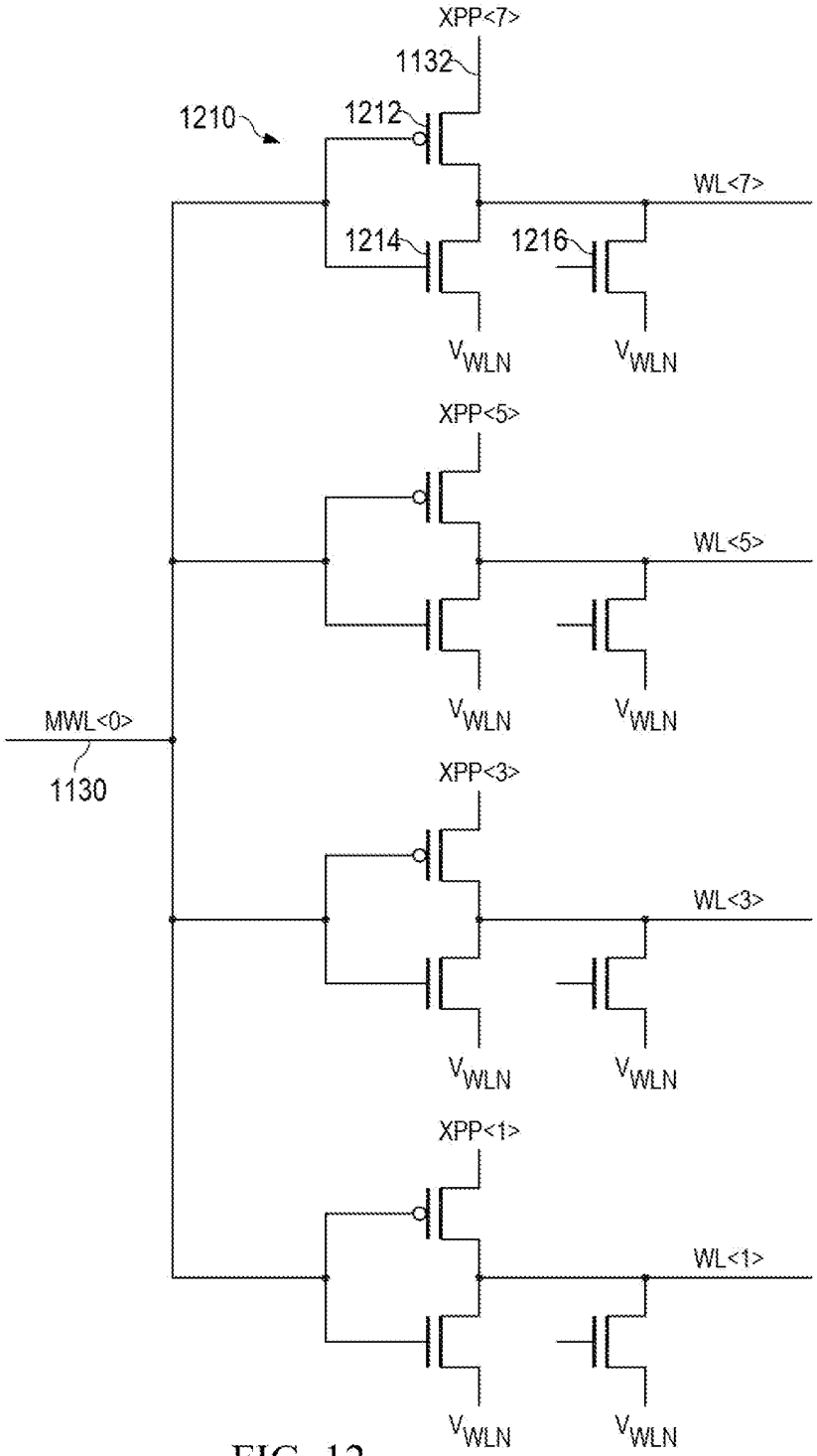

XPP<7>
1132
1210
1212
WL<7>
1214
1216
V_{WLN}
V_{WLN}
XPP<5>
WL<5>
MWL<0>
1130
V_{WLN}
V_{WLN}
XPP<3>
WL<3>
V_{WLN}
V_{WLN}
XPP<1>
WL<1>
V_{WLN}
V_{WLN}

FIG. 12

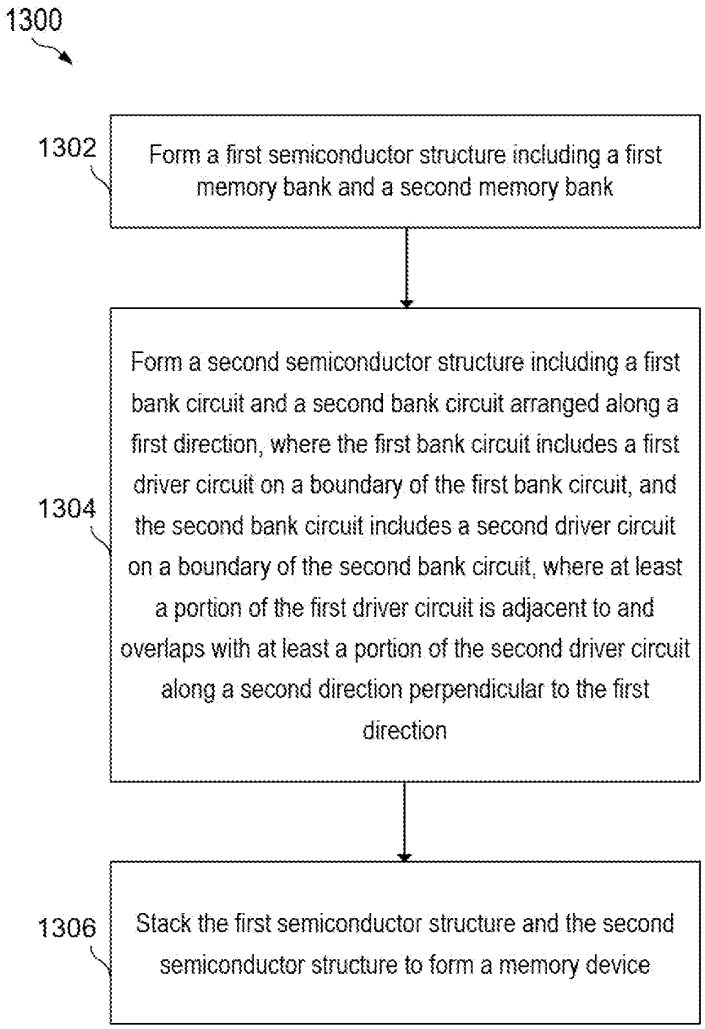

1300
1302
Form a first semiconductor structure including a first memory bank and a second memory bank
1304
Form a second semiconductor structure including a first bank circuit and a second bank circuit arranged along a first direction, where the first bank circuit includes a first driver circuit on a boundary of the first bank circuit, and the second bank circuit includes a second driver circuit on a boundary of the second bank circuit, where at least a portion of the first driver circuit is adjacent to and overlaps with at least a portion of the second driver circuit along a second direction perpendicular to the first direction
1306
Stack the first semiconductor structure and the second semiconductor structure to form a memory device

FIG. 13

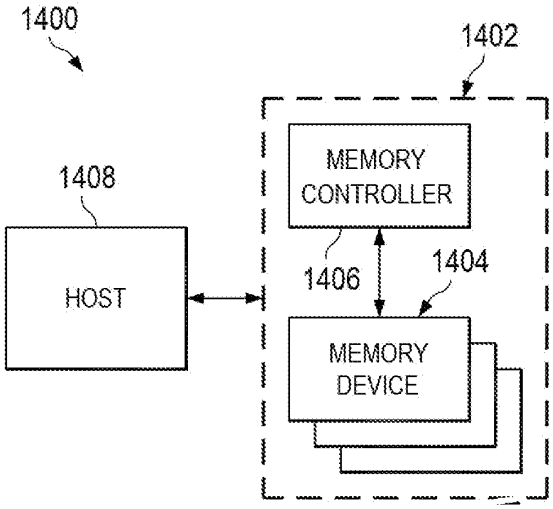

1400
1402
1408
MEMORY CONTROLLER
HOST
1406
1404
MEMORY DEVICE

FIG. 14

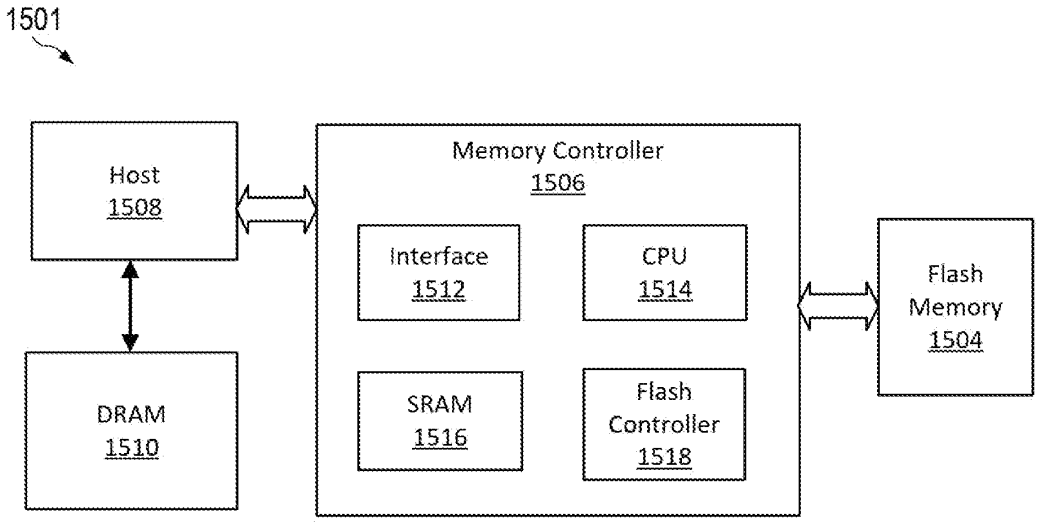


FIG. 15A

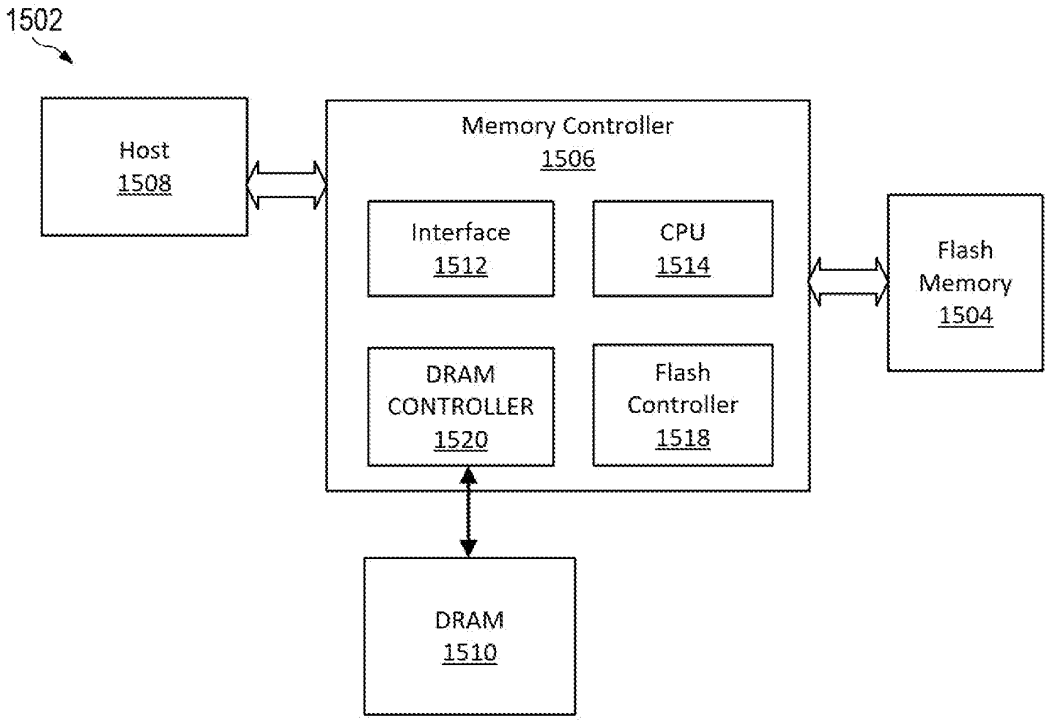


FIG. 15B