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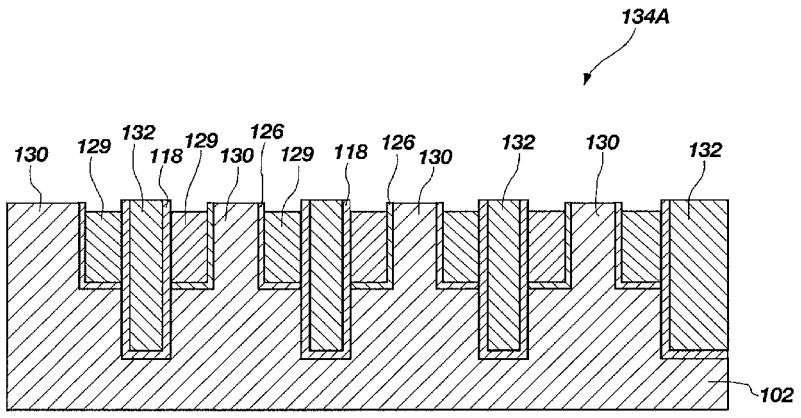


FIG. 8

(57) Abstract: Methods of isolating gates in a semiconductor structure. In one embodiment, isolation is achieved using a spacer material in combination with fins having substantially vertical sidewalls. In another embodiment, etch characteristics of various materials utilized in fabrication of the semiconductor structure are used to increase an effective gate length ("$L_{effective}$") and a field gate oxide. In yet another embodiment, a V-shaped trench is formed in the semiconductor structure to increase the $L_{effective}$ and the field gate oxide. Semiconductor structures formed by these methods are also disclosed.

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