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(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a process of making semiconductor integrated circuit devices having a plurality of active elements of different kinds formed in a single monocrystalline semiconductor body. The term "active elements of different kinds" is intended to mean transistors, diodes, etc., which differ in general structure. For example, an NPN transistor is different from a PNP transistor. The term is not meant to include elements having the same general structure but different operating parameters such as two NPN transistors of different base width.

Most prior integrated circuit devices have employed only one kind of active element, i.e. NPN bipolar transistors or P channel insulated gate field effect transistors, for example. Attempts to integrate other kinds of devices on the same chip have only been moderately successful. Additional processing steps have usually been required and significant losses in yield have resulted.

Some combinations of different kinds of devices have been prepared on a monocrystalline integrated circuit chip. For example, NPN—PNP bipolar combinations have been realized. Combinations of bipolar devices with insulated gate field effect transistors, however, have not been made with practical success, because processing steps required for the insulated gate field effect transistor have adversely affected the bipolar diffusions.

P channel insulated gate field effect transistors have been combined with N channel insulated gate field effect transistors, but their gate insulators have been complex and difficult to control as to cleanliness, fixed positive charge, and thickness.

According to the invention we provide a method of making a monolithic integrated circuit device which includes a body of semiconductive material containing at least two active elements of different kinds, at least one of which is an insulated gate field effect transistor having spaced source and drain regions of one type conductivity defining a charge carrier channel and a gate electrode adjacent to said channel and separated therefrom by an insulator, comprising heating said body, to form the gate insulator, in a wet oxidizing atmosphere which includes a hydrogen halide, and reheating said body at a temperature between about 900°C and 1200°C in a non-oxidizing atmosphere. The diffused regions of a bipolar transistor on the same chip are not adversely effected by this process below 1000°C. The insulators are easily controllable for cleanliness, fixed charge, and thickness.

In the accompanying drawings:—

FIGURES 1 to 6 are a sequence of cross sections illustrating the steps of the present novel process.

Example

FIGURE 6 illustrates the cross sectional structure of an integrated circuit device 10 of the kind which can be prepared by the present novel process. In the embodiment shown in FIGURE 6, the device 10 includes a P type substrate 12 which has an upper boundary 14 on which is disposed a layerlike body 16 of semiconductive material of N type conductivity. The body 16 has a surface 17 spaced from and substantially parallel to the boundary 14 of the substrate 12. The body 16 may be, for example, an epitaxial layer on the boundary 14 of the substrate 12.

In the device 10, as shown, there are three different active elements. At the left side of the figure is a p channel insulated gate field effect transistor 18 and at the right side of the figure there is an N channel insulated

gate field effect transistor 20. Between the transistors 18 and 20 is a bipolar transistor 22.

The bipolar transistor 22 is of conventional construction. It includes a buried region 24, which is of N+ type conductivity in this example, a P type base region 26, formed by diffusion of acceptor impurities into the body 16 through its surface 17, and an N+ type emitter region 28, formed by the diffusion of donor impurities into the body 16. The original N type material of the body 16 constitutes the collector region of the transistor 22. If desired, a collector contact diffusion, shown as a region 30, may be provided. Emitter, base and collector contacts 32, 33, and 34 are provided to connect the transistor 22 to other elements in the device. The transistor 22 is isolated from the transistors 18 and 20 by diffused P+ type regions 35.

The P channel insulated gate field effect transistor 18 has spaced source and drain regions 36 and 38, respectively, formed adjacent to the surface 17 of the body 16 and defining the ends of a charge carrier channel. A gate electrode structure 40 overlies the space between the source and drain regions 36 and 38. The gate electrode structure 40 comprises a gate electrode 42, which may be aluminium or silicon for example, disposed adjacent to the space between the source and drain regions 36 and 38 separated therefrom by an insulator 44.

The N channel insulated gate field effect transistor 20 has a structure similar to that of the transistor 18. Its substrate, however, is a diffused region 46 in the body 16. Within the region 46 are spaced source and drain regions 48 and 50, respectively, and over the space between these regions is a gate electrode structure 52 which comprises a gate electrode 54 separated from the semiconductor body 16 by an insulator 56.

The different elements shown in FIGURE 6 may be included in any combination of two or more in any integrated circuit devices, that is, there may be a P or an N channel insulated gate field effect transistor with either or both of a bipolar transistor and an insulated gate field effect transistor of opposite type conductivity. The material in which the elements are formed may be epitaxial material as shown in FIGURE 6 or it may be bulk semiconductor material. The epitaxial embodiment is preferred because it is similar to other integrated circuit devices presently known and can be readily introduced into existing manufacturing facilities.

The present novel process begins with the substrate 12 which is, in this example, of P type conductivity with a resistivity between about 0.5 and about 100 ohm cm. An N+ region 24s (FIGURE 1) is first formed in the substrate 12 adjacent to its boundary 14 by known photolithographic and diffusion techniques.

The next step in the present process is to grow an N type epitaxial layer on the boundary 14 of the substrate 12 to form the body 16. During this epitaxial growth process donor impurities from the region 24s diffuse upwardly into the body 16 to form the buried region 24 in the configuration shown in FIGURE 2. In this example, the epitaxial growth condition is adjusted in known fashion to provide a resistivity of about 0.2 to 40 ohm cm. in the body 16.

FIGURE 3 illustrates the next two steps in the present process. The first of these is to diffuse the P type substrate region 46 for the N channel insulated gate field effect transistor 20. After the completion of this step, a diffusion of acceptors is performed to establish the P+ type isolation zones 35.

The source and drain regions 36 and 38 and the base region 26 of the bipolar transistor 22 are next formed by a simultaneous diffusion process. The result is as shown in FIGURE 4. While these regions are of P type conductivity like the region 46 and the isolation zones 35 they should not be formed at the same time as these latter regions. The region 46 should have a relatively lower surface concentration of acceptors in order to reduce the threshold voltage of the insulated gate field effect transistor 20. The isolation zones on the other hand are deeper in order to maintain adequate isolation. The surface concentration of acceptor impurities in the region 46 should not be substantially in excess of $5 \times 10^{16}/cm^3$. This doping level may be achieved, for example, by carefully controlling the diffusion of this region.

The next step in the present process is the simultaneous formation, by known diffusion techniques, of the emitter 28 of the bipolar transistor 22, the collector contact 30, and the source and drain regions 48 and 50 respectively of the N channel transistor 20. The result of this step is illustrated in FIGURE 5.

The next step after the N+ diffusion is the formation of the gate insulators 44 and 56 for the two insulated gate field effect transistors 18 and 20. These insulators are also shown in FIGURE 5.

The insulators 44 and 56 should be formed in a manner which will reduce the density of effective fixed charge therein to a relatively low value. To achieve this, the entire surface 17 of the epitaxial body 16 is masked with a silicon dioxide mask layer 60 (FIGURE 5) and openings 62 are provided adjacent to the channel regions of the two transistors. The device 10 is then heated to a temperature of about 875°C in a wet oxidizing atmosphere which contains a hydrogen halide, such as an atmosphere of water vapor and gaseous hydrogen chloride derived by evaporation from an azeotropic mixture of water and hydrochloric

acid. The halide provides a chemical reaction with impurities, derived from the semiconductor body in the insulators 44 and 56 to form volatile chlorides thereof.

After the insulators 44 and 56 have been grown they should be annealed in a non-oxidizing atmosphere at relatively high temperature, i.e., between about 900°C and about 1200°C. Suitable atmospheres are hydrogen, forming gas, or helium. This annealing treatment produces a decrease in the density of fixed charge. Care is taken to insure that the surface concentration of acceptors in the P type region 46 is sufficiently low so that the threshold voltage of the N channel transistor 20 is not unduly increased by the oxidizing and annealing processes. Where there is a bipolar transistor such as the transistor 22 on the chip, the annealing temperature should be kept below about 1000°C in order to prevent undesired diffusion of the emitter region.

From this point, processing is conventional and is illustrated in FIGURE 6. Contact openings are formed, a metal layer is evaporated onto the surface and the interconnection pattern of the device is formed in the metal layer to provide the contacts shown in FIGURE 6. A final annealing heat treatment may be performed, at a temperature of about 450°C for about 15 minutes, after which the device may be packaged in known fashion.

The halide oxidation and high temperature annealing process, together with low surface concentration of impurities in the channel region 46, result in an improvement in the threshold voltage of both insulated gate field effect transistors when these two devices are present on the same chip. Where an insulated gate field effect transistor is combined with a bipolar transistor, the halide oxidation and annealing processes described allow the fabrication of the insulated gate field effect transistor without adversely affecting the diffusions for the bipolar transistor.

WHAT WE CLAIM IS:—

1. A method of making a monolithic integrated circuit device which includes a body of semiconductive material containing at least two active elements of different kinds, at least one of which is an insulated gate field effect transistor having spaced source and drain regions of one type conductivity defining a charge carrier channel and a gate electrode adjacent to said channel and separated therefrom by an insulator, comprising heating said body, to form the gate insulator, in a wet oxidizing atmosphere which includes a hydrogen halide, and reheating said body at a temperature between about 900°C and 1200°C in a non-oxidizing atmosphere.

2. A method as in claim 1, wherein at least one other of said active elements is an insulated gate field effect transistor having spaced source and drain regions of conductivity type opposite to that of the source and drain regions of the first mentioned insulated gate field effect transistor.

3. A method as in claim 1, wherein said wet oxidizing atmosphere is derived from an azeotropic mixture of water and hydrochloric acid.

4. A method as in claim 3, wherein said non-oxidizing atmosphere is a hydrogen-containing gas.

5. A method as in claim 1, wherein at least one other of said active elements is a bipolar transistor having emitter, base and collector regions.

6. A method as in claim 5 comprising the further step of diffusing at least one region of said bipolar transistor simultaneously with the source and drain regions of said insulated gate field effect transistor.

7. A method of making a monolithic integrated circuit device comprising a body of semiconductive material of one type conductivity having a surface, a region of conductivity type opposite to that of said body in said body adjacent to said surface, spaced source and drain regions of said one type conductivity within said region adjacent to said surface, spaced source and drain regions of said opposite type conductivity outside of said diffuse region adjacent to said surface and a gate electrode over the space between each pair of source and drain regions and separated therefrom by an insulator, characterized by said insulator being formed by heating said body in a wet oxidizing atmosphere which contains a hydrogen halide.

8. A method as in claim 7, wherein said oxidizing atmosphere is a mixture comprising water vapor and gaseous hydrogen chloride.

9. A method as in claim 8, comprising the further step of reheating said body at a temperature between about 900°C to 1200°C in a non-oxidizing atmosphere.

10. A method as in claim 7, wherein said body is an epitaxial layer formed on a substrate of conductivity type opposite to that of said body.

11. A method as in claim 7, wherein said integrated circuit device further comprises diffused regions in said epitaxial layer defining a bipolar transistor, said method further comprising diffusing at least one of said regions simultaneously with one pair of said source and drain regions.

12. A method as in claim 11, further comprising diffusing one other of said regions of

acid. The halide provides a chemical reaction with impurities, derived from the semiconductor body in the insulators 44 and 56 to form volatile chlorides thereof.

After the insulators 44 and 56 have been grown they should be annealed in a non-oxidizing atmosphere at relatively high temperature, i.e., between about 900°C and about 1200°C. Suitable atmospheres are hydrogen, forming gas, or helium. This annealing treatment produces a decrease in the density of fixed charge. Care is taken to insure that the surface concentration of acceptors in the P type region 46 is sufficiently low so that the threshold voltage of the N channel transistor 20 is not unduly increased by the oxidizing and annealing processes. Where there is a bipolar transistor such as the transistor 22 on the chip, the annealing temperature should be kept below about 1000°C in order to prevent undesired diffusion of the emitter region.

From this point, processing is conventional and is illustrated in FIGURE 6. Contact openings are formed, a metal layer is evaporated onto the surface and the interconnection pattern of the device is formed in the metal layer to provide the contacts shown in FIGURE 6. A final annealing heat treatment may be performed, at a temperature of about 450°C for about 15 minutes, after which the device may be packaged in known fashion.

The halide oxidation and high temperature annealing process, together with low surface concentration of impurities in the channel region 46, result in an improvement in the threshold voltage of both insulated gate field effect transistors when these two devices are present on the same chip. Where an insulated gate field effect transistor is combined with a bipolar transistor, the halide oxidation and annealing processes described allow the fabrication of the insulated gate field effect transistor without adversely affecting the diffusions for the bipolar transistor.

WHAT WE CLAIM IS:—

1. A method of making a monolithic integrated circuit device which includes a body of semiconductive material containing at least two active elements of different kinds, at least one of which is an insulated gate field effect transistor having spaced source and drain regions of one type conductivity defining a charge carrier channel and a gate electrode adjacent to said channel and separated therefrom by an insulator, comprising heating said body, to form the gate insulator, in a wet oxidizing atmosphere which includes a hydrogen halide, and reheating said body at a temperature between about 900°C and 1200°C in a non-oxidizing atmosphere.

2. A method as in claim 1, wherein at least one other of said active elements is an insulated gate field effect transistor having spaced source and drain regions of conductivity type opposite to that of the source and drain regions of the first mentioned insulated gate field effect transistor.

3. A method as in claim 1, wherein said wet oxidizing atmosphere is derived from an azeotropic mixture of water and hydrochloric acid.

4. A method as in claim 3, wherein said non-oxidizing atmosphere is a hydrogen-containing gas.

5. A method as in claim 1, wherein at least one other of said active elements is a bipolar transistor having emitter, base and collector regions.

6. A method as in claim 5 comprising the further step of diffusing at least one region of said bipolar transistor simultaneously with the source and drain regions of said insulated gate field effect transistor.

7. A method of making a monolithic integrated circuit device comprising a body of semiconductive material of one type conductivity having a surface, a region of conductivity type opposite to that of said body in said body adjacent to said surface, spaced source and drain regions of said one type conductivity within said region adjacent to said surface, spaced source and drain regions of said opposite type conductivity outside of said diffuse region adjacent to said surface and a gate electrode over the space between each pair of source and drain regions and separated therefrom by an insulator, characterized by said insulator being formed by heating said body in a wet oxidizing atmosphere which contains a hydrogen halide.

8. A method as in claim 7, wherein said oxidizing atmosphere is a mixture comprising water vapor and gaseous hydrogen chloride.

9. A method as in claim 8, comprising the further step of reheating said body at a temperature between about 900°C to 1200°C in a non-oxidizing atmosphere.

10. A method as in claim 7, wherein said body is an epitaxial layer formed on a substrate of conductivity type opposite to that of said body.

11. A method as in claim 7, wherein said integrated circuit device further comprises diffused regions in said epitaxial layer defining a bipolar transistor, said method further comprising diffusing at least one of said regions simultaneously with one pair of said source and drain regions.

12. A method as in claim 11, further comprising diffusing one other of said regions of

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said bipolar transistor simultaneously with the other pair of source and drain regions.

13. A method of making a monolithic integrated circuit device substantially as described in the example disclosed herein.

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