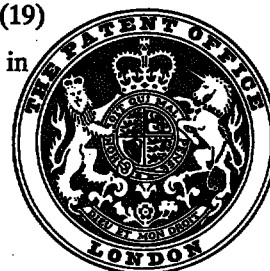


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(54) ELECTRONIC TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:-

5 This invention relates to electronic timepieces and in particular, although not so 5 restricted, to electronic watches.

10 The accuracy of an electronic timepiece depends upon an oscillator circuit which is used as a time standard. A crystal oscillator circuit used in an electronic watch usually incorporates a quartz crystal vibrator. The power consumption of an electronic watch is 10 dependent mainly upon the power consumption of a display device for displaying a time indication and time keeping circuitry controlled by the quartz crystal vibrator. Recently the time keeping circuitry in an electronic watch has been constructed as a semiconductor integrated circuit. The power dissipated in an integrated circuit broadly consists of static power consumption which does not depend on the operating frequency in 15 the integrated circuit and dynamic power consumption which is proportional to the operating frequency. 15

20 The accuracy of a quartz crystal vibrator mainly depends upon the rate of change of natural vibration frequency with temperature. A tuning fork type crystal vibrator, having a natural vibration frequency of 32 KHZ, is widely used as a time standard in present day watches. However, the temperature characteristics of a tuning fork type crystal vibrator are 20 not good. Thus an electronic watch having a tuning fork type crystal vibrator may gain or lose up to 10 seconds per month. On the other hand, when an AT cut quartz crystal vibrator having a natural frequency of 4 MHZ is used in an electronic watch an accuracy of about 10 seconds per year is achieved. Therefore, it is clear that the accuracy of an electronic watch 25 increases with the frequency of the time standard. 25

30 In the past, great efforts have been made to improve the accuracy of electronic watches. One way to improve electronic watches is to use an AT cut quartz crystal vibrator having a natural vibration frequency of 4 MHZ as the time stand. However, this causes the dynamic power consumption in the integrated time keeping circuitry to increase. Thus an electronic watch having a crystal vibrator with a natural vibration frequency of 4 MHZ has a power consumption in the integrated time keeping circuitry of at least a hundred times that of the power consumption of an electronic watch having a crystal vibrator whose natural vibration frequency is 32 KHz. 30

35 Actually, in an electronic watch having time indicating hands and quartz crystal vibrator with a natural vibration frequency of 32 KHz, the power consumption will be about 2μW. 35 However, if the quartz crystal vibrator has a natural vibration frequency of 4 MHZ the electronic watch will consume more than 10μW. From the above, it will be appreciated that an electronic watch using a crystal vibrator whose natural vibration frequency is 32 KHz can be operated continuously for more than five years without the need to exchange a driving battery, whilst an electronic watch using a crystal vibrator whose natural vibration frequency is 4 MHZ can be operated continuously for only one year. 40

45 According to the present invention there is provided an electronic timepiece comprising: a time standard; time keeping circuitry controlled by the time standard; and display means for displaying a time indication in response to an output of the time keeping circuitry, the time keeping circuitry including at least one static induction transistor. 45

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Preferably the time standard is a vibrator whose natural frequency of vibration is 1 MHz or greater, said static induction transistor being included in an amplifying circuit.

In the preferred embodiment the time keeping circuitry includes a driver circuit for driving the display means, said driver circuit including the or a said static induction transistor.

The display means may be a digital display means.

Preferably the or each said static induction transistor is operated in such a manner that its gate current is substantially zero and no drain current flows under conditions of zero bias and a gate current which is smaller than the drain current flows when the static induction transistor is biased in the forward direction.

The time keeping circuitry may include a frequency divider circuit having a plurality of flip-flop stages, each of which includes a static induction transistor.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a plan view of one embodiment of an electronic watch according to the present invention;

Figure 2 is a block diagram of the circuitry of the electronic watch shown in Figure 1;

Figure 3 illustrates the construction of an inverter of one embodiment of an electronic timepiece according to the present invention;

Figure 4 is a plan view of the inverter of Figure 3;

Figures 5(a) and 5(b) are electrical equivalent circuit diagrams of the inverter of Figure 3;

Figure 6 is a logic diagram of the inverter of Figure 3;

Figure 7 shows graphically the relationship between voltage and current of the inverter of Figure 3;

Figure 8 illustrates, in cross-section, a NAND gate of an electronic timepiece according to the present invention;

Figure 9 is a plan view of the NAND gate shown in Figure 8;

Figure 10 is an equivalent circuit diagram of the NAND gate shown in Figure 8;

Figure 11 is a logical diagram of the NAND gate shown in Figure 8;

Figure 12 is a block diagram of a crystal oscillator circuit for an electronic watch according to the present invention;

Figure 13 is a detailed circuit diagram of the oscillator circuit shown in Figure 12;

Figure 14 is a block diagram of a frequency divider circuit of another embodiment of an electronic watch according to the present invention;

Figure 15 is a logic diagram of a T-type flip-flop of Figure 14;

Figure 16 is an equivalent circuit diagram of the T-type flip-flop shown in Figure 15;

Figure 17 is a six-advance counting circuit of an electronic timepiece according to the present invention;

Figure 18 is a logic diagram of a D-type flip-flop of the counting circuit of Figure 17;

Figure 19 is a equivalent circuit diagram of the D-type flip-flop shown in Figure 18;

Figure 20 is a logic diagram of a signal converting circuit of an electronic timepiece according to the present invention;

Figure 21 is an equivalent circuit diagram of the signal converting circuit shown in Figure 20;

Figure 22(a) is a block diagram illustrating the connection between integrated time keeping circuitry and a display device of an electronic timepiece according to the present invention;

Figure 22(b) is an equivalent circuit diagram of the arrangement shown in Figure 22(a);

Figure 23 is a block diagram of a driving circuit driving a liquid crystal display device of an electronic timepiece according to the present invention;

Figure 24(a) is a logic diagram of an exclusive OR gate;

Figure 24(b) is a logic diagram of an exclusive OR gate shown in Figure 24(a);

Figure 25 is an equivalent circuit diagram of an exclusive OR gate of an electronic timepiece according to the present invention.

Figure 26 is a circuit diagram of a switching circuit of an electronic timepiece according to the present invention.

Figure 27(a) is a plan view of another embodiment of an electronic watch according to the present invention;

Figure 27(b) is a block diagram of the watch of Figure 27(a); and

Figure 27(c) is a circuit diagram of a driving circuit of the electronic watch of Figure 27(a).

Throughout the drawings like parts have been designated by the same reference numerals. The invention is described hereinafter as applied to an electronic watch but it is equally applicable to all forms of electronic timepieces.

Figure 1 is a plan view of one embodiment of an electronic watch according to the present

invention. A digital display device 2 is located in a centre region of a watch case 1 so that it can be seen clearly from the exterior. In addition, there are two push-buttons switches 3a, 3b for setting the time indication and a watch strap 4 attached to the case 1. In the case 1 there is a battery, a quartz crystal vibrator, and integrated time keeping circuitry, all of which are not shown, and which are connected in such a way that the display device 2 displays a time indication.

Figure 2 is a block diagram of the circuitry of the electronic watch shown in Figure 1. A crystal oscillator circuit 5 incorporating a quartz crystal vibrator having a natural vibration frequency of 4 MHz as a time standard, produced an output signal which is frequency divided by a frequency divider circuit 6 consisting of 22 T-type flip-flop stages to produce a 1-second output signal. The output signal from the frequency divider circuit 6 is counted by a counting circuit 8 which produces a binary time signal which is decoded by a signal converting circuit 9. The output of the signal converting circuit 9 is applied to a driver circuit 10 for driving the display device 2 which may consist of light emitting diodes, liquid crystal elements, or electrochromic elements. The watch has a time correcting circuit 7 whose input is produced by the switches 3a, 3b and whose output conditions the counting circuit 8.

Figure 3 shows the basic construction of a static induction transistor logic inverter 31 used in integrated time keeping circuitry of an electronic watch according to the present invention. The operating principle and construction of static induction transistor logic is described in detail in "NIKKEI ELECTRONICS" (Sept. 26, 1977, pages 40 to 45). An aim of the present invention is achieved by applying static induction transistor logic to the integrated time keeping circuitry of an electronic watch since static induction transistor logic has the advantage that its dynamic power consumption is lower than that of other types of integrated circuits so is extremely suitable for use in a high accuracy electronic watch. Static induction transistors were developed as logic elements at the Electric Communication Laboratory of Tohoku University.

The basic construction of the static induction transistor logic inverter 31 will be described in connection with Figures 3 to 6.

Inverters composed of two transistors namely a static induction transistor 42 and a bipolar transistor 41 used as a current source I_1 . The inverter has a substrate 32 of N-type silicon semiconductor material having an impurity concentration of the order of 10^{19} , and a N-type silicon layer 33 having an impurity concentration of the order of 10^{18} grown thereon by a crystal growth technique. Next, a region corresponding to an emitter 34 of the transistor 41 and a collector of the transistor 41 and a region corresponding to a gate 35a, 35b of the static induction transistor 42 are formed from a P-type semiconductor layer having an impurity concentration of the order of about 10^{19} . A region corresponding to a drain 36 of the static induction transistor 42 is formed from a N-type semiconductor layer with an impurity concentration of the order of about 10^9 . Then, metal electrodes of, for example, aluminium, are formed to make the desired electrical connections, and then a protective layer (not shown) such as a layer of a phosphorus-glass is formed over the electrodes. Thus a static induction transistor logic inverter only needs five masking operations during its construction.

When an input terminal 38 of the inverter is grounded, that is a logic 0 signal is applied thereto, the depletion layer between the gate 35 of the static induction transistor 42 and a channel 43 will be caused to spread by the conjunction voltage. In the case where the channel 43 is of N-type semiconductor material with an impurity concentration of the order of about 10^{18} , the thickness of the depletion layer will be $10 \mu\text{m}$ or so. The width of the channel 43, that is, the distance between gates 35a, 35b of the static induction transistor 42 shown in Figure 3, should be such that the depletion layer completely occupies the channel when the terminal 38 is grounded. Thus, since the channel 43 of the static induction transistor 42 constitutes the depletion layer when the terminal 38 of the inverter is grounded, current never flows from the drain 36 of the static induction transistor to the substrate 32 even if the current is injected from an output terminal 39 to the drain. The static induction transistor 42 is thus non-conductive and the output terminal 39 is in the open circuit condition so that the output is a logic 1 signal. At this time, a current I_1 flowing into the gate 35 of the static induction transistor 42 via the transistor 41 flows through the terminal 38 connected to the gate 35 to the substrate which also constitutes the source of the static induction transistor 42.

On the other hand, when the terminal 38 of the inverter is in the open-circuit condition, the current I_1 flows into the gate 35 of the static induction transistor 42 and a potential V_B of the gate 35 rises and approaches a voltage V_A applied to a terminal 37 connected to the emitter of the transistor 41, namely,

$$V_B \approx V_A$$

As a result, since the portion between the gate 35 and the channel 43 of the static induction transistor 42 is biased in the forward direction, the thickness of the depletion layer is decreased, and the channel 43 allows carriers to exist. When current is injected from the output terminal 39 to the drain 36 of the static induction transistor, it flows from the drain to the source constituted by the substrate 32. That is to say, the output becomes a logic 0 signal. From the above explanation, it will be appreciated that a logic 1 signal appears at the terminal 39 when the signal applied to the terminal 38 is a logic 0 signal and a logic 0 signal appears at the terminal 39 when a logic 1 signal is applied to the terminal 38. Thus a static induction transistor logic converter can be represented by the logic diagram shown in Figure 6.

As mentioned before, it is desirable to use, in an electronic watch, integrated time keeping circuitry which can be operated at a relatively high frequency with relatively low dynamic power consumption. The dynamic power consumption of an integrated circuit depends mainly upon the value of its stray capacity which is determined by its structure. This dynamic power consumption P_f is given by the following equation:

$$P_f = C + V_A^2,$$

where C is the value of the stray capacity per stage of the inverter, V_A is the applied voltage, and f is the operating frequency.

In order to show that there is a difference in the value of the dynamic power consumption depending upon the construction of the integrated circuit, the stray capacity in a CMOS-IC, a I^2L -IC and a static induction transistor logic integrated circuit will be calculated.

(i) The stray capacitance in a CMOS-IC is mainly composed of a gate capacity which is inevitable and cannot be removed. Assuming that the size of the gate is $7.5 \mu\text{m} \times 7.5 \mu\text{m}$ and the thickness is $1000 \text{ \AA}$, the value of the stray capacitance is about 0.1 PF .

(ii) The stray capacitance in an I^2L -IC is mainly composed of a conjunction capacitance between the base and the collector of a NPN transistor and a conjunction capacitance between the emitter and the base. Assuming that the impurity concentration of a crystal growth layer which acts as an emitter region of the NPN transistor is 10^{15} , the size of the base is $22.5 \mu\text{m} \times 22.5 \mu\text{m} \times 3 \mu\text{m}$ thickness and the size of the collector therefor is $7.5 \mu\text{m} \times 1 \mu\text{m}$, the stray capacitance will be about 0.05 PF .

(iii) A static induction transistor logic integrated circuit is nearly the same size as an I^2L -IC in plan. Assuming that the size of a gate region is $22.5 \mu\text{m} \times 22.5 \mu\text{m} \times 3 \mu\text{m}$ thickness and the size of a drain region is $7.5 \mu\text{m} \times 7.5 \mu\text{m} \times 1 \mu\text{m}$ in thickness, due to the channel layer having an impurity concentration of 10^{14} , the capacitance will be about 0.005 PF .

TABLE 1

Dynamic Power Consumption

$V_A = 1\text{V}$	C	$P_f(f = 4 \text{ MHz})$
CMOS	0.1 PF	$0.4 \mu\text{W}$
IIL	0.05 PF	$0.2 \mu\text{W}$
SITL	0.005 PF	$0.02 \mu\text{W}$

As seen from Table 1, the dynamic power consumption of a static induction transistor logic inverter is the least of all types of integrated circuit. This is due to the fact that the impurity concentration of the N-type layer forming the channel 43 is lower than that of an I^2L inverter by an order of two. Due to the bipolar operation of the I^2L -IC, it is impossible to reduce the impurity concentration of the crystal growth layer. However, in the case of a static induction transistor logic integrated circuit, the width of the depletion layer of the channel is increased by decreasing the impurity concentration thereof. Consequently, the stray capacitance value of a static induction transistor logic integrated circuit is inevitably smaller than that of an I^2L -IC.

Figure 7 is a graph showing the relationship between voltage and current for the inverter of Figure 3. The curve 1 represents the current-voltage characteristics of the bipolar transistor 41, and the curves 2, 3 represent the current-voltage characteristics of the static induction transistor 42. Since the channel 43 acts as a depletion layer when the input voltage V_B of the inverter is 0 V , in order to cause a drain current I_D to flow, it is necessary to

increase the drain voltage V_C of the static induction transistor 42. In practice, static induction transistor logic is used in the region wherein the drain current I_D is small when the static induction transistor 42 is non-conductive. Since the depletion layer in the channel 43 of the static induction transistor 42 ceases to exist when the input voltage V_B approximately equals the applied voltage V_A , the channel 43 acts as a fixed resistance element having a constant value which depends upon the size and the relative resistance of the channel 43. Thus the value of the current flowing through the channel 43 will be proportional to the value of the voltage V_C of the drain 39.

When the transistor 41 is connected to the static induction transistor 42 which, as mentioned above, acts as a load, the output voltage of the inverter can be changed in dependence upon the input signal to the inverter.

TABLE 2

V_V	V_C	V_D
O_V	$V_x = 0.7V$	$I_x = 0.05 \mu A$
$V_A = 0.7V$	$V_y = 0.1V$	$I_y = 1 \mu A$

Table 2 shows the electronic characteristics of one static induction transistor logic converter. It will be apparent that the voltage of 0.6V can be obtained as a logical output of the inverter.

Figures 8 to 11 illustrate a static induction transistor logic NAND gate which will not be described in detail, its operation being apparent from the previous description.

From the above explanation, it is obvious that a static induction transistor logic integrated circuit which can be operated at a relatively high frequency with relatively low dynamic power consumption can be achieved. Thus an open-drain type inverter or a NAND gate can be easily fabricated by using static induction transistor logic.

Figures 12 and 13 illustrate a crystal oscillator circuit for an electronic watch according to the present invention. The operation of the circuit shown in Figure 12 is the same as that of a CMOS-IC crystal oscillator circuit. The oscillator circuit comprises a main inverter 50 having a static induction transistor 42a, a quartz crystal vibrator 55 having a natural vibration frequency of 4.194304 MHz, resonant capacitors 54a, 54b, a resistor 53 and a static induction transistor 42c, the resistor 53 and the static induction transistor 42c constituting a bias circuit 52 to provide a bias voltage to the inverter 50. Furthermore, the oscillator circuit has an inverter 51 consisting of a static induction transistor 42b used as an output buffer circuit.

Figures 14 and 15 illustrate a frequency divider circuit of an electronic watch according to the present invention consisting of twenty-two T-type flip-flop stages 60a - 60v connected in cascade. Each T-type flip-flop shown in Figure 15 is constructed using static induction transistor logic: Figure 16 is an equivalent circuit diagram.

Figure 17 is a six-advance counting circuit used in an electronic watch according to the present invention. This counting circuit consists of a T-type flip-flop 60w and two D-type flip-flops 70a, 70b.

Figure 18 is a logic diagram of one of the D-type flip-flop stages in Figure 17 and Figure 19 is an equivalent circuit diagram of the D-type flip-flop which is constructed using static induction transistor logic.

(24)

TABLE 3

Count	Display	Decoder In			Decoder Out							
		Q _A	Q _B	Q _C	a	b	c	d	e	f	g	
5	0	0	0	0	1	1	1	1	1	1	1	5
10	1	1	0	0	0	1	1	0	0	0	0	10
	2	0	1	0	1	1	0	1	1	0	1	
	3	0	0	1	1	1	1	1	0	0	1	
15	4	1	0	1	0	1	1	0	0	1	1	15
	5	0	1	1	1	0	1	1	0	1	1	

20 Table 3 is a truth table for a part of a signal converting signal which forms part of an electronic watch according to the present invention and which converts a binary signal from the six-advance counting circuit shown in Figure 17 into a time signal and supplies the time signal to a driving circuit for driving a display device 2.

25 Figure 20 is a logic diagram of the signal converting circuit which can be represented by using the truth table of Table 3.

Figure 21 is an equivalent circuit diagram of the signal converting circuit shown in Figure 20, the signal converting circuit being constructed using static induction transistor logic.

30 Figure 22 (a) is a block diagram illustrating the connection between the integrated time keeping circuitry and a display device 2. In Figure 22 (a) a signal converting circuit 9 has a final stage logic circuit 80 and an interface circuit 81 whose output is connected to a driving circuit 10. Although, in general, applying a voltage of 0.7V to the static induction transistor logic is the most effective way to obtain the optimum operating conditions, the display device 2 if it uses light emitting diodes or liquid crystal elements, requires a voltage of about 3V. Therefore, the interface circuit 81 which includes constant current sources is required to change the voltage of 0.7V powering the static induction transistor logic to 3V to power the display device 2.

35 Figure 22 (b) is a circuit diagram of the circuit shown in Figure 22 (a) which is constructed using static induction transistor logic. A static induction transistor 82a acts as a part 80a of the logic circuit 80, the interface circuit 81 including a static induction transistor 82b. In the interface circuit 81, the current capacity of a current source used as the load of the static induction transistor 82b must be determined in such a way as to correspond to the current capacity of a digit driver static induction transistor 82c in a driving circuit 10a. A driving circuit 10b is used as a segment driver, and in this embodiment includes a lateral bipolar transistor 83a.

40 When the transistor in the logic circuit 80 is non-conductive (that is, it produces a logic 1 signal) the static induction transistor 82b of the interface circuit 81 will become conductive (that is, to produce a logic 0 signal). In turn, the static induction transistor 82c of the digit driver 10a becomes non-conductive and a sufficiently large positive bias is applied to the gate of a static induction transistor 82d of the digit driver 10a, as a result of which, the static induction transistor 82b becomes conductive. Thus, the digit driver 10a is turned on. On the other hand, in the segment driver 10b corresponding to that digit, a logic 0 signal is applied from the interface circuit 81 of the digit driver 10a, as a result of which, the transistor 83a becomes conductive. Therefore, in the case of the circuit shown in Figure 22, when an output terminal 86a of the interface circuit 81 becomes logic "0", a segment f of the display device 2a consisting of light emitting diodes D is lit. When an input terminal 86b of the segment driver 10b becomes logic "1", the segment f is not lit. A resistor 89a in the digit driver 10a may be replaced by a bipolar transistor.

45 Figure 23 is a block diagram showing the driving of a liquid crystal display of an electronic timepiece according to the present invention. Basically, the driving circuit used to drive a liquid crystal display device is the same as that used to drive a display device consisting of light emitting diodes, however, one difference is that, in the case of the liquid crystal display device, the final stages of the driver circuit 10 are complementary circuits and are connected in series. Thus a final logic circuit 80b in the signal converting circuit 90 is an exclusive OR gate 100.

Figure 24 is a logic diagram of an exclusive OR gate and Table 4 is a truth table thereof.

TABLE 4

5	A	B	C	5
	0	0	0	
	1	0	1	
10	0	1	1	10
	1	1	0	

Figure 25 shows an equivalent circuit for an exclusive OR gate using static induction transistor logic.

Figure 26 is a switching circuit for correcting a time indication of an electronic watch. A switching signal is obtained by directly connecting an emitter of a PNP transistor of an inverter using static induction transistor logic to a mechanical switch, e.g. switches 3a, 3b of Figure 2.

A manufacturing process for static induction transistor logic as seen from Figure 3, is the same as that for conventional integrated circuits. In the case of the fabrication of the CMOS-IC, at least seven masks are required for the fabrication. In the case of fabrication of static induction transistor logic, as well as IIL-IC, at least five masks are required. Therefore, the manufacturing process of static induction transistor logic is similar to that of IIL-IC and easier than that of CMOS-IC. However, the dynamic power consumption of static induction transistor logic is lower than that of IIL-IC by at least one order of magnitude. The density of a static induction transistor logic integrated circuit is equal to that of an IIL-IC.

Today, a CMOS-SOS-IC is a well known form of integrated circuit which can be operated at high frequency with less power consumption. However, CMOS-SOS-IC has disadvantages in that it is difficult to decrease leak current (static current consumption) if there is a fault at the junction between the substrate and the silicon layer which is manufactured by a crystal growth technique. The manufacturing process of CMOS-SOS-IC is different from conventional integrated circuits and is more complex compared to conventional integrated circuits and CMOS-SOS-IC is expensive to manufacture. However, if static induction transistor logic is fabricated by using an insulating substrate, such as the SOS, it is possible to reduce the dynamic power consumption further.

In addition, static induction transistor logic may be used together with other types of integrated circuits. Thus static induction transistor logic may be formed on a chip of another type of integrated circuit or on an independent chip. For example, reduced power consumption can be achieved if a CMOS-IC, which can be operated with relatively low static power consumption is used in low frequency (less than 32 KHz) operating conditions and static induction transistor logic, which can be operated with relatively low dynamic power consumption, is used in high frequency (more than 32 KHz) operating conditions. Figure 27 (b) shows an example of an electronic watch according to the present invention with an analog display wherein two types of integrated circuit are involved. A quartz crystal vibrator 55 having a natural vibration frequency of 4 MHz is driven using a static induction transistor logic integrated circuit 118. A signal of 32 KHz is produced by a frequency divider 6b in the integrated circuit 118. The signal of 32 KHz from the integrated circuit 118 is applied to a CMOS-IN 119 including a divider circuit 6d and a driver circuit 10e. An output signal from the integrated circuit 119 is fed to a motor 120 which drives hands 123 of the watch.

In Figure 27 (a) it will be seen that the watch has a casing 121 and a strap 122. In addition, if the driver circuit 10e is made up using static induction transistor logic or bipolar transistors instead of MOS, the area of integrated circuit can be reduced and this is highly advantageous.

Moreover, the driver circuit 10e, when constructed using static induction transistor logic, can be operated with less dynamic power consumption compared to the case where it is a CMOS-IC or an IIL-IC. Moreover, in the case of using CMOS-IC, static power consumption can be reduced but CMOS-IC has the disadvantage of low packing density and low output power.

A driving circuit using static induction transistor logic is suitable for driving a motor or light emitting diode because it has less output resistance compared to bipolar type driving

circuits from which large power can only be easily derived by the enlargement of the area of the circuitry.

WHAT WE CLAIM IS:

1. An electronic timepiece comprising: a time standard; time keeping circuitry controlled by the time standard; and display means for displaying a time indication in response to an output of the time keeping circuitry, the time keeping circuitry including at least one static induction transistor.

2. An electronic timepiece as claimed in claim 1 in which the time standard is a vibrator whose natural frequency of vibration is 1 MHz or greater, said static induction transistor being included in an amplifying circuit.

3. An electronic timepiece as claimed in claim 1 or 2 in which the time keeping circuitry includes a driver circuit for driving the display means, said driver circuit including the or a said static induction transistor.

4. An electronic timepiece as claimed in any preceding claim in which the display means is a digital display means.

5. An electronic timepiece as claimed in any preceding claim in which the or each said static induction transistor is operated in such a manner that its gate current is substantially zero and no drain current flows under conditions of zero bias and a gate current which is smaller than the drain current flows when the static induction transistor is biased in the forward direction.

6. An electronic timepiece as claimed in any preceding claim in which the time keeping circuitry includes a frequency divider circuit having a plurality of flip-flop stages, each of which includes a static induction transistor.

7. An electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.

J. MILLER & CO.
Chartered Patent Agents
Agents for the Applicants
Lincoln House,
296/302 High Holborn,
London WC1V 7JH

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1. An electronic timepiece comprising: a time standard; time keeping circuitry controlled by the time standard; and display means for displaying a time indication in response to an output of the time keeping circuitry, the time keeping circuitry including at least one static induction transistor.
2. An electronic timepiece as claimed in claim 1 in which the time standard is a vibrator whose natural frequency of vibration is 1 MHz or greater, said static induction transistor being included in an amplifying circuit.
3. An electronic timepiece as claimed in claim 1 or 2 in which the time keeping circuitry includes a driver circuit for driving the display means, said driver circuit including the or a said static induction transistor.
4. An electronic timepiece as claimed in any preceding claim in which the display means is a digital display means.
5. An electronic timepiece as claimed in any preceding claim in which the or each said static induction transistor is operated in such a manner that its gate current is substantially zero and no drain current flows under conditions of zero bias and a gate current which is smaller than the drain current flows when the static induction transistor is biased in the forward direction.
6. An electronic timepiece as claimed in any preceding claim in which the time keeping circuitry includes a frequency divider circuit having a plurality of flip-flop stages, each of which includes a static induction transistor.
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J. MILLER & CO.
Chartered Patent Agents
Agents for the Applicants
Lincoln House,
296/302 High Holborn,
London WC1V 7JH