

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Emitter Gated Memory Cell

5 We, FAIRCHILD CAMERA & INSTRUMENT CORPORATION of 300 Robbins Lane, Syosset, Long Island, New York, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —
10 This invention relates to a novel signal storage and processing apparatus, and in particular to a solid state bistable memory device.
15 Presently known data handlers, such as computers, commonly utilize magnetic cores as memory elements, or bits. Also, thin films, electroluminescent-photoconductive assemblies, transfluxors, and other ferroelectric and ferro-magnetic structures have been proposed for use as memory devices in signal storage and processing systems. Generally, each type of memory device is characterized by inherent limitations which tend to restrict the versatility and operation of the systems. For example, in computer systems employing magnetic cores, associated circuitry including buffer stages are needed. Also, core assemblies require a multiplicity of interconnecting electrical windings, adding to space requirements, as well as to the expense of manufacture and maintenance. Thus, new approaches and techniques of signal storage and processing are constantly being sought.

35 Present day technology affords various solid state devices that are useful for different types of circuits. The trend towards miniaturization has led to the development of integrated circuitry and micromodules. One new device that has been developed is the multiple emitter

transistor (MET). MET devices are now commercially available, such as the Fairchild Semiconductor device No. μ C1134 and μ C9996. It is understood, however, that an MET can be made by connecting the bases and collectors of discrete transistors in parallel. Such a device is considered an MET for the purposes of this specification and claims. It would be highly desirable to utilize such a solid state transistor device as a signal storage device for logic circuits and data processing systems.

An object of this invention is to provide a novel and improved means for the storage and processing of signal information.

Another object of this invention is to provide a novel solid state memory device utilizing multi-emitter transistors.

Briefly, the signal storage and processing apparatus of the invention comprises first and second MET's as hereinbefore defined each having at least first, second and third emitter electrodes, a base electrode and a collector electrode; a first source of drive signal having two steady states; viz. a first and second state, coupled to the first emitters of both said MET's; a second source of drive signals having two steady states viz. a first and second state, coupled to the second emitters of both said MET's; a pair of data input signal sources coupled respectively to each of the third emitters of both said MET's; means coupling the base of each MET to the collector of the other MET whereby a storage circuit is formed and a sense output circuit whose inputs are coupled to both said first and second drive signal sources and to the collector of one of the MET's, whereby the sense output circuit is enabled to receive data from said one MET

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when both said first and second drive signals are in the first state.

The invention will be described in greater detail with reference to the drawing in which:

5 FIGURE 1 is a schematic circuit diagram of the storage device, according to this invention;

FIGURES 2A and 2B are schematic circuits of the readout or sensing circuits utilized with the present invention;

10 FIGURE 3 is a logic diagram of the essential elements of the invention;

FIGURE 4 is a schematic diagram representing four memory cells of this invention, connected in a matrix to store separate data bits; and

15 FIGURE 5 is a schematic circuit diagram of an alternative readout circuit, utilizing a plurality of multi-emitter transistors providing an output to a common buffered sense output.

20 Similar numerals refer to similar elements throughout the drawing.

With reference to FIG. 1, the solid state memory element or bistable storage device of this invention comprises a pair of cross-coupled multi-emitter transistors 10 and 12. The transistor pair may be formed by planar epitaxial processes and may constitute an integrated unit. Any number of such units may be joined by the technique of diffusion into a wafer. The MET 10 has three distinct emitter or common electrodes 14, 16, and 18, a base output electrode 20, and a collector or output electrode 22, the electrodes being arranged in NPN fashion. Similarly, the MET 12 has three emitter electrodes 24, 26 and 28, a base 30 and a collector electrode 32, also in an NPN arrangement. The base of the MET 10 is coupled through a resistance 34 to the output electrode or collector 32 of the MET 12; and the base of the MET 12 is coupled through a resistance 36 to the collector 22 of the MET 10. The collectors 22 and 32 are also connected through load resistors 38 and 40 respectively to a source of positive potential 42, which provides collector voltage to the NPN transistors.

Drive signal sources X and Y are coupled respectively to like emitters 18 and 28, and corresponding emitters 16 and 26. The matrix drive signal sources X and Y must be simultaneously in the active state in order for any incoming data signal to be registered in the memory device. The active state is defined as the most positive voltage state of the two allowable binary states. This is generally +1.0 volts or more, with the inactive or binary zero state being near 0.0 volts with a 0.5 volts maximum. If MET's 10 and 12 are fabricated, as illustrated, as NPN transistors, these devices will be in their active state upon application to the base of a positive voltage; if the devices, on the other hand, are PNP polarity, they will be in their active state upon application of a negative voltage.

Throughout this specification, it must be understood that the active states will be reversed from that described if opposite polarity type transistors are employed.

For the purpose of explanation, the state of the storage device shown in Figure 1 is defined by the voltage state of the collector electrode of MET10. The more positive voltage of 1.0 volts or more on the collector electrode of MET10 when MET10 is non-conducting and consequently the less positive voltage of approximately zero on the collector electrode of MET12 when MET12 is conducting, is defined as binary "1". Conversely the less positive voltage of approximately zero on the collector electrode of MET10 when MET10 is conducting and consequently the most positive voltage on the collector electrode of MET12, is defined as binary "0". Thus when the Data 1 signal to the emitter 14 is turned off, so that the emitter 14 is nonconducting, and the Data 0 signal is turned on so that emitter 24 conducts, a binary 1 is stored in the memory device. Conversely, if the Data 0 portion of the device is inactive and the Data 1 portion is energized, a binary 0 is registered.

In operation, the memory cell is accessed for write (or read) by coincident trigger voltages applied to signal sources X and Y. It will be assumed that binary "1" is stored in the device, that is MET10 is non-conducting and MET12 is conducting. If it is now required to store binary "0", Data 1 signal will be turned on and Data "0" signal will be turned off. On the coincident occurrence of the X and Y drive signals therefore, MET10 will start to conduct and the conduction of MET12 will decrease, these effects being enhanced by the coupling circuits between the collector electrodes and base electrodes. The rapid changeover of the device therefore occurs in the well known manner and binary "0" is stored by the conduction of MET10 and the non-conduction of MET12. It will be understood that if binary "1" is stored and a binary "1" signal is applied on the occurrence of the drive signals, there will be no change in the condition of the device and the same applies if both data inputs are in the inactive state on the occurrence of the drive signals. This is the non-destructive read-out feature.

Fig. 2A illustrates a representative sense output circuit that may be utilized in conjunction with the binary storage device of Fig. 1. To achieve readout, the stored signal is applied to the base of the MET 44 through an input terminal 46 and resistor 48. Input terminal 46 of MET 44 is coupled to the collector of MET 12 in Fig. 1. The binary complement or inverted output, collector electrode 32 of MET12 rather than collector electrode 22 of MET10 is used to drive the sense output circuit since the sense output circuit



has an inherent inversion characteristic. Positive potential is applied to the circuit of the collector 50 from a source 52 through a resistor 54. The input terminals marked "X" and "Y" are coupled to both the first and second drive signal sources X and Y. When the X and Y drive signals are coincidentally in their active state as applied to the emitters 54 and 56, then the transistor 44 is properly biased and thus enabled to receive data from MET12 in Fig. 1. The signal is fed from the emitter 58 to the base of the transistor 60, which has its emitter 62 coupled to ground through a bias resistor 64. The readout signal is amplified by a transistor 66 having its base connected to the emitter 62. The signal is channeled from the collector of transistor 66 simultaneously with the data signal that is passed through an emitter 68 of the transistor 44, to a sense output circuit for further processing or display. The circuit including emitter 68 acts as a clamp, and prevents the transistor 66 from saturating. In the network wherein the three transistors 44, 60 and 66 are arranged essentially in a Darlington type circuit, the drive current requirement from the binary storage device is extremely low, such that the sense output circuit functions very well with very low beta transistors. Furthermore, with the inventive circuit, a substantial improvement in noise immunity is realized.

Fig. 2B depicts an alternative embodiment of a readout circuit, which is advantageous in that the circuit presents a load to the binary storage device only when the binary is in the low state; i.e., the low output resistance state of the binary. The circuit of Fig. 2B includes a unidirectional conducting device or diode 70, coupled to a source of potential 72 through a resistor 74. The collector 76 of transistor 78 is also coupled to the source 72 through a resistor 80. A pair of emitters 82 and 84 are tied respectively to the sources of drive signals X and Y for receiving concurrent active signals so that data from the binary storage device may be sensed during the readout process.

When the X and Y drive sources are in the active state, then emitter 86 passes the output signal derived from the binary storage device to transistor 88, which has its emitter 90 coupled to the base of transistor 94 of reference potential. A transistor 94, with its base coupled to the emitter 90, channels the signal to a sense output or readout circuit. Concomitantly, the binary output is conducted through a clamping emitter 96 directly to the readout circuit. Resistor 98 is coupled between the junction of emitter 96 and the readout circuit, and the power supply 72. Both sensing circuits of FIGS. 2A and 2B are characterized by improved noise immunity and low drive requirements from the binary stage.

In FIG. 3, a logic diagram illustrates the operation of the signal storage and readout system including the memory device of FIG.

1 in conjunction with a readout circuit of FIGS. 2A or 2B. To pass either a signal from Data 0 or Data 1 inputs, both X and Y drive signals must be in the active states, corresponding to $XY = \text{logic } 1$. Thus, coincident high triggering voltages applied from the X and Y inputs open the AND gates 100 and 102 to allow either the binary "0" or "1" signal to pass to a latching circuit 104, which is the circuit shown in FIG. 1. If either the X or Y drive source is in the inactive state, then the AND gates 100 and 102 are inhibited, precluding the passage of a signal to the latch 104. The latching circuit 104 stores and holds the binary information bit, which may be retrieved during the readout process.

For readout, the X and Y drives are applied to an AND gate 106 that allows the signal stored in the latch circuit 104 to pass to a sense output.

It should be noted that when the X and Y drive signals are applied to the AND gate 106, Data 1 and Data 0 in the inactive state or logic zeros act to negate the effect of application of drive signals X and Y to the storage input. With both X and Y drives in the active state, hence AND gate 106 enabled, the sense output receives the stored signal for further utilization.

FIG. 4 depicts an arrangement of four interconnected memory devices 107, 108, 109, and 110 in a matrix format, each capable of storing separate bits of information. Each storage device is subject to be activated by its own intersection of X and Y matrix drive lines, when in the active state. Thus, device 107 responds to the X_1 and Y_1 drives, device 108 responds to the X_2 and Y_1 drives and so on. Each of the storage elements is also tied to data input sources D_1 and D_0 to store a binary bit when activated by the X and Y active state signals. The elements may be triggered sequentially by known address systems by activation, for instance, of the X_1 drive line and by successive activation of drive lines Y_1 and Y_2 , or concurrently in parallel, such as in rows or columns, for instance by the simultaneous activation of drive lines X_1 , Y_1 and Y_2 .

FIG. 5 is directed to another sense output circuit affording high speed operation, wherein a sensing threshold voltage is employed. The threshold voltage may be established at any predetermined value by resistances 111 and 112 coupled in series to the collector voltage supply and to the common base circuit of a pair of NPN transistors 113 and 114. These transistors 113 and 114 act as a current source to maintain the current to the output circuit substantially constant.

The sensing circuit includes a diode 116 coupled to an input terminal 118, which receives the stored signal from the binary storage device whenever the X and Y matrix

drive sources are simultaneously in the active state. The X and Y matrix drive sources bias the first two emitters 120 and 122, respectively, of MET 124 so that MET 124 becomes
 5 conducting. With the collector 126 of the MET 124 tied to a suitable voltage source 128 through a load resistance 130, the sensed signal is passed through a third emitter 132 of MET 124 and fed to the emitter 134 of an
 10 output transistor 136. The emitter electrode 134 of transistor 136 is coupled both to a third emitter 132 of MET 124 and to the current source comprising transistors 113 and 114 (via the collector of transistor 113). The third
 15 emitter electrode 132, the base electrode 132a, and the collector electrode 126 of MET 124, together with transistor 136 comprise a differential current switch. The output signal may be channeled to a sense output or to a utilization
 20 circuit, which may be a readout display for example. Terminal 138 may be used to connect any number of multi-emitter transistor circuits 124a—n to respective binary storage devices n_1 — n_n for readout through a common
 25 differential current switch comprising transistor 136 and the current source (transistors 113 and 114).

The solid state memory element and read-out apparatus of this invention affords non-destructive readout, high speed and high level
 30 output signals. Increased packing density at low cost is made possible and associated circuitry is relatively simple and inexpensive. While the specific embodiment chooses for the above detailed description of the invention and
 35 drawings described a three emitter MET as used in a two dimensional matrix, one skilled in the art will appreciate that matrices having more than two dimensions may be employed. In such matrices MET's having more than
 40 three emitters are used.

WHAT WE CLAIM IS:—

1. A signal storage and processing apparatus comprising:
 45 first and second MET's as hereinbefore defined each having at least first, second and third emitter electrodes, a base electrode, and collector electrode;
 a first source of drive signal having two
 50 steady states, viz. a first and a second state, coupled to the first emitters of both said MET's;
 a second source of drive signal having two
 steady states, viz. a first and a second state
 55 coupled to the second emitters of both said MET's;
 a pair of data input signal sources coupled respectively to each of the third emitters of both said MET's;

means coupling the base of each MET to the collector of the other MET whereby a storage circuit is formed; and

a sense output circuit whose inputs are coupled to both said first and second drive signals and to the collector of one of said MET's, whereby said sense output circuit is enabled to receive data from said one MET when both said first and second drive signals are in the first state.

2. The signal storage and processing apparatus of claim 1 further characterized by said sense output circuit having a third MET having first, second and third emitter electrodes, a base electrode and a collector electrode, said third MET being coupled to one of said first and second MET's, and two of said emitters of said third MET being respectively coupled to said first and second sources of drive signals.

3. The signal storage and processing apparatus of claim 2 further characterized by said third MET being coupled through its base electrode to one of said first and second MET's.

4. The signal storage and processing apparatus of claim 3 further characterized by said sense output circuit including an additional transistor having emitter, base and collector electrodes said emitter electrode of said transistor being coupled to a third emitter electrode of said third MET, and a current source coupled to said emitter of said transistor and to said third emitter of said third MET whereby said third emitter electrode, said base electrode, and said collector electrode of said third MET, together with said transistor comprise a differential current switch.

5. The signal storage and processing apparatus of claim 4 further characterized by an input terminal means coupled between said third emitter of said third MET and said emitter of said transistor, said input terminal means being adapted to connect said transistor and said current source to additional MET's receiving other input signals, whereby the same transistor and current source serve as part of a differential current switch for a plurality of emitter electrodes from different MET's.

6. A signal storage and processing apparatus substantially as described with reference to the accompanying drawings.

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drive sources are simultaneously in the active state. The X and Y matrix drive sources bias the first two emitters 120 and 122, respectively, of MET 124 so that MET 124 becomes conducting. With the collector 126 of the MET 124 tied to a suitable voltage source 128 through a load resistance 130, the sensed signal is passed through a third emitter 132 of MET 124 and fed to the emitter 134 of an output transistor 136. The emitter electrode 134 of transistor 136 is coupled both to a third emitter 132 of MET 124 and to the current source comprising transistors 113 and 114 (via the collector of transistor 113). The third emitter electrode 132, the base electrode 132a, and the collector electrode 126 of MET 124, together with transistor 136 comprise a differential current switch. The output signal may be channeled to a sense output or to a utilization circuit, which may be a readout display for example. Terminal 138 may be used to connect any number of multi-emitter transistor circuits 124a—n to respective binary storage devices n_1 — n_n for readout through a common differential current switch comprising transistor 136 and the current source (transistors 113 and 114).

The solid state memory element and readout apparatus of this invention affords non-destructive readout, high speed and high level output signals. Increased packing density at low cost is made possible and associated circuitry is relatively simple and inexpensive. While the specific embodiment chooses for the above detailed description of the invention and drawings described a three emitter MET as used in a two dimensional matrix, one skilled in the art will appreciate that matrices having more than two dimensions may be employed. In such matrices MET's having more than three emitters are used.

WHAT WE CLAIM IS:—

1. A signal storage and processing apparatus comprising:
 - first and second MET's as hereinbefore defined each having at least first, second and third emitter electrodes, a base electrode, and collector electrode;
 - a first source of drive signal having two steady states, viz. a first and a second state, coupled to the first emitters of both said MET's;
 - a second source of drive signal having two steady states, viz. a first and a second state coupled to the second emitters of both said MET's;
 - a pair of data input signal sources coupled respectively to each of the third emitters of both said MET's;

means coupling the base of each MET to the collector of the other MET whereby a storage circuit is formed; and

a sense output circuit whose inputs are coupled to both said first and second drive signals and to the collector of one of said MET's, whereby said sense output circuit is enabled to receive data from said one MET when both said first and second drive signals are in the first state.

2. The signal storage and processing apparatus of claim 1 further characterized by said sense output circuit having a third MET having first, second and third emitter electrodes, a base electrode and a collector electrode, said third MET being coupled to one of said first and second MET's, and two of said emitters of said third MET being respectively coupled to said first and second sources of drive signals.

3. The signal storage and processing apparatus of claim 2 further characterized by said third MET being coupled through its base electrode to one of said first and second MET's.

4. The signal storage and processing apparatus of claim 3 further characterized by said sense output circuit including an additional transistor having emitter, base and collector electrodes said emitter electrode of said transistor being coupled to a third emitter electrode of said third MET, and a current source coupled to said emitter of said transistor and to said third emitter of said third MET whereby said third emitter electrode, said base electrode, and said collector electrode of said third MET, together with said transistor comprise a differential current switch.

5. The signal storage and processing apparatus of claim 4 further characterized by an input terminal means coupled between said third emitter of said third MET and said emitter of said transistor, said input terminal means being adapted to connect said transistor and said current source to additional MET's receiving other input signals, whereby the same transistor and current source serve as part of a differential current switch for a plurality of emitter electrodes from different MET's.

6. A signal storage and processing apparatus substantially as described with reference to the accompanying drawings.

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