

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Semiconductor Device Fabrication

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare this invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor structures. More particularly it relates to the use of etching techniques in the formation of such structures and the fabrication of semiconductor devices in isolated bodies of semiconductor material.

According to the present invention a method of fabricating a semiconductor structure includes the steps of forming a layer of etch resistant material intermediate a first portion and a second portion of a body of semiconductor material, and etching the first portion of the body with an etchant which does not attack the etch-resistant material to any appreciable degree to remove substantially all of the first portion while leaving the etch resistant layer and the second portion of the body substantially unaffected.

More usually, a plurality of discrete second portions of semiconductor materials are attached to but separated from the said first portion by a continuous layer of etch resistant electrically isolating material and the etching step leaves the second portions attached to the etch resistant layer. The discrete second portions can be formed by forming a plurality of mesas at a surface of a member of semiconductor material, the etch resistant material being formed to cover the mesas and a layer of semiconductor material being deposited on the etch resistant material to form the said first portion

of the body. Semiconductor material of the said member is removed to leave the mesas separated from each other thereby forming the second portions.

In a particular embodiment, the first portion of the body is composed of polycrystalline semiconductor material and the or each second portion of monocrystalline semiconductor material. Preferably the etch resistant layer is composed of silicon carbide.

As the miniaturization of electronic circuits has evolved, it has been realized that one of the greatest potentials in microelectronics due to the greater reliability in performance and substantial savings in cost and space is being offered by a method whereby individual components such as transistors, resistors, diodes, etc. are formed within a single piece of semiconductor material, preferably single crystal, the components being interconnected to perform the desired circuit function. The resulting structure is referred to as an integrated network.

The formation of all components in one single crystal semiconductor substrate, however, presents the problem of electrically isolating the circuit components from one another. In particular, when a number of transistors and resistors are formed within one portion of the substrate, with the substrate forming the collector region of each of the transistors, it is necessary for many circuit applications to isolate the transistors from each other to avoid the collectors from being commoned; and to isolate the transistors from the resistors. Many techniques have been developed to accomplish this isolation, all of them possessing certain disadvantages.

The specification of copending application No. 43149/66 (Serial No. 1151848) discloses a novel thermal print head utilizing

[Price 4s. 6d.]

integrated network techniques whereby a matrix of individual printing elements is formed on an insulating, e.g. ceramic, substrate. The successful operation of these individual mesa printing elements depends largely upon a fabrication technique which substantially thermally isolates the elements from each other.

The present invention also provides a method of fabricating a semiconductor network comprising formation of circuit components in pockets of monocrystalline semiconductor material in a surface of a support body of semiconductor material (suitably polycrystalline material) with a layer of etch resistant, electrically isolating material (e.g. silicon carbide) intermediate the pockets and the body. Interconnections are formed between the circuit components, the interconnections overlying and adjacent the said surface of the support body. The entire structure thus formed is mounted upon an insulating, e.g. ceramic, substrate face-down with the interconnections in juxtaposition to and making ohmic contact with desired ones of electrical leads on a surface of the substrate. All of the support body is then etched away with an etchant which does not attack the etch resistant material to any appreciable degree, whereby each of the individual interconnected circuit components remain mounted in mesas upon the substrate, electrically isolated from each other by the etch resistant, electrically isolating layer and the surrounding ambient.

In use of this method to form a matrix of thermal printing elements, interconnected diode-resistor pairs are formed within the mesas. The removal of the support body, in addition to providing electrical isolation of the diode-resistor pairs from each other, provides substantial thermal isolation between the mesa printing elements. For this application, it is preferable that the circuit components be formed adjacent the mesa surfaces next to the substrate whilst being spaced from the opposite surfaces of the mesas covered by the etch resistant material.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings, in which

FIGURE 1 is a pictorial view in section of semiconductor wafer in an early stage of production of an integrated network embodying the present invention.

FIGURE 2 is a front elevation of one form of apparatus used in carrying out a process embodying the present invention;

FIGURES 3 and 4 are elevational views in section of the semiconductor body of FIGURE 1 in successive stages of production;

FIGURE 5 is a pictorial view of the lower side of the semiconductor body of FIGURE 4 after the body has been inverted;

FIGURE 6 is a sectional view of a portion of the wafer of FIGURE 5 taken along the line 6-6, showing a subsequent step of the process of this invention;

FIGURE 7 is the same sectional view as FIGURE 6 after diffusion operations have been completed and interconnections have been applied;

FIGURE 8 is a pictorial view of the device described with reference to FIGURES 1-7;

FIGURE 9 is a pictorial view of the device shown in FIGURE 8 after the device has been mounted face down upon an insulating substrate having external expanded leads thereupon;

FIGURE 10 is a pictorial view of the structure shown in FIGURE 9 after the polycrystalline material has been removed, the components isolated from each other by the silicon carbide layer and the surrounding ambient;

FIGURE 11 is a sectional view of a portion of the structure shown in FIGURE 10 taken along the section line 11-11;

FIGURE 12 is a schematic diagram of the integrated circuit contained within the device of FIGURE 10;

FIGURE 13 is a top view of a thermal print head, showing an array or matrix of mesa heating elements with selected elements energized to define the numerical digits "1", "2", "3", "4", and "5".

FIGURE 14 is an underside view of a portion of the array shown in FIGURE 13, illustrating the formation of diode-resistor pairs within each mesa element, and the lead and expanded interconnection pattern between elements; and

FIGURES 15-18 are sectional views of a portion of the heating elements shown in FIGURE 14, taken along the section line 15-15, and depicting subsequent steps in the fabrication of the print head.

Referring now to FIGURE 1, there is described the first step in one embodiment of this invention. A slice of low resistivity N+ single crystal semiconductor material, such as silicon is used as the starting material. The slice may be about one inch in diameter and ten mils thick. A small segment of the slice may be represented as a chip or wafer 10, this segment representing the space to be occupied by one integrated circuit. The top surface of the slice is first masked and etched to form a pattern of raised mesas, for example 11-15. The masking may be by a material such as wax, or preferably by conventional photoresist techniques which permit excellent geometry control. The height of the mesas 11-15, or, in other words, the depth of the etching, may be about two mils. At this point the top surface of the slice is covered with a coating 16 of high resistivity silicon carbide which

may be formed by any conventional technique to a thickness of perhaps 0.5 mil or more.

One method of depositing the silicon carbide is described with reference to FIGURE 2. Apparatus for depositing the silicon carbide in accordance with the process comprises a reactor in the form of a tube furnace 20 having heating coils 21. The furnace may be of a horizontal or vertical type, may be suited for single or multiple slices, and may be either resistively or inductively heated. Silicon wafers, including the wafer 10, are disposed within the furnace in such a position as to expose the slices to gases directed into the tube through a conduit 23. Toluene (C_7H_8) and silicon tetrachloride ($SiCl_4$) vapors are respectively introduced into the conduit 23 from cylinders containing liquid toluene and liquid silicon tetrachloride, through which hydrogen gas is bubbled. Purified dried hydrogen enters end 22 of the conduit. The flow of the gases into the tube furnace 20 is regulated by conventional valves.

The rate of deposition is determined largely by the temperature at which the reactor is maintained, the flow rate through the conduit 23, and the percentage composition of the constituents. For example, when the flow rate was kept at approximately 10 liters/minute, the temperature at approximately $1080^\circ C$, and the reactive mixture consisted of 0.87 mol percent $SiCl_4$, 0.18 mol percent C_7H_8 , and the remaining mol percent H_2 , a layer of silicon carbide was deposited upon the wafer 10 as seen in FIGURE 1 at a rate of approximately one micron/minute.

A layer 28 of material, for example polycrystalline semiconductor material, is now deposited over the top surface of the slice 10, as seen in FIGURE 3. The most common method of deposition is by the hydrogen reduction of silicon tetrachloride, a technique well known in the art and requiring no elaboration here. The conductivity-type of the layer 28 is not critical as it may be N-type, P-type, or intrinsic, and the thickness of the layer should be perhaps seven or eight mils or more to facilitate handling the unit without breakage. The layer may also be either monocrystalline or amorphous.

As the next step in the process of this invention, the structure of FIGURE 3 is subjected to a lapping and polishing treatment on its lower face to remove all of the original silicon material except that portion remaining within the mesas 11-15, as illustrated in FIGURE 4, the lower portions of the silicon carbide layer 16 serving as a substantially continuous "stop" to the lapping and polishing operation.

Inverting the device and looking at what was the bottom surface of face 32 of FIGURE 4, but will now be considered

the top face of the unit, the structure will appear as in FIGURE 5. Each of the low resistivity N+ monocrystalline portions or pockets 11-15 is insulated from the others and from the substrate of layer 28 by the silicon carbide coating 16. This coating 16 is not shown to scale in the drawings, and would actually be perhaps an order of magnitude thinner in proportion than is shown in the sectional view of the drawings.

The low resistivity portions 11-15 are then selectively masked and, using a vapor etch and epitaxial redeposition process, select portions of the N+ low resistivity material are removed and replaced by high resistivity semiconducting material. The resulting structure is shown with respect to two of the regions in FIGURE 6 wherein high resistivity N-type regions 30 and 31 are formed adjacent the low resistivity N+ regions 12 and 14 respectively.

The regions 30 and 31 now serve as regions into which subsequent diffusions, or upon which epitaxial depositions, may be made in order to fabricate various components of an integrated circuit. Referring now to FIGURE 7, a sectional view of a portion of a completed integrated circuit is seen, with an NPN transistor T_1 and a resistor R_1 having been formed by diffusion in the N-type redeposited regions 30 and 31. A P-type diffused region provides the base of the transistor, while an elongated P-type region formed simultaneously with the base provides the resistor R_1 . An N-type diffused region 58 provides the transistor T_1 emitter. The diffusion operations utilize conventional silicon oxide masking so that an oxide layer 42 acquires a stepped configuration in the final device. Openings are made in the oxide where contact is necessary, then metal film is deposited over the oxide and selectively removed to provide the desired contacts, interconnections and bonding pads.

The resulting structure or device 10 is shown in FIGURE 8 with the transistors T_1 and T_2 and the resistors R_1 , R_2 , and R_3 along with the metal film interconnections providing a logic circuit. Bonding pads 50-54 are provided to allow interconnection with the metallized lead pattern on insulating substrate upon which the device 10 is to be subsequently mounted.

In accordance with this latter objective, the device 10, with the individual interconnected circuit components, is inverted and mounted upon an insulating substrate 55 for example ceramic, in the manner depicted in FIGURE 9 so that the polycrystalline layer 28 forms the top surface of the device. The substrate 55 has a series of expanded leads (not shown) deposited in a conventional manner upon its upper face, the leads terminating in bonding pads in, and, out, V+ (shown in FIGURE 9) for external

connections (input terminals, ground, etc.). The device 10 is then oriented upon the substrate 55 so that the bonding pads 50-54 shown in FIGURE 8 are in contact with the respective expanded leads upon the substrate 55. Through a conventional technique, such as soldering, the bonding pads and the leads are then physically joined to make electrical connection, while the entire structure itself is cemented to the ceramic substrate 55 by a suitable adhesive, as epoxy.

As the next step in the process, the polycrystalline semiconductor material 28 is completely removed from the top surface of the device 10 resulting in the structure shown in FIGURE 10 (and partially in section in FIGURE 11), whereby each of the individual interconnected circuit components are mounted upon the ceramic substrate 55 within mesas isolated from each other by the high resistivity layer of silicon carbide and the surrounding ambient (air for example). This removal is accomplished by applying an etchant, such as a mixture of hydrofluoric acid (2 parts per volume), nitric acid (15 parts per volume), and acetic acid (5 parts per volume), to the top surface of the device, whereby all of the polycrystalline material 28 is etched away, while the individual components are protected from the etchant by the layer 16 of silicon carbide which acts as an etch barrier. Without the presence of the etch resistant silicon carbide layer 16, the individual components within the mesas would be destroyed. The expanded leads on the substrate 55 are protected from the etching step either by forming a protective wax coating over the leads or by using an etchant that will not attack the metal.

FIGURE 11 is a sectional view of a portion of the device of FIGURE 10 showing the interconnected components R_1 and T_1 mounted upon the insulating substrate 55 with the epoxy layers 56. FIGURE 12 shows the schematic form of the logic circuit illustrated in FIGURE 10.

There is now described with reference to FIGURES 13-18 the fabrication of a thermal print head of the type described and claimed in the specification of copending patent application, No. 43149/66 (Serial No. 1151848), whereby an etch-resistant layer, as silicon carbide, provides an "etch barrier".

Referring now to FIGURE 13, there is depicted a top view of the thermal print head 1 comprising a wafer 110 of semiconductor material, silicon for example, having five "characters" 111-115 formed therein. Each of the characters is composed of a matrix or array of thermal printing elements such as the elements 121-125 of the character 111. Each element is a raised mesa of semiconductor material with a layer of silicon carbide 160 over the top of the mesas and the rest of the slice 10 (the fabri-

cation of which will be subsequently described with reference to FIGURES 15-18), each mesa containing an interconnected diode and resistor. The particular array of the dimensions of the characters are not critical. In the particular embodiment herein shown and described, however, each character is composed of a 5 x 5 array of printing elements, each of the printing elements, 121-125 for example, being approximately 0.016 inch in length and 0.012 inch in width, the spacing between each element being approximately 0.004 inch. The silicon bar 110 may be approximately 0.3 inch in width by 0.5 inch in length and having a thickness of 0.001 inch. The active printing surface (in other words, the "characters" and their spacing) occupies an area of approximately 0.1 inch by 0.5 inch, and is centrally located upon the wafer 110.

The silicon wafer 110 with the mesas therein is mounted upon a ceramic substrate 120 so that the metallized leads 130-132, for example, formed upon the sides of the substrate 120 interconnect with the expanded leads 130a-132a, respectively, located on the underside of the excess material of the wafer 10. These expanded leads, as well as the other expanded leads, are actually extensions of the second level interconnections which make contact to the various first level interconnections of the printing elements shown in FIGURE 14. The metallized leads 130-132 may be formed directly upon the surface of the ceramic substrate 120, or may be formed within slots within the ceramic. The joining of the expanded leads 130a-132a to the external metallized leads 130-132 may be accomplished by any conventional technique as, for example, by flow solder fillets. An epoxy may then be placed under the overhanging portions of the silicon slice to provide added mechanical support.

The actual operation of the thermal printer may be accomplished by various techniques and is not restricted to any one method of excitation of the appropriate heating elements. For example, a short high power pulse may be applied to selected external leads, such as 130-132, the pulse causing current to flow through resistors of select printing elements, the selected printing elements heating up to say 300°C in a pattern corresponding to the letters or numbers to be printed. The selection of the proper leads to be energized may be accomplished manually or by a separate diode digital decoder, for example. Accordingly, as shown in FIGURE 13, select elements of the "characters" 111-115 may be heated to define the numerical digits "1", "2", "3", "4", and "5", respectively, which then are printed on heat sensitive paper which has been indexed over the face of the thermal

print head 1. (The select elements which have been heated are represented on FIGURE 13 by a double cross-hatching, and may be best seen by holding the drawing at arms length from the eye.) The printing may be accomplished, for example, by simultaneously heating select elements of "characters" 111-115, thereby printing a whole line at a time, or by heating the select elements of the characters in a manner so as to sequentially print out the numerical digits "1" to "5".

Referring now to FIGURE 14, there is depicted an underside plan view of a portion of one of the characters 111, showing some of its heating elements 140, 141, 142, and 143 and a typical, but not restrictive, pattern of interconnections. Each of the heating elements comprises a raised mesa of the semiconductor material (as observed in the cross-sectional view of FIGURES 15-18), a diode and resistor pair such as D_{140} and R_{140} , being formed by conventional masking and diffusion techniques, for example, in the base of the mesa, the pair being interconnected with each other and with the rest of the system. The function of the resistors R_{140} , R_{141} , R_{142} , and R_{143} is to provide the source of heat for each printing element, and the function of the diodes D_{140} , D_{141} , D_{142} , and D_{143} is to limit the current flow through only those resistors which are to be heated. First level interconnectors such as 150 and 151 ohmically connect the P-type regions of the diodes D_{140} and D_{141} and the P-type regions of diodes D_{142} and D_{143} to the second level interconnector 175 respectively, and first level interconnectors 152, 153, and 154 connect the ends of the resistor R_{140} and to other resistors of other mesas (not shown in FIGURE 14) to the second level interconnectors 130a, 131a, and 132a, respectively.

With reference to the cross-sectional views of FIGURES 15-18 there is now described the fabrication of the novel print head of this invention, particularly the formation of the silicon mesa thermal printing elements. Single crystal semiconductor material, such as silicon, is used as the starting material for a slice 110. A portion of this slice is shown in FIGURE 15. The top surface of the slice is first masked and etched to form a pattern of raised mesas such as 140, 141, and 145. The masking may be by a material such as wax or preferably by photoresist techniques which permit excellent geometry control. The height of the mesas 140, 141, and 145, for example, or in other words, the depth of the etching may be approximately 1.5 to 2 mils. After the mesas are formed, the top surface of the slice is covered with a coating 160 of silicon carbide which may be formed by the technique previously

described with reference to FIGURE 2, to a thickness of perhaps 0.3 to 0.8 mil.

A layer 161 of material, for example polycrystalline semiconductor material, is now deposited over the top surface of the slice 110 adjacent the silicon carbide layer 160, as seen in FIGURE 15 in the same manner as previously described. As the next step in the fabrication of the thermal printing head, the structure of FIGURE 15 is subjected to a lapping and polishing treatment on its lower face to remove all the original silicon material except that portion remaining within the mesas 140, 141, and 145, as illustrated in FIGURE 16.

Inverting the structure and looking at what was the bottom surface of face 162 of FIGURE 16, but what will now be considered the top face of the unit, the structure appears as in FIGURE 17. The mesa regions 140 and 141 now serve as regions into which subsequent diffusions, or upon which epitaxial depositions, may be made in order to fabricate the diode-resistor pair of each printing element. In this particular embodiment, the diode-resistor pair D_{140} and R_{140} and D_{141} and R_{141} are formed by conventional oxide masking and diffusion operations in the N-type material of mesa elements 140 and 141, respectively.

P-type diffused regions 163a and 163b provide the respective anodes of the diodes D_{140} and D_{141} , while elongated P-type regions 164a and 164b, formed simultaneously with the anode regions, provide the resistors R_{140} and R_{141} . The N-type material of the mesas 140 and 141 provide the cathodes of the diodes D_{140} and D_{141} . Contact to the N regions are made through low resistivity N+ regions as shown. The diffusion operations utilize silicon oxide masking as mentioned so that an oxide layer 165 is formed which acquires a stepped configuration in the final device. Openings are made in the oxide where contact is necessary, then metal film is deposited over the oxide and selectively removed to provide the desired contacts and interconnections.

It is to be observed that the silicon mesa 145 is masked with a region 165a of the silicon oxide layer 165 during the formation of the diodes and resistors in the various printing elements. This region 165a provides the spacing between the individual "characters" as shown in FIGURES 13 and 14. The second level interconnections 130a, 131a, and 132a, for example, are formed over the regions 165a between the characters rather than over the printing elements in order to prevent exposure of insulation between leads to the high temperature thermal transients associated with the thermal printing elements. An insulating layer 166 formed of silicon dioxide, for example, and capable

of withstanding high temperatures is formed by conventional techniques intermediate the first level interconnections and the second level interconnections 130a and 130b, as shown in FIGURE 17.

As the final steps in the fabrication of the thermal print head, the composite structure with the individual printing elements is sawn into the individual wafers and inverted and mounted upon ceramic substrate 120 with a suitable adhesive 168, such as epoxy, as shown in FIGURE 18. The wafer with the mesa printing elements is aligned so that the second level interconnections 130a, 131a, and 132a, for example, engage the appropriate metallized lead pattern on the ceramic substrate, as shown in FIGURE 13, the joining of the metal being accomplished by soldering. As the next step in the process, the polycrystalline semiconductor layer 161 is completely removed, resulting in a structure shown in FIGURE 18, whereby each of the mesa thermal printing elements 140 and 141, for example, are isolated from each other by the layer 160 of silicon carbide and the surrounding ambient (air, for example). This removal is accomplished by applying an etchant such as a mixture of hydrofluoric acid (2 parts per volume), nitric acid (15 parts per volume) and acetic acid (5 parts per volume) to the top surface, whereby all of the polycrystalline material 161 is etched away, while the semiconductor material within the individual mesas is protected from the etchant by the layer 160 of silicon carbide acting as an etch barrier.

As a result of the above described process, a matrix of mesa printing elements, such as 140 and 141, is produced, the complete structure providing numerous advantages. As seen in FIGURE 18, the diode-resistor pair of each element is positioned away from the surface over which the thermally sensitive paper passes, the silicon material within the mesas and the silicon carbide coating 160 providing the protection for these components. The final structure, even without the silicon carbide, will offer considerable wear resistance, the silicon material itself affording substantial protection from the abrasive action of the thermal sensitive paper. The presence of the silicon carbide layer 160, however, affords much greater protection for both the components and the overlying silicon material. In addition, since the interconnections are also formed away from the upper surface, they will be protected, providing greater reliability.

The removal of the polycrystalline material between each mesa, the silicon carbide acting as an "etch barrier", resulting in the gaps between each printing element, provides substantial thermal isolation between each of the printing elements, thereby reducing heat "spillovers" into the adjacent

elements and keeping the quantity of power required to heat each element at a minimum.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention is defined by the appended claims.

WHAT WE CLAIM IS:

1. A method of fabricating a semiconductor structure including the steps of forming a layer of etch resistant material intermediate a first portion and a second portion of a body of semiconductor material, and etching the first portion of the body with an etchant which does not attack the etch resistant material to any appreciable degree to remove substantially all of the first portion while leaving the etch resistant layer and the second portion of the body substantially unaffected.

2. A method according to Claim 1, in which a plurality of discrete second portions of semiconductor material are attached to but separated from the said first portion by a continuous layer of etch resistant electrically isolating material, the etching step leaving the second portions of semiconductor material attached to the etch resistant material.

3. A method according to Claim 2, in which a member of semiconductor material has a plurality of mesas formed on a surface thereof and the layer of etch resistant material is formed to cover the mesas, in which a layer of semiconductor material is formed over the etch resistant material to overlie the mesas and form the said first portion of the said body, and semiconductor material of the said member is removed to leave the mesas separated from each other thereby forming the said second portions.

4. A method according to Claim 3, in which the said mesas are formed by etching a surface of the said member.

5. A method according to any one of the preceding claims, in which the said first portion is composed of polycrystalline semiconductor material and the or each second portion is composed of monocrystalline semiconductor material.

6. A method of fabricating a semiconductor network comprising forming pockets of monocrystalline semiconductor material in a surface of a support body of semiconductor material with a layer of etch resistant electrically isolating material separating the pockets from the support body, forming circuit components in the respective pockets and forming interconnections be-



of withstanding high temperatures is formed by conventional techniques intermediate the first level interconnections and the second level interconnections 130a and 130b, as shown in FIGURE 17.

As the final steps in the fabrication of the thermal print head, the composite structure with the individual printing elements is sawn into the individual wafers and inverted and mounted upon ceramic substrate 120 with a suitable adhesive 168, such as epoxy, as shown in FIGURE 18. The wafer with the mesa printing elements is aligned so that the second level interconnections 130a, 131a, and 132a, for example, engage the appropriate metallized lead pattern on the ceramic substrate, as shown in FIGURE 13, the joining of the metal being accomplished by soldering. As the next step in the process, the polycrystalline semiconductor layer 161 is completely removed, resulting in a structure shown in FIGURE 18, whereby each of the mesa thermal printing elements 140 and 141, for example, are isolated from each other by the layer 160 of silicon carbide and the surrounding ambient (air, for example). This removal is accomplished by applying an etchant such as a mixture of hydrofluoric acid (2 parts per volume), nitric acid (15 parts per volume) and acetic acid (5 parts per volume) to the top surface, whereby all of the polycrystalline material 161 is etched away, while the semiconductor material within the individual mesas is protected from the etchant by the layer 160 of silicon carbide acting as an etch barrier.

As a result of the above described process, a matrix of mesa printing elements, such as 140 and 141, is produced, the complete structure providing numerous advantages. As seen in FIGURE 18, the diode-resistor pair of each element is positioned away from the surface over which the thermally sensitive paper passes, the silicon material within the mesas and the silicon carbide coating 160 providing the protection for these components. The final structure, even without the silicon carbide, will offer considerable wear resistance, the silicon material itself affording substantial protection from the abrasive action of the thermal sensitive paper. The presence of the silicon carbide layer 160, however, affords much greater protection for both the components and the overlying silicon material. In addition, since the interconnections are also formed away from the upper surface, they will be protected, providing greater reliability.

The removal of the polycrystalline material between each mesa, the silicon carbide acting as an "etch barrier", resulting in the gaps between each printing element, provides substantial thermal isolation between each of the printing elements, thereby reducing heat "spillovers" into the adjacent

elements and keeping the quantity of power required to heat each element at a minimum.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention is defined by the appended claims.

WHAT WE CLAIM IS:

1. A method of fabricating a semiconductor structure including the steps of forming a layer of etch resistant material intermediate a first portion and a second portion of a body of semiconductor material, and etching the first portion of the body with an etchant which does not attack the etch resistant material to any appreciable degree to remove substantially all of the first portion while leaving the etch resistant layer and the second portion of the body substantially unaffected.

2. A method according to Claim 1, in which a plurality of discrete second portions of semiconductor material are attached to but separated from the said first portion by a continuous layer of etch resistant electrically isolating material, the etching step leaving the second portions of semiconductor material attached to the etch resistant material.

3. A method according to Claim 2, in which a member of semiconductor material has a plurality of mesas formed on a surface thereof and the layer of etch resistant material is formed to cover the mesas, in which a layer of semiconductor material is formed over the etch resistant material to overlie the mesas and form the said first portion of the said body, and semiconductor material of the said member is removed to leave the mesas separated from each other thereby forming the said second portions.

4. A method according to Claim 3, in which the said mesas are formed by etching a surface of the said member.

5. A method according to any one of the preceding claims, in which the said first portion is composed of polycrystalline semiconductor material and the or each second portion is composed of monocrystalline semiconductor material.

6. A method of fabricating a semiconductor network comprising forming pockets of monocrystalline semiconductor material in a surface of a support body of semiconductor material with a layer of etch resistant electrically isolating material separating the pockets from the support body, forming circuit components in the respective pockets and forming interconnections be-



tween the circuit components, the interconnections overlying and adjacent the said surface of the support body, mounting the body so formed on an electrically insulating substrate with the said interconnections in juxtaposition to and making ohmic contact with desired ones of electrical leads formed on a surface of the substrate, and then etching away all of the support body with an etchant which does not attack the etch resistant material to any appreciable degree to leave mesas containing the components mounted on the substrate and covered by the etch resistant, electrically isolating material.

7. A method according to Claim 6, in which the components are formed to lie adjacent the mesa surfaces next to the substrate and spaced from the opposite surfaces of the mesas covered by etch resistant material.

8. A method according to Claim 6 or Claim 7, at least one mesa containing an active circuit component and at least one mesa containing a passive component.

9. A method according to Claim 6 or Claim 7, at least one mesa containing an

active component and a passive component.

10. A method according to any one of the preceding claims, the etch resistant material being silicon carbide.

11. A method according to any one of the preceding claims, the semiconductor material being silicon.

12. A method of fabricating an integrated semiconductor network substantially as described herein with reference to and as illustrated by Figs. 1 and 3-12 in conjunction with Fig. 2 of the accompanying drawings.

13. A method of fabricating a semiconductor structure substantially as described herein with reference to and as illustrated by Figures 13-18 in conjunction with Figure 2 of the accompanying drawings.

14. A semiconductor structure manufactured by a process according to any one of Claims 1-12.

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