~~What is claimed is:~~

1. A method of manufacture of an integrated circuit system comprising:

forming an etch stop layer over a bulk substrate;

forming a buffer layer on the etch stop layer;

forming a hard mask on the buffer layer;

forming a through silicon via through the etch stop layer with the hard mask detected and the buffer layer removed with a low down force; and

forming a passivation layer on the through silicon via and the etch stop layer.

2. The method as claimed in claim 1 wherein forming the through silicon via includes forming the through silicon via coplanar with the etch stop layer.

3. The method as claimed in claim 1 wherein forming the through silicon via includes forming the through silicon via in the bulk substrate.

4. The method as claimed in claim 1 further comprising:

forming a conductive layer over the etch stop layer; and

wherein:

forming the through silicon via includes removing a portion of the conductive layer with a high down force.

5. The method as claimed in claim 1 further comprising:

forming a conductive layer over the buffer layer; and

wherein:

forming the through silicon via includes removing a portion of the conductive layer with the low down force.

6. A method of manufacture of an integrated circuit system comprising:

forming an interlayer dielectric over a bulk substrate having an active side;

forming an etch stop layer over the bulk substrate;

forming a buffer layer on the etch stop layer;

forming a hard mask on the buffer layer;

forming a recess in the bulk substrate;

forming a conductive layer within the recess;

forming a through silicon via through the etch stop layer with the hard mask detected and the buffer layer removed with a low down force; and

~~forming a passivation layer on the through silicon via and the etch stop layer.~~

7. The method as claimed in claim 6 wherein forming the etch stop layer over the interlayer dielectric.

8. The method as claimed in claim 6 wherein forming the through silicon via includes removing a portion of the conductive layer with a high selectivity slurry to the etch stop layer, the high selectivity slurry having a high removal ratio of the buffer layer to the etch stop layer.

9. The method as claimed in claim 6 further comprising forming a contact along the active side.

10. The method as claimed in claim 6 wherein forming the through silicon via includes forming the through silicon via within the recess.

11. An integrated circuit system comprising:

a bulk substrate having a recess;

an etch stop layer over the bulk substrate;

a through silicon via through the etch stop layer, the through silicon via having characteristics of being formed with a hard mask detected and a buffer layer removed; and

a passivation layer on the through silicon via and the etch stop layer.

12. The system as claimed in claim 11 wherein the through silicon via is coplanar with the etch stop layer.

13. The system as claimed in claim 11 wherein the through silicon via is in the bulk substrate.

14. The system as claimed in claim 11 further comprising:

a liner within the recess; and

wherein:

the through silicon via is over the liner.

15. The system as claimed in claim 11 wherein the through silicon via has characteristics of being formed with a low down force.

16. The system as claimed in claim 11 wherein:

the bulk substrate has an active side; and

wherein:

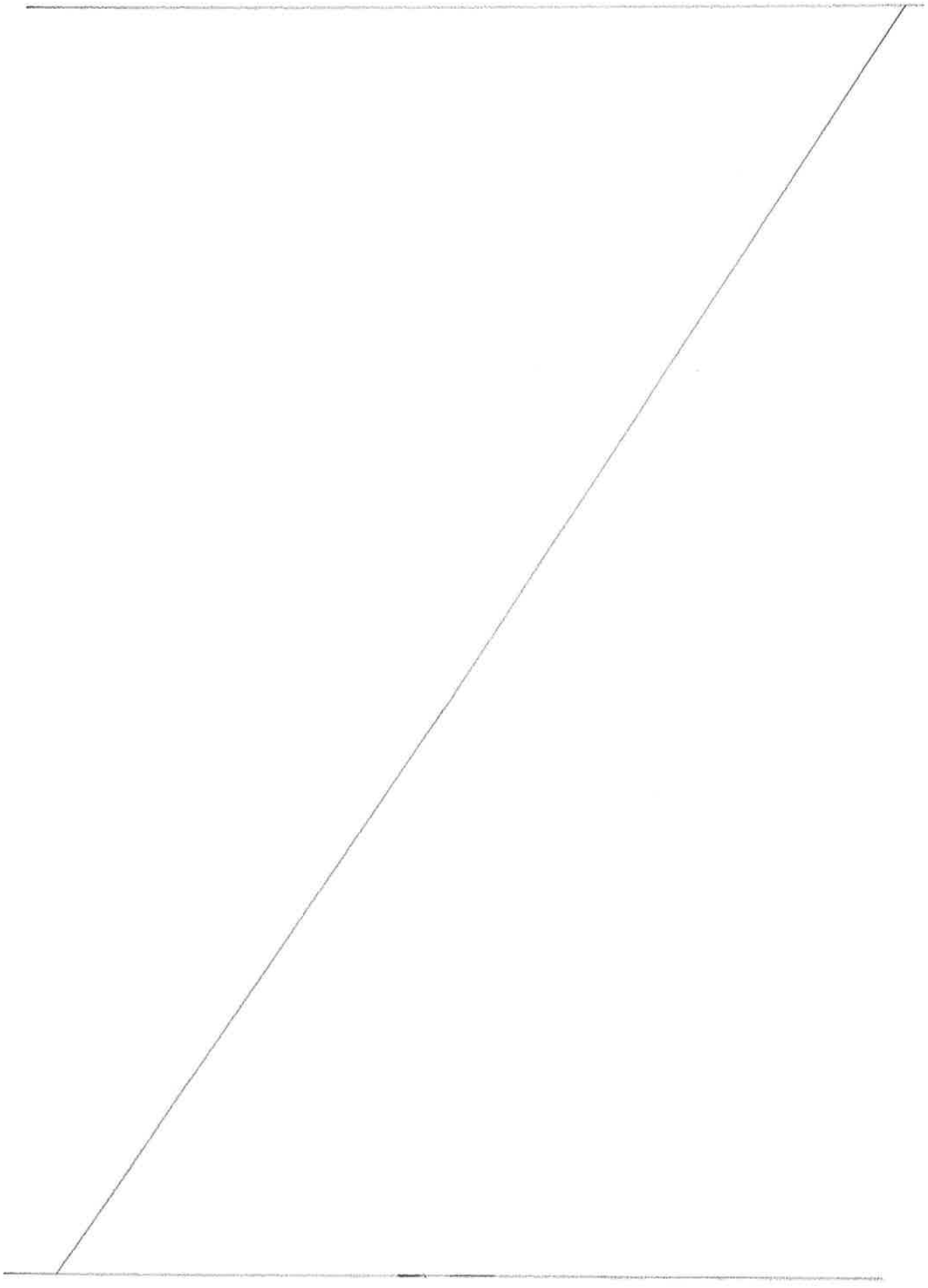
an interlayer dielectric over the bulk substrate.

17. The system as claimed in claim 16 wherein the etch stop layer is over the interlayer dielectric.

18. The system as claimed in claim 16 wherein the through silicon via has characteristics of being formed with the buffer layer removed with a high selectivity slurry to the etch stop layer, the high selectivity slurry having a high removal ratio of the buffer layer to the etch stop layer.

19. The system as claimed in claim 16 further comprising a contact along the active side.

20. The system as claimed in claim 16 wherein the through silicon via is within the recess.



What is claimed is:

1. A method of manufacture of an integrated circuit system comprising:
providing a bulk substrate;

forming an interlayer dielectric directly on the bulk substrate;

forming a contact of a first conductive material in the interlayer dielectric;

forming an etch stop layer over the bulk substrate;

forming a buffer layer on the etch stop layer;

forming a hard mask on the buffer layer;

forming a recess through the etch stop layer;

forming an insulator in the recess and over the etch stop layer;

forming a barrier layer over the insulator;

depositing a second conductive material different from the first conductive material of the contact over the barrier layer;

applying a first planarization force to remove portions of the first conductive material, the barrier layer, and the insulator until the hard mask is reached;

applying a second planarization force to remove the hard mask and the buffer layer such that a top surface of the etch stop layer is coplanar with top surfaces of the insulator, the liner, and the second conductive material; and

forming a passivation layer directly on the top surfaces of the second conductive material and the etch stop layer, the second conductive material and the etch stop layer having uniform surface planarity.

2. The method as claimed in claim 1 wherein forming the through silicon via includes forming the through silicon via coplanar with the etch stop layer.

3. The method as claimed in claim 1 wherein forming the through silicon via includes forming the through silicon via in the bulk substrate.

4. The method as claimed in claim 1 further comprising:
forming a conductive layer over the etch stop layer; and wherein:

forming the through silicon via includes removing a portion of the conductive layer with a high down force.

5. The method as claimed in claim 1 further comprising:
forming a conductive layer over the buffer layer; and wherein:

forming the through silicon via includes removing a portion of the conductive layer with the low down force.

6. A method of manufacture of an integrated circuit system comprising:
providing a bulk substrate;

forming an interlayer dielectric directly on the bulk substrate having an active side;

forming a contact of a first conductive material in the interlayer dielectric;

forming an etch stop layer over the bulk substrate;

forming a buffer layer on the etch stop layer;

forming a hard mask on the buffer layer;

forming a recess through the etch stop layer;

forming an insulator in the recess and over the etch stop layer;

forming a barrier layer over the insulator;

depositing a second conductive material different from the first conductive material of the contact over the barrier layer;

applying a first planarization force to remove portions of the first conductive material, the barrier layer, and the insulator until the hard mask is reached;

applying a second planarization force to remove the hard mask and the buffer layer such that a top surface of the etch stop layer is coplanar with top surfaces of the insulator, the liner, and the second conductive material; and

forming a passivation layer directly on the top surfaces of the second conductive material through silicon via and the etch stop layer, the second conductive material through silicon via and the etch stop layer having uniform surface planarity.

7. The method as claimed in claim 6 wherein forming the etch stop layer over the interlayer dielectric.

8. The method as claimed in claim 6 wherein forming the through silicon via includes removing a portion of the conductive layer with a high selectivity slurry to the etch stop layer, the high selectivity slurry having a high removal ratio of the buffer layer to the etch stop layer.

9. The method as claimed in claim 6 wherein:
depositing the second conductive material includes depositing copper; and

forming the contact of the first conductive material includes forming the contact of tungsten.

10. The method as claimed in claim 6 wherein forming the through silicon via includes forming the through silicon via within the recess.

11. An integrated circuit system comprising:
a bulk substrate having a recess;

an interlayer dielectric directly on the bulk substrate;

a contact formed from a first conductive material in the interlayer dielectric;

an etch stop layer over the bulk substrate;

an insulator formed in the recess;

a liner over the insulator;

a through silicon via formed from a second conductive material different from the first conductive material of the contact, positioned through the etch stop layer, a top surface of the etch stop layer that is coplanar with top surfaces of the insulator, the liner, and the through silicon via; and

a passivation layer directly on the top surfaces of the through silicon via and the etch stop layer.

12. The system as claimed in claim 11 wherein the through silicon via is coplanar with the etch stop layer.

13. The system as claimed in claim 11 wherein the through silicon via is in the bulk substrate.

14. The system as claimed in claim 11 wherein:
the liner is within the recess; and

the through silicon via is over the liner.

15. The system as claimed in claim 11 wherein the through silicon via is free of dishing.

16. The system as claimed in claim 11 wherein the bulk substrate has an active side.

17. The system as claimed in claim 16 wherein the etch stop layer is over the interlayer dielectric.

18. The system as claimed in claim 16 wherein the through silicon via has polishing marks characteristic of being formed with the buffer layer removed with a high selectivity slurry to the etch stop layer, the high selectivity slurry having a high removal ratio of the buffer layer to the etch stop layer.

19. The system as claimed in claim 16 wherein the second conductive material is copper and the first conductive material is tungsten.

20. The system as claimed in claim 16 wherein the through silicon via is within the recess.