

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
13 September 2007 (13.09.2007)

PCT

(10) International Publication Number
WO 2007/103745 A3

(51) International Patent Classification:
GI1C 29/34 (2006.01)

(21) International Application Number:

PCT/US2007/063097

(22) International Filing Date: 1 March 2007 (01.03.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/365,648 1 March 2006 (01.03.2006) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

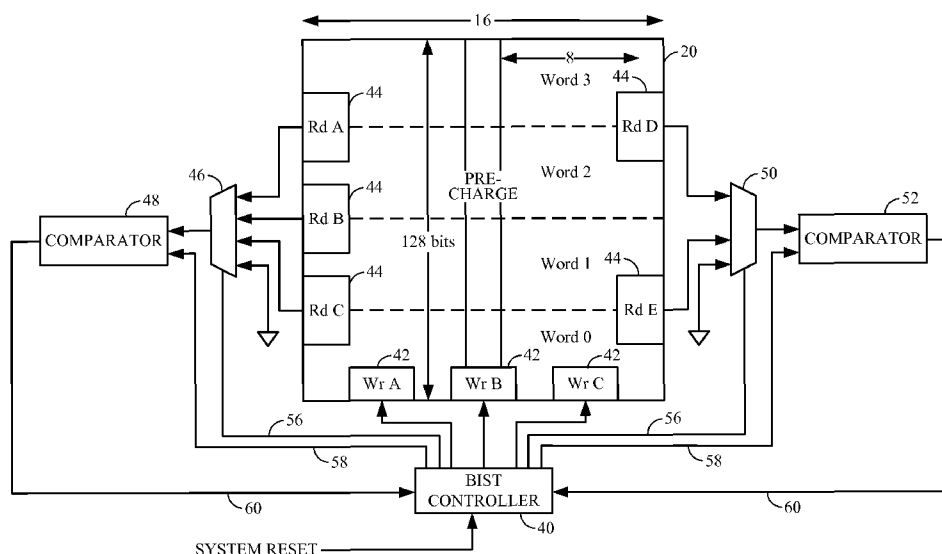
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: AT-SPEED MULTI-PORT MEMORY ARRAY TEST METHOD AND APPARATUS



(57) Abstract: A multi-port memory array is tested by simultaneously writing data to the array via two or more write ports, and/or simultaneously reading data from the array via two or more read ports, at the processor operating frequency. Comparing the data read from the array to that written to the array may be performed sequentially or in parallel. Comparator circuits are effectively disabled during normal processor operations. By simultaneously writing and/or reading data via multiple ports, latent electrical marginalities may be exposed. In addition, writing test patterns using multiple write ports and reading the patterns using multiple read ports significantly reduces test time during semiconductor manufacturing tests.



- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

(88) **Date of publication of the international search report:**
29 November 2007

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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