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(54) TRAFFIC SIGNAL CONTROL APPARATUS

(71) We, OMRON TATEISI ELECTRONICS CO. a Japanese Body Corporate, of 10 Tsuchido-cho, Hanazono, Ukyo-ku, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to traffic signal control apparatus, and, more particularly, to control apparatus for systematically controlling a plurality of local stations, having traffic signal equipment, from a remote central control station or central equipment.

In such a traffic signal control apparatus, control of traffic signals by an electronic computer provided in a central control station is transferred, if for any reason the computer should fail, to control by a fail-safe apparatus provided in the central station. At the time of transfer of control by the computer to control by the fail-safe apparatus, the systematic control will be distorted unless the fail-safe apparatus and the local traffic signal controllers in the local equipments are synchronized.

The object of the invention is to provide a traffic signal control apparatus for controlling a plurality of local traffic signals, wherein a fail-safe apparatus and local traffic signal controllers are synchronized at the time of transfer from the control by a computer to control by the fail-safe apparatus, whereby the transfer of control can be performed without distorting the display of traffic signals.

According to the invention, there is provided traffic signal control apparatus for switching the phase of display of traffic signals at an intersection by means of a local traffic signal control unit installed at the intersection and a central control equipment for controlling a plurality of such local traffic signal control units, comprising a phase counter for advancing the phase of the traffic signals; a phase-timing means, provided in the local traffic signal control

unit, for time-counting during the successive display phases of the traffic signals, and for generating a signal each time the time-count value, as counted by a time counter of the phase-timing means, reaches a pre-set value in each phase of display; a fail-safe apparatus adapted to transmit a hold signal while the phase of the said fail-safe apparatus is in coincidence with that of the local equipment; and a logic control circuit responsive to a signal from said phase-timing means and to the simultaneous absence of a hold signal from said fail-safe apparatus for advancing the phase counter to the next signal phase, and for clearing the time counter so as to begin counting the phase period of the next phase, the logic control circuit also being responsive to a signal from said phase-timing means, and to the simultaneous existence of the hold signal from the fail-safe apparatus for stopping the time counter, and to the subsequent change of phase in the fail-safe apparatus for advancing the phase counter to the next signal phase, and for clearing the time counter to commence the time counting of the next successive phase.

The central control equipment may comprise a computer, from which a signal is transmitted to the local equipment during normal operation of the computer. This signal, which will be described hereinafter as a hold signal, inhibits the control of the traffic signals by the local stations and the traffic signals are controlled instead by the computer. If the computer should fail, a hold signal from the computer is no longer transmitted to the local stations, and the fail-safe apparatus or other signal generating means transmits the hold signal to the local stations only when the phases of the fail-safe apparatus and the local stations are in coincidence. In the fail-safe apparatus are set the times for providing right-of-way for a main street at respective intersection and the times for providing right-of-way for a cross street thereof, the times being counted by a clock or a time counter. The periods for providing right-of-way for the main street or

the cross street by the fail-safe apparatus are called the phases of the fail-safe apparatus.

When the hold signal is not present at the time of transfer from control by the computer to control by the fail-safe apparatus, each local station advances a respective phase counter thereof by a signal generated each time the period of the phase of display of traffic signals has elapsed in each phase. The data of each period of the phases of display of traffic signals are pre-set in the equipment at the local station. The phase counter switches the phase of display of the traffic signals each time the phase counter is advanced. The local controller clears a respective time counter thereof by the signal above described so that the time counter commences counting of the time of succeeding phase of traffic signals when the traffic signals is switched by the phase counter. Thus the timing of each phase of the display of traffic signals is controlled in accordance with the phase periods pre-set in the local traffic signal equipment, if the phase of the fail-safe apparatus is not in coincidence with that of the local equipment at the time of transfer from control by the computer to control by the fail-safe apparatus until both the phases coincide.

If, when the time counter in a respective local equipment has counted out the pre-set time of the phase at the time of transfer of control, the hold signal is present, the time counting of the time counter is stopped for a while, and at the time when the phase of the fail-safe apparatus is advanced, a signal is generated by a suitable means. This signal is supplied to the phase counter and to the time counter of the local equipment, to advance the phase counter as well as to commence time counting of the time counter, thereby the control of the local equipment is transferred to the control by the fail-safe apparatus.

Thus, the control by the computer is transferred to control by the fail-safe apparatus at a time when the phase of the fail-safe apparatus is advanced after the right-of-way period for main street or right-of-way period for cross street has elapsed while the phase of the fail-safe apparatus is in coincidence with the phase of the local equipment, both of these right-of-way periods being set in the fail-safe apparatus.

An embodiment of the invention will now be described by way of example, reference being made to the accompanying drawings in which:

Figure 1 is a block diagram illustrating the equipment of one of a large number of local stations for controlling traffic signals at respective intersections;

Figure 2 is a wiring diagram of a part of the local equipment of Figure 1;

Figure 3 is a block diagram of the means

for generating hold signal utilized in the invention;

Figure 4 is an explanatory drawing for explaining the operation of the registers of Figure 3, and

Figure 5 is a block diagram illustrating an embodiment of the hold signal generator provided in a central equipment.

In Figure 1, 1 denotes a clock pulse generator which generates one pulse per second. These pulses will be described hereinafter as "second pulses." 2 denotes an AND gate, 3 and 4 denote time-counters respectively, 5 denotes a diode AND matrix, 6 to 11 denote diodes constituting OR circuits in the matrix 5, 12 to 17 denote diodes constituting AND circuits in the matrix 5, 18 denotes a differentiation circuit, 19 denotes a bistable vibrator, (hereinafter to be described as a flip-flop), 20 and 21 denote inhibit circuits, 22 denotes a differentiation circuit, 23 denotes an OR circuit, 24 denotes a phase counter, 25 denotes a controller for traffic signal lights, 26 denotes a terminal for receiving phase advance signals from a central station, and 27 denotes a terminal for receiving hold signals from the central station.

Diodes 6 to 11 and 12 to 17 constitute a part of matrix 5 as illustrated in Figure 2. 30 and 31 are resistances, 34, 35, 36, 37 are pin hole connectors which are connected respectively to various outputs of a time counter, 32, 33 are diodes constituting AND circuits respectively together with the diodes 12 and 13, and the diodes 6, 7 constitute OR circuits respectively.

Referring again to Fig. 1, the outputs of the diodes 6 and 9 are connected to the reset input terminal of the flip-flop 19 as well as to the input terminal of the inhibit circuit 21. The respective output of the diodes 7, 8; 10, 11 is connected to the input terminal of the differentiation circuit 18, the output terminal of the differentiation circuit 18 is connected to the input terminal of inhibit circuit 20, and the output terminal of inhibit circuit 21 is connected to the input terminal of the differentiation circuit 22. The phase advance signals are supplied to the OR circuit 23 through the terminal 26 from the central equipment. The output of the inhibit circuit 20 and the differentiation circuit 22 are also supplied to the OR circuit 23, and the output of the OR circuit 23 is supplied to the input of the phase counter 24 as well as to the clearance inputs of the counters 3, 4 and also to the set input of the flip-flop 19. The signal lights controller 25 is controlled by the output of the phase counter 24.

The data of Green period (1G), Yellow period (1Y) and Red period (1R) of the display of traffic signals for a main street, and the data of Green period (2G), Yellow period (2Y) and Red period (2R) of the

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display of traffic signals for a cross street are set in the matrix 5. The AND gate 2 is open when the set output of the flip-flop 19 is supplied thereto, thereby allowing the second pulses generated by the generator 1 to be supplied to, and counted by, the counters 3, 4. The counters 3, 4 constitute one overall counter.

The phase counter 24 has output stages for 1G, 1Y, 1R, 2G, 2Y and 2R. When the output of the stage for 1G of the phase counter 24 is "1", the phase of display of the traffic signals is made 1G by the controller 25. Similarly, when the output of the stage for 1Y or 1R, 2G, 2Y, 2R of the counter 24 is "1", the phase of display of the traffic signals is made 1Y or 1R, 2G, 2Y, 2R, respectively. Hereinafter, the state that the output of the stage of phase counter 24, for 1G (or 1Y, 1R, 2G, 2Y, 2R) is "1" will be described as the phase of the counter 24 is 1G (or 1Y, 1R, 2G, 2Y, 2R).

Now the operation of the control by the computer in the central equipment will be explained. While the local equipment is under control of the computer, the hold signal is generated by the central equipment and the hold signal is transmitted to the local equipment, and is supplied to the inhibit circuits 20, 21 through the terminal 27, thereby inhibiting the circuits 20, 21. The hold signal can be obtained utilizing the output of the computer while the computer is operating normally. All the phase advance signals are generated by the computer and are supplied to the phase counter 24 through the OR circuit 23, thereby advancing the phase counter 24. The phase advance signals are also supplied to the counters 3, 4 through the OR circuit 23, thereby clearing the counters 3, 4. Further, the phase advance signals are supplied to the set-input of the flip-flop 19.

In the state where the inhibit circuits 20, 21 are inhibited by the hold signal, the diode 6 or 9 generates a termination signal when the count value of the counters 3, 4 reaches the phase period of 1G or 2G pre-set in the matrix 5 while the phase of the phase counter 24 is 1G or 2G. The termination signal is supplied to the inhibit circuit 21. However, the output of the inhibit circuit 21 does not become "1" since it is inhibited. Accordingly, the output of the OR circuit 23 does not become "1". The termination signal is also supplied to the reset-input of the flip-flop 19 through a line 28, thereby the flip-flop 19 is reset, and the set-output thereof becomes "0". Accordingly, the AND gate 2 is closed and the counters 3, 4 stop their time counting. When the phase advance signal is transmitted from the computer in this state, and supplied to the OR circuit 23 through the terminal 26, the output of the OR circuit 23 becomes "1", and advances

the phase of the counter 24 and accordingly the phase of display of traffic signals to 1Y or 2Y, and, at the same time, the counters 3, 4 are cleared and the flip-flop 19 is set by the output "1" of the OR circuit 23. The AND gate 2 is open upon set of the flip-flop 19, and thereby the counters 3, 4 commence the counting of time of 1Y or 2Y. Similarly, when the count value of the counters 3, 4 reaches the pre-set phase period of 1Y or 2Y during the phase of the phase counter 24 is 1Y or 2Y, the diode 7 or 10 in the matrix 5 generates a termination signal. This signal is supplied to the differentiation circuit 18, thereupon the output of the differentiation circuit 18 is supplied to the inhibit circuit 20. However, since the inhibit circuit 20 is inhibited by the hold signal, the output of the inhibit circuit 20 does not become "1", and, accordingly, no signal is supplied to the phase counter 24. The phase counter 24 is advanced, by the advance signal which is transmitted later from the computer in the central equipment, to the next phase 1R or 2R. At the time of the advance of the counter 24 to the phase 1R or 2R, the advance signal from the computer is also supplied to the counters 3, 4. The counters 3, 4 are cleared by the signal and commence the counting of phase period of 1R or 2R. When the count value of the counters 3, 4 reaches the pre-set phase period of 1R or 2R, the diode 8 or 11 generates a termination signal. The phase counter 24 is not advanced by this termination signal for the same reason as described with respect to the termination signal at the end of the phase 1Y or 2Y. As described above, the local equipment, even though it is operating, supplies no signal to the counter 24, and the counter 24 is controlled by the computer.

If the computer should fail for some reason, the computer ceases the transmission of the phase advance signals to the local equipment. At the same time, discrimination circuits provided in the central equipment discriminate whether the phase of the fail-safe apparatus is in coincidence with the phases of the local equipments, respectively. The phase of a local equipment is the same as the phase of display of a local equipment, which in turn is the same as the phase of display of traffic signals thereof. The fail-safe apparatus comprises, corresponding to each local equipment, as illustrated in Fig. 3, two registers 41 and 42, a flip-flop 43, AND circuits 44 and 45 and an OR circuit 46. The fail-safe apparatus transmits signals for terminating the period of 1G and the period of 2G to the local equipment. The outputs of the registers 41 and 42 become high level alternately, as shown in Fig. 4. The output of the register 41 falls to a low level at the times t_1 and t_2 where 1G period is to be ter-

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minated, and the output of the register 42 falls to a low level at the times t_1 and t_2 where 2G period is to be terminated. Accordingly, the output of the register 41 is at a high level during the time from t_1 to t_2 and from t_3 to t_4 , and the output of the register 41 is at a high level during the time from t_2 to t_3 . The flip-flop 43 is set upon rising of the output of the register 42. In other words, the flip-flop 43 is reset upon falling of the output of the register 41, and is set upon falling of the output of the register 42. The set output of the flip-flop 43 is supplied to the AND circuit 44, and the reset output of the flip-flop 43 is supplied to the AND circuit 45. A signal is transmitted from the local equipment while the phase of display of the local signals is 1G or 2G, and is supplied to respective another input of the AND circuits 44 and 45 through the respective terminals 47 and 48. Therefore, if the phase of display of the traffic signals is 1G while the output of the register 41 is at the high level, then the output of the AND circuit 44 becomes "1". Similarly, if the phase of display of the traffic signal is 2G while the output of the register 42 is at the high level, then the output of the AND circuit 45 becomes "1". When the output of the AND circuit 44 or 45 is "1", then the output of the OR circuit 46 is "1", and this output is transmitted to the local equipment as a hold signal.

Assume that the phase of the local equipment becomes 1G during the time t_1 and t_2 , then the output of the AND circuit 44 becomes "1", and the hold signal is transmitted to the local equipment, thereby the inhibit circuits 20 and 21 in the local equipment are inhibited. If the phase of the local equipment is 1G until the time t_2 , the output of the AND circuit 44 becomes "0" at the time t_2 in accordance with the fall of the output of the register 41 to the low level. Accordingly, the output of the OR circuit 46 becomes "0" at the time t_2 , thereby the hold signal disappears. Then the local equipment advances the phase of display of the traffic signals in accordance with the data of phase periods pre-set in the matrix 5.

If the phase period 1G pre-set in the matrix 5 has elapsed before the time t_2 , then the output of the diode 6 becomes "1", thereby the flip-flop 19 is reset, and the supply of the second pulses to the counters 3 and 4 ceases. Accordingly, the counters 3 and 4 stop counting, and thus the output of the diode 6 is held at "1". Since the inhibit circuit 21 is inhibited, the output "1" of the diode 6 does not serve for advancing the phase counter 24. In this case, the outputs of the AND circuit 44 becomes "0" upon falling of the output of the register 41 at the time t_2 , and accordingly the output of the OR circuit 46 becomes "0," thereby the hold signal

disappears. Since the output of the diode 6 is held at "1" at this time, the output of the differentiation circuit 22 appears upon release of inhibit circuit 21 and, accordingly, the output of the OR circuit 23 becomes "1". The counter 24 is advanced by the output "1" of the OR circuit 23 to the phase of 1Y. At the same time, the flip-flop 19 is set and the counters 3 and 4 are cleared by the output "1" of the OR circuit 23, thereby the counters 3 and 4 commence the counting of the phase period of 1Y. As the hold signal is not transmitted from the fail-safe apparatus until the phase of the local controller is advanced to the next 2G, the phase 1Y and succeeding phase 1R are advanced each time the count value of the counters 3, 4 reaches respective phase period pre-set in the matrix 5. When the count value of the counter 3, 4 reaches the phase period 1Y or 1R pre-set in the matrix 5, then the output of diode 7 or 8 becomes "1", thereupon the differentiation circuit 18 generates a differentiation output which is supplied to the OR circuit 23 through inhibit circuit 20. Thereby the output of the OR circuit 23 becomes "1", and advances the counter 24, and, at the same time, clears the counters 3, 4 to commence the counting of the succeeding phase period, while the flip-flop 19 is held in the set state.

The operation while the phase of display is 2G is similar to the operation as described above.

The phase 1G or 2G of the phase of display of the traffic signals is terminated, or advanced to the succeeding phase, upon extinction of the hold signal when the hold signal was present at the time the count value of the counters 3, 4 reaches the respective pre-set value of 1G or 2G.

The operations as described above can be summarized as follows.

When the computer ceases transmission of the phase advance signals, the fail-safe apparatus does not generate the hold signal if the phase of the fail-safe apparatus is not in coincidence with that of the display of the local traffic signals, thereby the hold signal is "0". In this case, the inhibit circuits 20 and 21 are not inhibited, and, when the count value by the counters 3, 4 while the phase of display is 1G or 2G, reaches, respectively, pre-set value in the matrix 5, the termination signal is generated in the local equipment, in other words, the output of the diode 6 or 9 becomes "1". This output "1" is supplied to the differentiation circuit 22 through the inhibit circuit 21, thereupon the differentiation output from the circuit 22 is supplied to the phase counter 24 through the OR circuit 23 and the phase counter 24 is advanced, and the phase of display of traffic signals is switched. The flip-flop 19 is reset by the output "1" of the diode 6 or 9,

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however, when the output of the OR circuit 23 becomes "1", this output clears the counters 3, 4 and, at the same time, sets the flip-flop 19. Thereby the AND gate 2 is open and the counters 3, 4 commence the counting of the succeeding phase period. Each time the count value of counters 3, 4 reaches the respective pre-set value of 1Y, 1R; or 2Y, 2R in the matrix 5, the respective output of the diode 7, 8; 10 or 11 becomes "1", and is supplied to the differentiation circuit 18, thereby the differentiation output thereof appears. The differentiation output is supplied to the phase counter 24 through the inhibit circuit 20 and the OR circuit 23, thereby the counter 24 is advanced, and the phase of display of traffic signals is switched. Each time the output of the OR circuit 23 becomes "1", the counters 3, 4 are cleared and commence the counting of the succeeding phase period. Thus the traffic signals are controlled in accordance with the pre-set phase times in the matrix 5.

Since the phase periods or cycle period pre-set in the matrix 5 differs from the phase periods or cycle period set in the fail-safe apparatus as is well known, the phases of the fail-safe apparatus and the phase counter 24 comes into coincidence during the control of the traffic signals in accordance with the pre-set phase times in the matrix 5.

If the phase of the fail-safe apparatus is in coincidence with the phase of display of local traffic signals at the time the computer ceases transmission of the phase advance signals, or comes into coincidence with the phase of display of local traffic signals during the control by the local equipment, the hold signal is transmitted from the fail-safe apparatus, thereby the inhibit circuits 20 and 21 are inhibited. When the count value of the counters 3, 4 reaches the pre-set value of 1G or 2G in the matrix 5, output of the diode 6 or 9 becomes "1", thereby the flip-flop 19 is reset. Accordingly, the supply of second pulses to the counters 3, 4 ceases and the counters 3, 4 stop the counting. When the phase of the fail-safe apparatus is switched and the hold signal disappears thereby the inhibit circuits 20, 21 are released, the phase counter 24 is advanced to the succeeding phase by the output "1" of the diode 6 or 9, and, at the same time, the counters 3, 4 are cleared and the flip-flop 19 is set. Upon the setting of the flip-flop 19, the counters 3, 4 commence the counting of the time of the succeeding phase. Since the hold signal is not supplied to the inhibit circuits 20 and 21 during the phases 1Y, 1R, 2Y and 2R of the display of the traffic signals, these phases are advanced respectively in accordance with the phase times pre-set in the matrix 5. After the phase 1G or 2G of the display is once terminated at the time of the switching of the phase of

the fail-safe apparatus, the succeeding respective phase of 1G and 2G of the display is terminated at each time the phase of the fail-safe apparatus is switched.

Further, if the hold signal disappears, in the case the hold signal has been generated and transmitted to the local equipment before the count value of the counters 3, 4 reaches the pre-set value of the phase of 1G or 2G in the matrix 5, the phase counter 24 is advanced in accordance with the pre-set phase times in the matrix 5.

Fig. 5 is a block diagram illustrating an embodiment of hold signal generating apparatus. 51 denotes an electronic computer, 52 denotes a flip-flop which is set by the output of the computer 51 when it is operating normally, 53 denotes a second pulse generator, 54 denotes a time counter for counting second pulses generated by the generator 53. The second pulse generator 53 may be a clock which generates one pulse per second. 57, 58, 59 and 60 respectively denote a register. Data of the time for starting the phases of 1G and 2G, or data of the time for terminating the phases of 2G and 1G, at a local equipment are respectively set in the registers 57 and 58, and data of the time for starting the phases 1G and 2G, or data for terminating phases 2G and 1G, at another local equipment are respectively set in the registers 59 and 60. A plurality of sets of the registers 57, 58; 59, 60 are provided in a central equipment, two sets of which are shown in Fig. 5. 61, 62, 63 and 64 denote respectively a coincidence circuit. Each output terminal of the registers 57, 58, 59 and 60 is connected to the respective one input terminal of the coincidence circuits 61, 62, 63 and 64; and the output terminal of the counter 54 is connected to each other input terminal of the coincidence circuits 61 through 64. A flip-flop 65 is set by the output of the circuit 61, and is reset by the output of the circuit 68, and is reset by the output of the circuit 62. A flip-flop 66 is set by the output of the circuit 64. Since both circuits following the flip-flops 65 and 66, respectively, are the same for respective local equipment, only the circuit following the flip-flop 65 will be explained hereunder. The set output terminal of the flip-flop 65 is connected to one impact terminal of an AND circuit 67, and the rest output terminal of the flip-flop 65 is connected to one input terminal of an AND circuit 68. Signals transmitted from the local equipment of which data of the time for starting 1G and 2G are set in the registers 7, 8, respectively, are supplied to the other inputs of the AND circuits 67 and 68. That is to say, the signal transmitted from the local equipment while the phase of display thereof is 1G, is supplied to the AND circuit 67, and the signal, transmitted while the phase

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of display is 2G, is supplied to the AND circuit 68. The output terminals of the AND circuits 67 and 68 are connected to the input terminal of an OR circuit 69, and the output terminal of the OR circuit 69 is connected to one input terminal of an AND circuit 70. The output terminal of an inverter 71 of which input terminal is connected to the set output terminal of the flip-flop 52, is connected to the other input terminal of the AND circuit 70. The set output terminal of the flip-flop 52 and the output terminal of the AND circuit 70 are connected to the input terminal of an OR circuit 72. The output of the OR circuit 72 is transmitted to the local equipment, and is supplied to the inhibit circuits 20 and 21 in Fig. 1 through the terminal 27 as the hold signal.

When the computer 51 is operating normally, it transmits phase advance signals to each local equipment, thereby the phase of display of each local equipment is advanced.

During the normal operation of the computer 51, the flip-flop 52 is set and the set output thereof is "1". Accordingly the output of the inverter 71 is "0", and the output of the AND circuit does not become "1". However, since the set output of the flip-flop 52 is "1", the output of the OR circuit 72 becomes "1", and this is transmitted to the local equipment as the hold signal.

Should the computer 51 fail, the phase advance signal is no longer transmitted to the local equipment. Then the flip-flop 52 is reset, and the set output thereof becomes "0", and, accordingly, the output of the inverter 71 becomes "1". When the count value of the counter 54 reaches the value set in the register 57 or 58, the output of the coincidence circuit 61 or 62 appears. The output of the coincidence circuit 61 appears, for example, at the times t_1 and t_2 in Fig. 4, then the output of the coincidence circuit 62 appears at the times t_2 and t_3 , thereby the flip-flop 65 is set during the periods from t_1 to t_2 and from t_2 to t_3 , and is reset during the period from t_3 to t_4 . If the phase of display of the local traffic signals becomes 1G while the flip-flop 65 is set, then the output of the AND circuit 67 becomes "1". Since the output of the inverter 71 is "1", the output of the AND circuit 70 becomes "1", and accordingly the output of the OR circuit 72 becomes "1" when the output of the AND circuit 67 becomes "1" and the hold signal is transmitted to the local equipment. Also, if the phase of display of the local traffic signals becomes 2G while the flip-flop 65 is reset, then the output of the AND circuit 68 becomes "1", and thereby the output of the OR circuit 72 becomes "1", and the hold signal is transmitted to the local equipment. If the phase

of display of the local traffic signals does not become 1G or 2G, respectively, while the flip-flop 65 is set or reset, the hold signal is not transmitted to the local equipment.

Although the flip-flop 65 and the following circuits 67, 68, 69, 70 and 71 are provided in the central station in the embodiment illustrated in Fig. 5, the circuit 65 through 72 for generating the hold signal may be provided in the local equipment.

WHAT WE CLAIM IS:—

1. Traffic signal control apparatus for switching the phase of display of traffic signals at an intersection by means of a local traffic signal control unit installed at the intersection and a central control equipment for controlling a plurality of such local traffic signal control units, comprising a phase counter for advancing the phase of the traffic signals; a phase-timing means, provided in the local traffic signal control unit, for time-counting during the successive display phases of the traffic signals, and for generating a signal each time the time-count value, as counted by a time counter of the phase-timing means, reaches a pre-set value in each phase of display; a fail-safe apparatus adapted to transmit a hold signal while the phase of the said fail-safe apparatus is in coincidence with that of the local equipment; and a logic control circuit responsive to a signal from said phase-timing means and to the simultaneous absence of a hold signal from said fail-safe apparatus for advancing the phase counter to the next signal phase, and for clearing the time counter so as to begin counting the phase period of the next phase, the logic control circuit also being responsive to a signal from said phase-timing means, and to the simultaneous existence of the hold signal from the fail-safe apparatus for stopping the time counter, and to the subsequent change of phase in the fail-safe apparatus for advancing the phase counter to the next signal phase and for clearing the time counter to commence the time counting of the next successive phase.
2. Traffic signal control apparatus according to claim 1 wherein the central control equipment is adapted normally to supply control signals for advancing the phase counter, and adapted when operative, to generate a further hold signal, said logic control circuit being adapted to inhibit the advancement of the phase counter by the signals from the phase-timing means whilst the said further hold signal exists.
3. Traffic signal control apparatus according to claim 1 or claim 2, wherein the time counting means comprises a clock pulse generator, a counter connected to the clock pulse generator by a gate, and a circuit coupled to the counter, and respon-

of display is 2G, is supplied to the AND circuit 68. The output terminals of the AND circuits 67 and 68 are connected to the input terminal of an OR circuit 69, and the output terminal of the OR circuit 69 is connected to one input terminal of an AND circuit 70. The output terminal of an inverter 71 of which input terminal is connected to the set output terminal of the flip-flop 52, is connected to the other input terminal of the AND circuit 70. The set output terminal of the flip-flop 52 and the output terminal of the AND circuit 70 are connected to the input terminal of an OR circuit 72. The output of the OR circuit 72 is transmitted to the local equipment, and is supplied to the inhibit circuits 20 and 21 in Fig. 1 through the terminal 27 as the hold signal.

When the computer 51 is operating normally, it transmits phase advance signals to each local equipment, thereby the phase of display of each local equipment is advanced.

During the normal operation of the computer 51, the flip-flop 52 is set and the set output thereof is "1". Accordingly the output of the inverter 71 is "0", and the output of the AND circuit does not become "1". However, since the set output of the flip-flop 52 is "1", the output of the OR circuit 72 becomes "1", and this is transmitted to the local equipment as the hold signal.

Should the computer 51 fail, the phase advance signal is no longer transmitted to the local equipment. Then the flip-flop 52 is reset, and the set output thereof becomes "0", and, accordingly, the output of the inverter 71 becomes "1". When the count value of the counter 54 reaches the value set in the register 57 or 58, the output of the coincidence circuit 61 or 62 appears. The output of the coincidence circuit 61 appears, for example, at the times t_1 and t_3 in Fig. 4, then the output of the coincidence circuit 62 appears at the times t_2 and t_4 , thereby the flip-flop 65 is set during the periods from t_1 to t_2 and from t_3 to t_4 , and is reset during the period from t_2 to t_3 . If the phase of display of the local traffic signals becomes 1G while the flip-flop 65 is set, then the output of the AND circuit 67 becomes "1". Since the output of the inverter 71 is "1", the output of the AND circuit 70 becomes "1", and accordingly the output of the OR circuit 72 becomes "1" when the output of the AND circuit 67 becomes "1" and the hold signal is transmitted to the local equipment. Also, if the phase of display of the local traffic signals becomes 2G while the flip-flop 65 is reset, then the output of the AND circuit 68 becomes "1", and thereby the output of the OR circuit 72 becomes "1", and the hold signal is transmitted to the local equipment. If the phase

of display of the local traffic signals does not become 1G or 2G, respectively, while the flip-flop 65 is set or reset, the hold signal is not transmitted to the local equipment.

Although the flip-flop 65 and the following circuits 67, 68, 69, 70 and 71 are provided in the central station in the embodiment illustrated in Fig. 5, the circuit 65 through 72 for generating the hold signal may be provided in the local equipment.

WHAT WE CLAIM IS:—

1. Traffic signal control apparatus for switching the phase of display of traffic signals at an intersection by means of a local traffic signal control unit installed at the intersection and a central control equipment for controlling a plurality of such local traffic signal control units, comprising a phase counter for advancing the phase of the traffic signals; a phase-timing means, provided in the local traffic signal control unit, for time-counting during the successive display phases of the traffic signals, and for generating a signal each time the time-count value, as counted by a time counter of the phase-timing means, reaches a pre-set value in each phase of display; a fail-safe apparatus adapted to transmit a hold signal while the phase of the said fail-safe apparatus is in coincidence with that of the local equipment; and a logic control circuit responsive to a signal from said phase-timing means and to the simultaneous absence of a hold signal from said fail-safe apparatus for advancing the phase counter to the next signal phase, and for clearing the time counter so as to begin counting the phase period of the next phase, the logic control circuit also being responsive to a signal from said phase-timing means, and to the simultaneous existence of the hold signal from the fail-safe apparatus for stopping the time counter, and to the subsequent change of phase in the fail-safe apparatus for advancing the phase counter to the next signal phase and for clearing the time counter to commence the time counting of the next successive phase.

2. Traffic signal control apparatus according to claim 1 wherein the central control equipment is adapted normally to supply control signals for advancing the phase counter, and adapted when operative, to generate a further hold signal, said logic control circuit being adapted to inhibit the advancement of the phase counter by the signals from the phase-timing means whilst the said further hold signal exists.

3. Traffic signal control apparatus according to claim 1 or claim 2, wherein the time counting means comprises a clock pulse generator, a counter connected to the clock pulse generator by a gate, and a circuit coupled to the counter, and respon-



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7 sive to the successive values counted in the counter reaching respective pre-set values, to generate the said signals.

5 4. Traffic signal control apparatus according to claim 3, including means responsive to the advancement of said phase counter for resetting said counter and for opening said gate to allow pulses to pass to said counter.

10 5. Traffic signal control apparatus according to any preceding claim, wherein said logic circuit includes inhibit gating means responsive to the presence of said hold signal and to the presence of said

further hold signal for preventing the passage of the signal from the phase timing means to the phase counter. 15

6. Traffic signal control apparatus, substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings. 20

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