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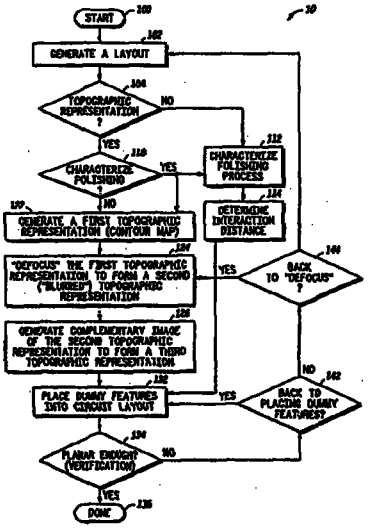
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(54) Title: PROCESS FOR DESIGNING A MASK



(57) Abstract: Selective placement of polishing dummy feature patterns, rather than indiscriminate placement of polishing dummy feature patterns, is used. Both low frequency (hundreds of microns and larger) and high frequency (10 microns and less) of topography changes are examined. The polishing dummy feature patterns can be specifically tailored to a semiconductor device and polishing conditions used in forming the semiconductor device. When designing an integrated circuit, polishing effects for the active features can be predicted. After polishing dummy feature pattern(s) are placed into the layout, the planarity can be examined on a local level (a portion but not all of the device) and a more global level (all of the device, devices corresponding to a reticle field, or even an entire wafer).

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