

STRUCTURE FOR RADIOFREQUENCY APPLICATIONS AND PROCESS FOR MANUFACTURING SUCH A STRUCTURE

FIELD OF THE INVENTION

5 The invention relates to a structure for radiofrequency applications and to a process for manufacturing such a structure.

BACKGROUND OF THE INVENTION

10 In radiofrequency (RF) applications, different types of structures may be used for making RF components.

 Among these structures, HR-SOI (acronym for “High Resistivity Silicon On Insulator”) type substrates are of interest.

 In the present text, “high resistivity” means an electrical resistivity of more than 500 Ohm.cm.

15 A Silicon On Insulator (SOI) structure comprises successively a silicon base substrate, a dielectric (e.g. oxide) layer (usually called “buried oxide” (BOX) layer), and a silicon active layer.

 To improve the insertion loss, harmonic distortion and isolation performance required for Radiofrequency (RF) switches, the silicon base substrate of an SOI substrate
20 was replaced by a high-resistivity base substrate in order to form a HR-SOI

 The adoption of HR-SOI wafers for RF applications has allowed monolithic integration of RF front-end module. This leads to smaller size, better reliability, improved performance and lower system cost.

25 While HR-SOI substrates are well suited for 2G and 3G applications, they suffer from the parasitic surface conduction (PSC) layer induced under the buried oxide due to fixed oxide charges which attract free carriers near the Si/SiO₂ interface.

 This drastically reduces the substrate effective resistivity by more than one order of magnitude, limiting the substrate capability in meeting performance requirement for next generation.

30 To address this intrinsic limitation and improve effective resistivity, a polycrystalline silicon layer is introduced between the dielectric layer and the high resistivity base substrate, to provide a trap-rich layer underneath the dielectric layer to freeze the PSC.

 These traps originate from the grain boundaries of the polycrystalline silicon layer in which RF components are to be made.

35 Reference can be made to document WO 2012/127006.

 FIG. 1 shows an enhanced HR-SOI structure that comprises an HR silicon substrate 1, covered successively by a polycrystalline silicon (also called “polysilicon”) layer 2’, an

oxide layer 4 and a monocrystalline silicon layer 3 that forms the active layer of the substrate.

Such an enhanced HR-SOI structure can be made by the Smart Cut™ process, which comprises the following steps:

- 5 - providing a HR silicon substrate,
- depositing a polycrystalline silicon layer on said HR silicon substrate,
- providing a monocrystalline silicon donor substrate comprising a weakened zone that defines the active layer to be transferred onto the HR silicon substrate; said weakened zone can be obtained by implantation of atomic species into the donor
- 10 substrate,
- forming a dielectric layer on at least one of the polycrystalline silicon substrate and the monocrystalline donor substrate, e.g. by oxidizing at least one of said substrates,
- bonding the donor substrate and the HR silicon substrate, the at least one dielectric layer being at the bonding interface; said at least one dielectric layer forms the BOX layer,
- 15 - detaching the donor substrate along the weakened zone, thereby transferring the monocrystalline active layer onto the HR silicon substrate.

The enhanced HR-SOI structure resulting from this process includes residual electrical charges at the interface between the BOX layer and the underlying layer, that are due to the implantation and oxidation steps.

- 20 Said electrical charges deteriorate the RF performance of the components that are later formed in or on the active layer. In particular, said electrical charges may create undesirable interactions between adjacent RF components.

- 25 The polycrystalline silicon layer is intended to trap said electrical charges and thus avoid their detrimental effect on the RF performance. Indeed, the surface of the polycrystalline silicon layer comprises a plurality of grain boundaries which allow trapping said electrical charges at the interface with the BOX layer.

- 30 Further information on this subject can be found in publications written by D. Lederer, R. Lobet and J.-P. Raskin, "Enhanced high resistivity SOI wafers for RF applications," *IEEE Intl. SOI Conf.*, pp. 46-47, 2004; D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 805-807, 2005; D. Lederer and J.-P. Raskin, "RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate", *IEEE Transactions on Electron Devices*, vol. 55, no. 7, pp. 1664-1671, 2008; and D. C. Kerr and al., "Identification of RF harmonic distortion on Si substrates and its reduction using a trap-rich layer", 978-1-4244-1856-5/08, IEEE 2008 IEEE.
- 35

However, the manufacturing of such an HR-SOI structure involves some steps carried out at high temperature (e.g. a heat treatment is carried out after bonding in order

to reinforce the bonding strength). Said high temperature induces recrystallization of the polycrystalline silicon layer, the underlying HR silicon substrate – which is monocrystalline – acting as a seed for such recrystallization. In other words, a recrystallization front propagates through the polysilicon layer from the interface with the HR monocrystalline silicon substrate.

When recrystallizing, the polysilicon layer loses its trapping efficiency due to the drop in the number of grain boundaries and larger grain size variation which could results in larger surface roughness and charge trapping uniformity.

In order to limit recrystallization, the thickness of the polysilicon layer can be set to a sufficiently high thickness such that, at the end of the high temperature step(s), at least a part of the polysilicon layer has not recrystallized yet.

Besides, a large deposited thickness is also needed to compensate the fact that the polysilicon layer has to be polished after deposition in order to reduce its roughness, said polishing step removing a certain thickness of the polysilicon layer.

For these reasons, in current enhanced HR-SOI structures, the deposited polysilicon layer typically has a thickness thicker than 2 μm .

However, increasing the thickness of the polysilicon layer has a drawback. Indeed, when the polysilicon layer is deposited using chemical vapour deposition (CVD), the polysilicon first forms nuclei on the surface of the HR silicon substrate, then forms small grains that progressively enlarge in a substantially conical way as the thickness of the polysilicon layer grows. As a result, the surface of the polysilicon layer opposite to the HR silicon substrate comprises less grain boundaries than the surface located at the interface with the HR silicon substrate. Hence, the greater the thickness of the polysilicon layer, the smaller the number of grain boundaries and thus the smaller the trapping efficiency of the polysilicon layer.

BRIEF DESCRIPTION OF THE INVENTION

A goal of the invention is to overcome the above-mentioned problems and in particular to allow reducing the thickness of the polycrystalline silicon layer without deteriorating the trapping efficiency of said layer.

Accordingly, the invention provides a structure for radiofrequency applications comprising:

- a monocrystalline substrate,
- a polycrystalline silicon layer directly on the monocrystalline substrate,
- an active layer on the polycrystalline silicon layer, intended to receive radiofrequency components,

said structure being characterized in that at least a first portion of the polycrystalline silicon layer extending from the interface of the polycrystalline silicon layer with the

monocrystalline layer includes carbon and/or nitrogen atoms located at the grain boundaries of the polycrystalline silicon, in a concentration comprised between 2% and 20%.

As will be explained in more detail below, the carbon and/or nitrogen atoms are trapped at grain boundaries of the polycrystalline silicon, which slows down the recrystallization kinetics.

This allows reducing the thickness of the polysilicon layer while still avoiding complete recrystallization of said layer at the end of the heat treatment(s).

Such a polysilicon layer with a reduced thickness comprises, at the surface opposite to the monocrystalline substrate, a greater number of grain boundaries and thus traps more efficiently the electrical charges present at said surface than a thicker layer. In addition, a smaller thickness of the polysilicon induces a limited surface roughness and thus minimizes the polishing step and more uniformity grain size across the wafer and wafer-to-wafer.

15

According to an embodiment, the whole polycrystalline silicon layer contains carbon and/or nitrogen atoms.

In such case, the thickness of the polycrystalline silicon layer ranges from 200 to 1000 nm.

20

According to another embodiment, the polycrystalline silicon layer further comprises, on the first portion containing carbon and/or nitrogen atoms, a second portion free from carbon and/or nitrogen atoms.

By "free" is meant that the concentration in carbon and/or nitrogen atoms is less than 0.5%.

25

In such case, the thickness of the first portion of the polycrystalline silicon layer advantageously ranges from 10 to 200 nm. The whole thickness of the polycrystalline silicon layer thus preferably ranges from 20 to 500 nm.

30

According to an embodiment, the monocrystalline substrate comprises at least one of: monocrystalline silicon having an electrical resistivity greater than 500 Ohm.cm, silicon carbide, and/or germanium.

According to an embodiment, the active layer comprises at least one of: a semiconducting material, a dielectric material, a ferroelectric material, and a substructure comprising at least one cavity and at least one suspended element on said cavity.

35

According to another embodiment, the structure further comprises a dielectric layer on the polycrystalline silicon layer, the active layer being on said dielectric layer.

Another object of the invention relates to a process for manufacturing such a structure.

Said process comprises:

- providing a monocrystalline substrate,
 - depositing, on said monocrystalline substrate, a polycrystalline silicon layer,
 - providing a donor substrate comprising an active layer intended to receive radiofrequency components,
 - 5 - bonding the monocrystalline substrate and the donor substrate such that the polycrystalline silicon layer and the active layer are at the bonding interface,
 - transferring the active layer onto the monocrystalline substrate and the polycrystalline silicon layer,
- said process being characterized in that during deposition of at least a first portion of the polycrystalline silicon layer located at the interface with the monocrystalline substrate,
- 10 carbon and/or atoms are deposited in said first portion.

Advantageously, the polycrystalline silicon layer is deposited by Low-Pressure Chemical Vapor Deposition (LPCVD) in a reactor.

- A gas containing carbon and/or nitrogen atoms is introduced in the LPCVD reactor
- 15 to form at least the first portion.

According to an embodiment, said gas is introduced in the LPCVD reactor during the deposition of the whole polycrystalline silicon layer.

The thickness of the polycrystalline silicon layer thus preferably ranges from 200 to 1000 nm.

- 20 According to another embodiment, after the first portion has been deposited, the process comprises stopping the introduction of the gas containing the carbon and/or nitrogen atoms in the LPCVD reactor and further depositing a carbon and/or nitrogen-free second portion of the polycrystalline layer, the concentration in carbon and/or nitrogen in the second portion being less than 0.5%.

- 25 The thickness of the first region of the polycrystalline silicon layer thus preferably ranges from 10 to 200 nm.

According to another embodiment, the process further comprises forming a dielectric layer on the polycrystalline silicon layer and/or on the active layer of the donor substrate.

30

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the invention will become apparent from the detailed description that follows, based on the appended drawings, wherein:

- FIG. 1 shows a cross sectional view of a known semiconductor on insulator structure comprising a polysilicon layer;
- 35 - FIG. 2 shows a cross sectional view of a structure according to an embodiment of the invention;

- FIG. 3 shows a cross sectional view of a structure according to another embodiment of the invention;

- FIGS. 4A to 4D show several steps of the manufacturing process of a structure according to the invention.

5 It is to be noted that the drawings may be not to scale.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

FIG. 2 illustrates a structure 100 according to a first embodiment of the invention.

The structure 100 comprises a monocrystalline substrate 1.

10 The monocrystalline substrate can be a bulk substrate made of a single material or a composite substrate made of a stack of different materials, at least a monocrystalline material lying at a main surface of the substrate.

Advantageously, the monocrystalline substrate is made of monocrystalline silicon having an electrical resistivity greater than 500 Ohm.cm, although other materials could
15 be selected.

For example, the following materials could be used to form the monocrystalline substrate: silicon, silicon carbide, germanium or a combination of at least two of said materials.

A polycrystalline silicon layer 2 extends directly on the monocrystalline substrate 1.
20 By “directly” is meant that the polycrystalline silicon is in contact with the material of the monocrystalline substrate at the interface I; in particular, no polycrystalline or amorphous layer is interposed between the monocrystalline substrate 1 and the polycrystalline silicon layer 2.

The polycrystalline silicon layer 2 includes carbon and/or nitrogen, meaning that
25 carbon and/or nitrogen atoms are located at the grain boundaries of the polycrystalline silicon. As will be explained in more detail below, said carbon and/or nitrogen atoms are typically introduced during growth of the polysilicon.

The concentration of carbon atoms in the polysilicon layer 2 is in the 2 – 20 % range, which can be determined using chemical composition characterization techniques such as
30 Auger Electron Spectroscopy or Secondary Ion Mass Spectrometry.

Said carbon and/or nitrogen concentration may be uniform throughout the thickness of layer 2 or can vary along the thickness of layer 2.

The thickness of the polycrystalline silicon layer 2 ranges typically from 200 to 1000 nm, which is much thinner than in prior art structure as illustrated in FIG. 1.

35 A dielectric layer 4, such as an oxide layer, can be present on the polysilicon layer 2. However, this layer 4 is optional.

The structure 100 then comprises, on the polysilicon layer 2 (or, if present, on the dielectric layer 4), an active layer intended to receive radiofrequency components. Said

radiofrequency components (not illustrated) can thus be formed on or in said active layer 3.

The active layer 3 can comprise a semiconducting material, a dielectric material, a ferroelectric material, and/or a substructure comprising at least one cavity and at least one
5 suspended element on said cavity.

FIG. 3 illustrates a structure 100 according to a second embodiment of the invention.

Elements designated by the same reference numerals as in FIG. 2 are the same and thus need not being described in detail again.

As compared to the structure of FIG. 2, the structure of FIG. 3 comprises a
10 polysilicon layer 2 that is made of two portions: a first portion 2a, extending from the interface I and a second portion 2b, extending on the first portion 2a.

The first portion 2a includes carbon and/or nitrogen.

The concentration of carbon and/or nitrogen atoms in the first portion 2a of the polysilicon layer is in the 2% - 20% range.

15 The thickness of said first portion 2a ranges from 10 to 200 nm.

By contrast, the second portion 2b is substantially free for carbon and/or nitrogen atoms. Assuming that some carbon and/or nitrogen atoms may have contaminated said second portion, for example during the manufacturing process, the concentration in carbon and/or nitrogen atoms of said second portion is less than 0.5%.

20 A manufacturing process of the structures illustrated in FIGS. 2 and 3 is described with reference to FIGS. 4A to 4D.

On the one hand, as shown in FIG. 4A, a monocrystalline substrate 1 is provided.

Said substrate is introduced in a reactor so as to carry out deposition of the polycrystalline layer. The deposition technique is advantageously Low-Pressure Chemical
25 Vapor Deposition (LPCVD) or plasma-enhanced LPCVD.

To that end, silane (SiH_4), disilane (Si_2H_6) or trisilane (Si_3H_8) and methane (CH_4) or methylsilane (SiH_3CH_3) are introduced in the reactor. The temperature in the reactor typically ranges from 500°C to 900°C.

30 Concurrently with the introduction of methylsilane or methane, a gas containing carbon and/or nitrogen is introduced in the reactor, so as to introduce said carbon and/or nitrogen atoms into the polysilicon layer being grown. The concentration of said carbon and/or nitrogen-containing gas is comprised between 50 and 300 sccm.

As a result, a first portion 2a of polysilicon including carbon and/or nitrogen is obtained on the monocrystalline substrate 1. The thickness of this first portion 2a is
35 comprised between 10 and 200 nm.

According to an embodiment, the growth of polysilicon along with introduction of the carbon and/or nitrogen-containing gas can be pursued until obtaining the final polysilicon

layer having a thickness between 200 and 1000 nm. In such case, the whole polysilicon layer includes carbon and/or nitrogen (FIG. 4B, left).

According to an alternative embodiment, the introduction of the carbon and/or nitrogen-containing gas is stopped after formation of the first portion 2a and the growth of
 5 a second portion 2b of carbon and/or nitrogen-free polysilicon is pursued until obtaining a total thickness of the polysilicon layer 2 from 20 to 500 nm (FIG. 4B, right). The advantage of this embodiment is that the quantity of carbon introduced in the reactor is limited and that dirtying of the reactor walls by carbon is thus minimized. Thus, the reactor requires less cleaning than in the previous embodiment.

10 Then, the monocrystalline substrate covered with the polysilicon layer is taken from the reactor.

On the other hand, as shown in FIG. 4C, a donor substrate 30 comprising a layer 3 intended to form the active layer of the structure is provided. The layer 3 can be delimited in the donor substrate 3 for example by a weakness zone 31. The weakness zone can be
 15 formed by implantation of species or by any other suitable process. These techniques are known *per se* and do not need to be described in more detail here.

A dielectric layer may be formed on the polysilicon layer and/or on the active layer of the donor substrate. For instance, said dielectric layer can be obtained by an oxidation of the polysilicon layer and/or of the donor substrate. By way of example, such a dielectric
 20 layer 4 is illustrated on the active layer 3 of the donor substrate 30 in FIG. 4C. When dielectric layers are formed on both the polysilicon layer and of the donor substrate, both dielectric layers form together, after bonding, a buried dielectric layer.

Then, as shown in FIG. 4D, the monocrystalline substrate 1 and the donor substrate 30 are bonded such that the polycrystalline silicon layer 2 and the active layer 3 (or, if
 25 appropriate, the dielectric layer(s) present on layers 2 and/or 3) are at the bonding interface.

A thermal treatment is carried out to reinforce the bonding strength. The temperature of this thermal treatment is typically comprised between 100 and 1250°C and its duration generally ranges from 10 seconds to 2 hrs.

30 The thermal budget of such a treatment would be sufficient to induce recrystallization of a polysilicon layer from the interface with the monocrystalline substrate that forms a seed for recrystallization. However, due to the presence of carbon atoms in at least the portion 2a of the polysilicon layer in contact with the monocrystalline substrate 1, the recrystallization kinetics is substantially slowed down since the carbon atoms block the
 35 grain boundaries of the polysilicon. Thus, even with a thickness of carbon and/or nitrogen-containing polysilicon region as small as about 100 nm, the polysilicon layer 2 will not recrystallize completely at the end of the thermal treatment.

Then, the active layer 3 is transferred onto the monocrystalline substrate 1 and polysilicon layer 2 by removing the remainder 32 of the donor substrate 30. Said removal can be carried out by fracturing the donor substrate along the weakness zone 31 (Smart Cut™ process), or by etching and/or grinding the donor substrate so as to leave only the active layer 3.

The resulting structure is shown in FIG. 2 (in the case of a polysilicon layer containing carbon and/or nitrogen on its whole thickness) or in FIG. 3 (in the case where only the first portion of the polysilicon layer includes carbon and/or nitrogen).

In such a structure, the polysilicon layer 2 has a thickness of between 200 to 1000 nm (or even from 10 to 500 nm in the situation depicted with reference to FIG. 3), which provides, at the surface opposite to the monocrystalline substrate, a greater number of grain boundaries than in a thicker layer 2' as in FIG. 1. As a result, said polysilicon layer traps more efficiently the electrical charges present at said surface than a thicker layer.

In addition, since the polysilicon layer 2 is thinner as layer 2' in FIG. 1, it is also less rough and thus requires less polishing before bonding to the donor substrate. As a result, a smaller loss of material due to polishing is to be taken into account when forming the polysilicon layer.

REFERENCES

WO 2012/127006

D. Lederer, R. Lobet and J.-P. Raskin, "Enhanced high resistivity SOI wafers for RF applications," *IEEE Intl. SOI Conf.*, pp. 46-47, 2004

D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 805-807, 2005

D. Lederer and J.-P. Raskin, "RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate", *IEEE Transactions on Electron Devices*, vol. 55, no. 7, pp. 1664-1671, 2008

D. C. Kerr et al., "Identification of RF harmonic distortion on Si substrates and its reduction using a trap-rich layer", 978-1-4244-1856-5/08, IEEE 2008 IEEE.

CLAIMS

1. Structure for radiofrequency applications comprising:
 - a monocrystalline substrate,
 - 5 - a polycrystalline silicon layer directly on the monocrystalline substrate,
 - an active layer on the polycrystalline silicon layer, intended to receive radiofrequency components,

characterized in that at least a first portion of the polycrystalline silicon layer extending from the interface of the polycrystalline silicon layer with the monocrystalline

 - 10 layer includes carbon and/or nitrogen atoms located at the grain boundaries of the polycrystalline silicon, in a concentration comprised between 2% and 20%.
-
2. Structure according to claim 1, wherein the whole polycrystalline silicon layer contains carbon and/or nitrogen atoms.
 - 15
-
3. Structure according to claim 2, wherein the thickness of the polycrystalline silicon layer ranges from 200 to 1000 nm.
-
4. Structure according to one of claims 1 to 3, wherein the polycrystalline silicon
 - 20 layer further comprises, on the first portion containing carbon and/or nitrogen atoms, a second portion free from carbon and/or nitrogen atoms in that the concentration in carbon and/or nitrogen in the second portion is less than 0.5%.
-
5. Structure according to claim 4, wherein the thickness of the first portion of the
 - 25 polycrystalline silicon layer ranges from 10 to 200 nm.
-
6. Structure according to one of claims 4 to 5, wherein the thickness of the polycrystalline silicon layer ranges from 20 to 500 nm.
-
7. Structure according to one of claims 1 to 6, wherein the monocrystalline
 - 30 substrate comprises at least one of: monocrystalline silicon having an electrical resistivity greater than 500 Ohm.cm, silicon carbide, and/or germanium.
-
8. Structure according to one of claims 1 to 7, wherein the active layer comprises
 - 35 at least one of: a semiconducting material, a dielectric material, a ferroelectric material, and a substructure comprising at least one cavity and at least one suspended element on said cavity.

9. Structure according to one of claims 1 to 8, wherein said structure further comprises a dielectric layer on the polycrystalline silicon layer, the active layer being on said dielectric layer.

- 5 10. Process for manufacturing a structure for radiofrequency applications, comprising:
- providing a monocrystalline substrate,
 - depositing, on said monocrystalline substrate, a polycrystalline silicon layer,
 - providing a donor substrate comprising an active layer intended to receive
- 10 radiofrequency components,
- bonding the monocrystalline substrate and the donor substrate such that the polycrystalline silicon layer and the active layer are at the bonding interface,
 - transferring the active layer onto the monocrystalline substrate and the polycrystalline silicon layer,
- 15 said process being characterized in that during deposition of at least a first portion of the polycrystalline silicon layer located at the interface with the monocrystalline substrate, carbon and/or atoms are deposited in said first portion.

11. Process according to claim 10, wherein the polycrystalline silicon layer is

20 deposited by Low-Pressure Chemical Vapor Deposition (LPCVD) in a reactor.

12. Process according to claim 11, wherein a gas containing carbon and/or nitrogen atoms is introduced in the LPCVD reactor to form at least the first portion.

25 13. Process according to one of claim 12, wherein said gas is introduced in the LPCVD reactor during the deposition of the whole polycrystalline silicon layer.

14. Process according to claim 13, wherein the thickness of the polycrystalline silicon layer ranges from 200 to 1000 nm.

30

15. Process according to claim 12, wherein after the first portion has been deposited, the process comprises stopping the introduction of the gas containing the carbon and/or nitrogen atoms in the LPCVD reactor and further depositing a carbon and/or nitrogen-free second portion of the polycrystalline layer, the concentration in

35 carbon and/or nitrogen in the second portion being less than 0.5%.

16. Process according to claim 15, wherein the thickness of the first region of the polycrystalline silicon layer ranges from 10 to 200 nm.

17. Process according to one of claims 10 to 16, wherein said process further comprises forming a dielectric layer on the polycrystalline silicon layer and/or on the active layer of the donor substrate.