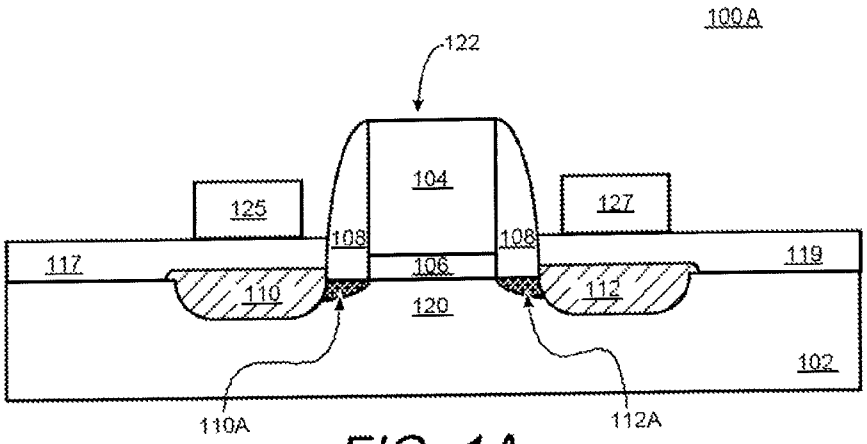


FIG. 1A

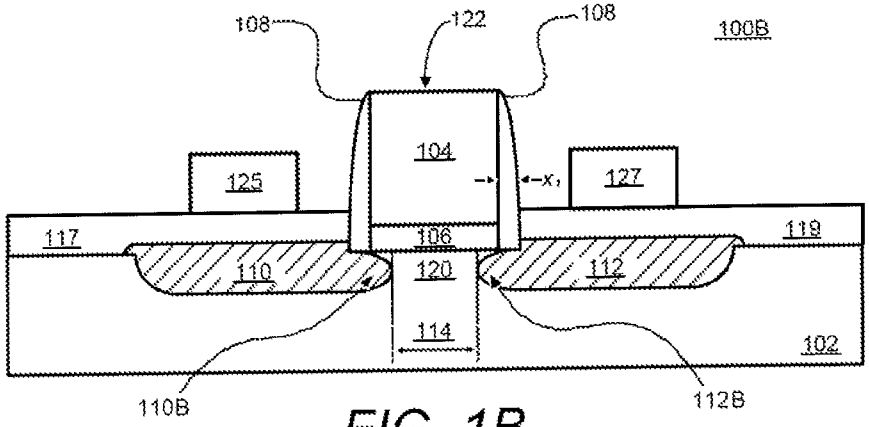


FIG. 1B

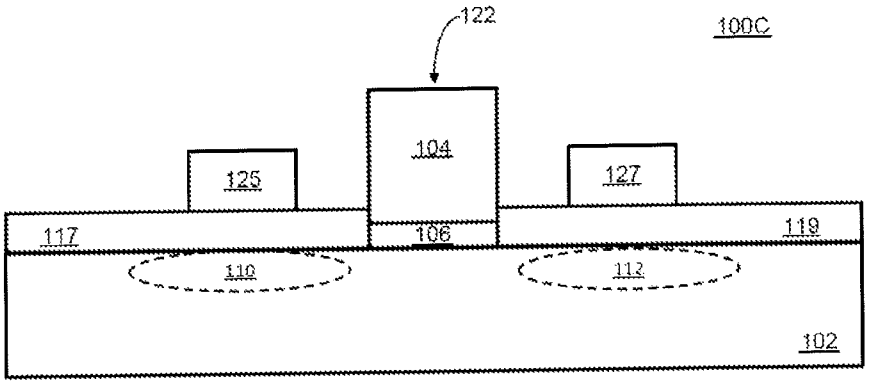


FIG. 1C

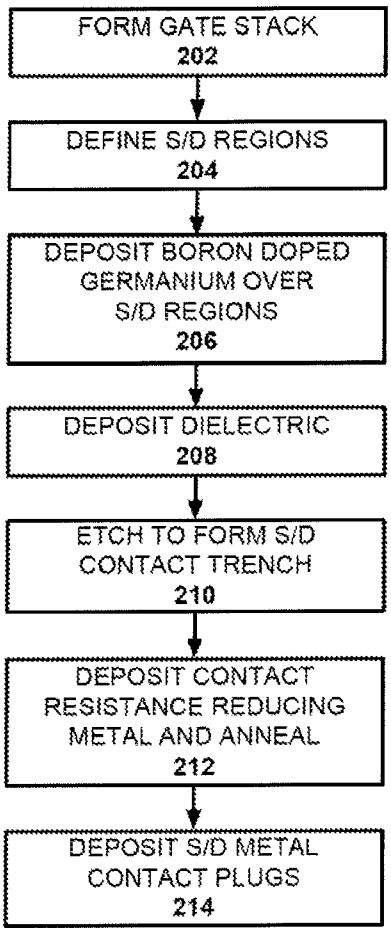

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

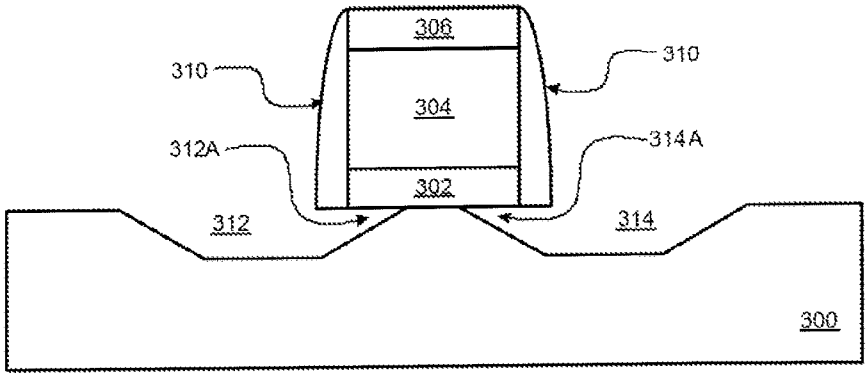


FIG. 3A

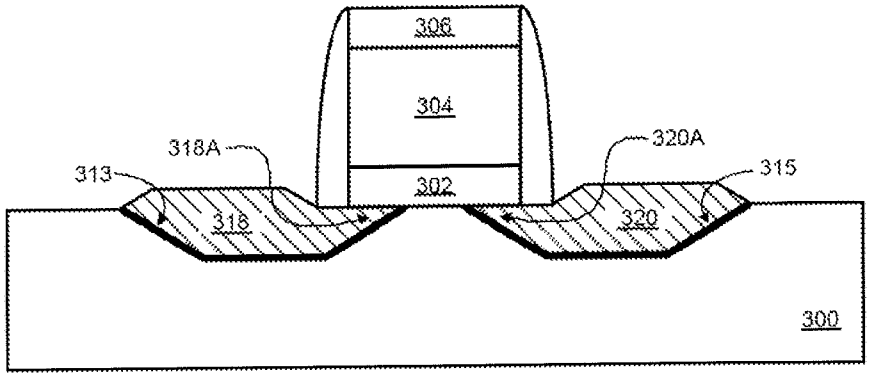


FIG. 3B

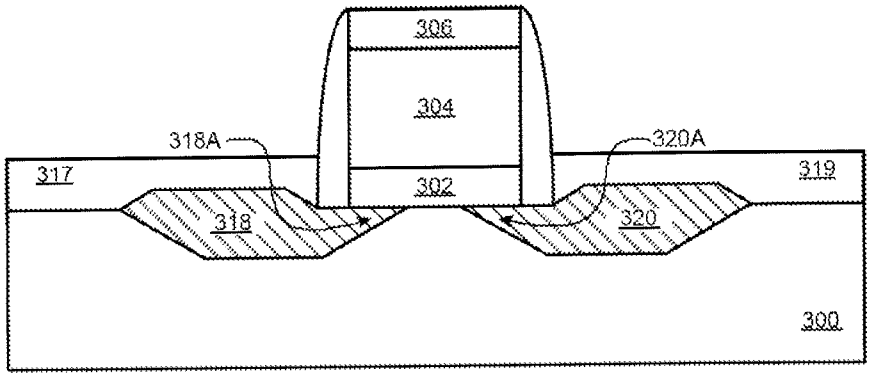


FIG. 3C

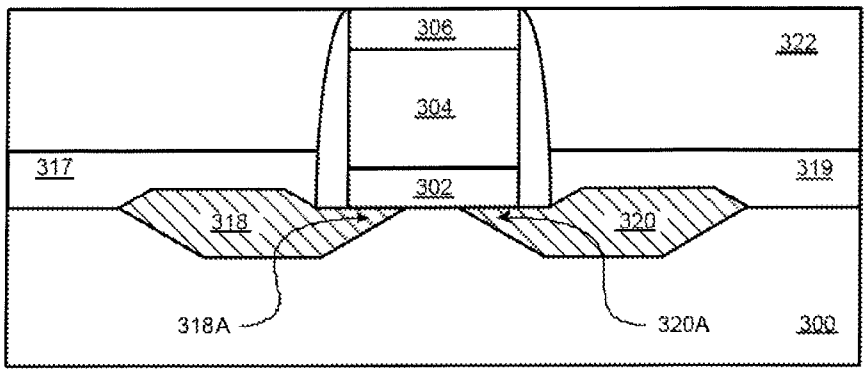


FIG. 3D

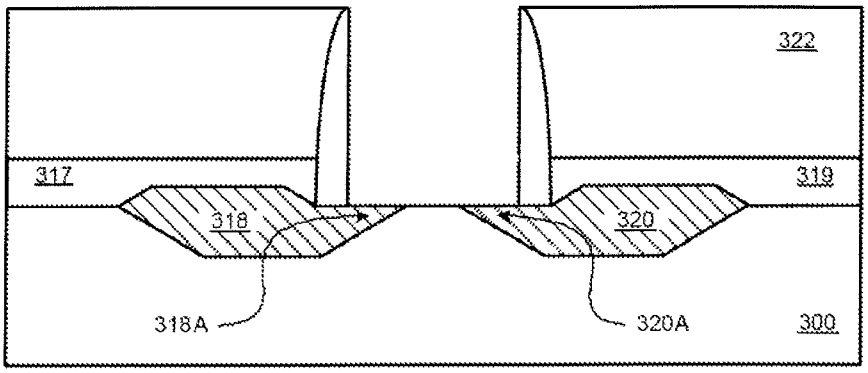


FIG. 3E

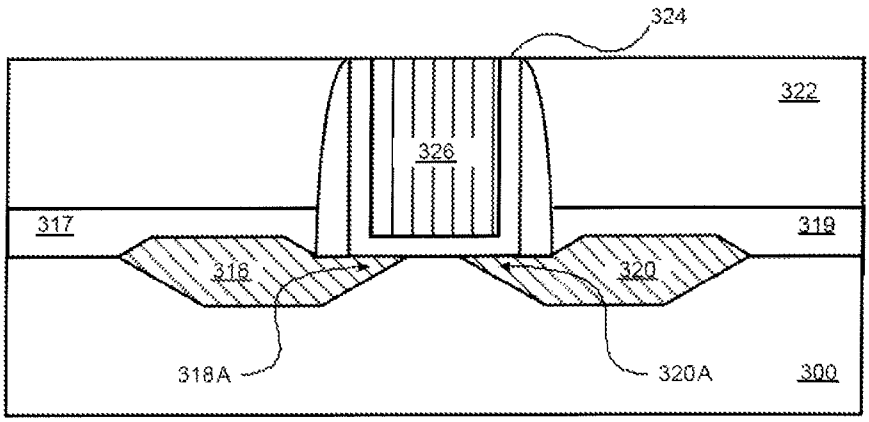


FIG. 3F

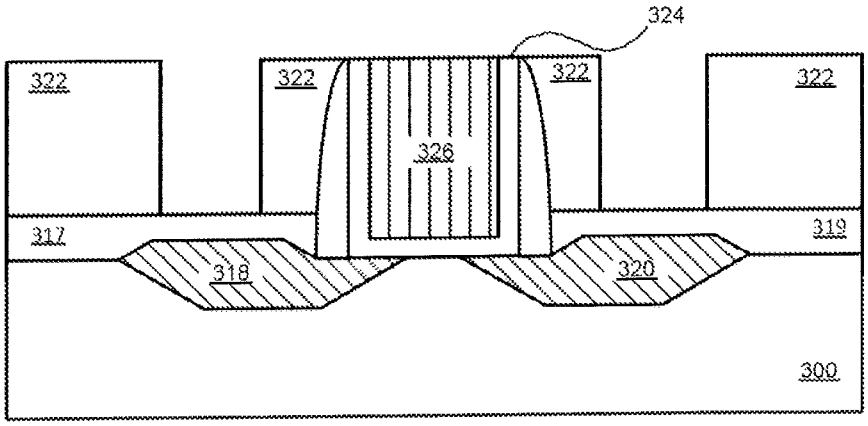


FIG. 3G

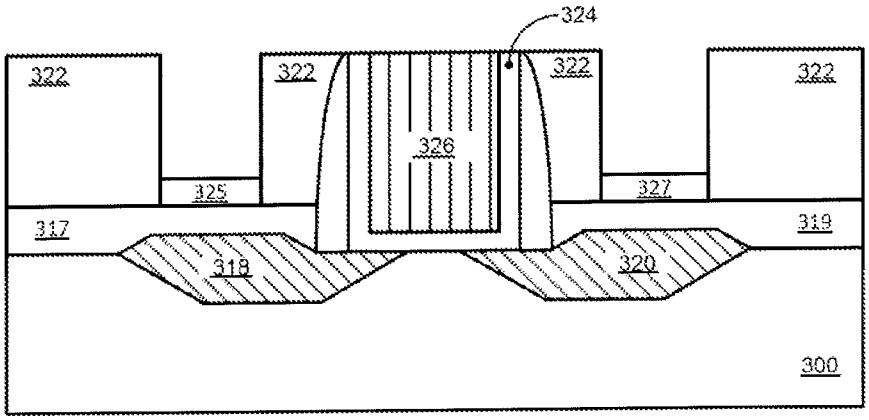


FIG. 3H

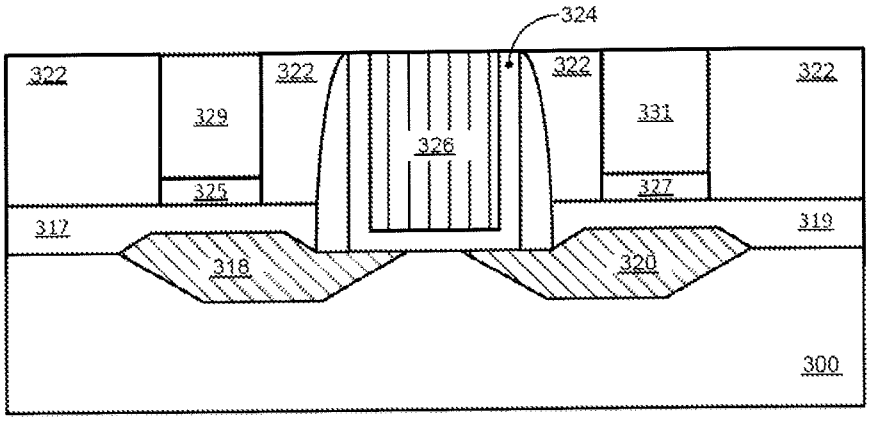


FIG. 3I

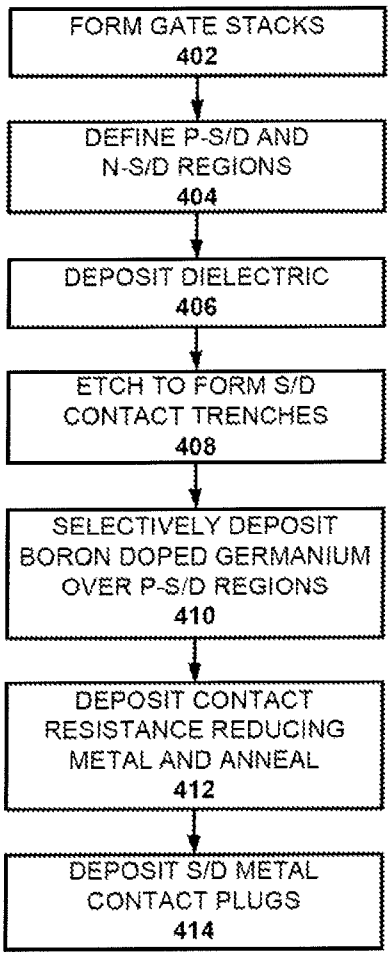

FORM GATE STACKS
402
DEFINE P-S/D AND N-S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCHES
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER P-S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

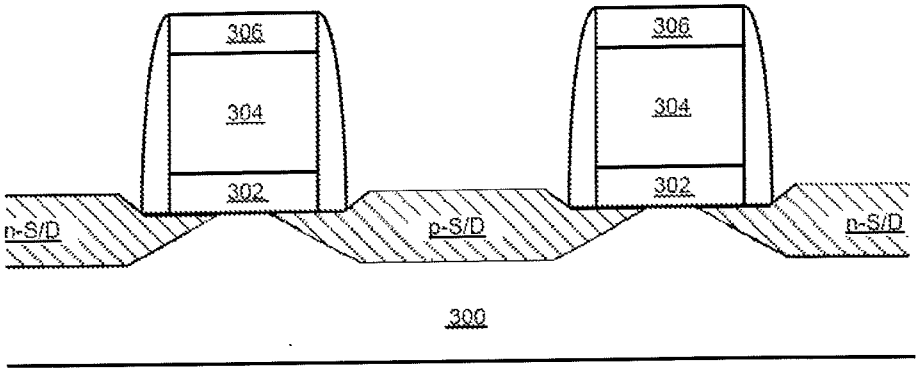


FIG. 5A

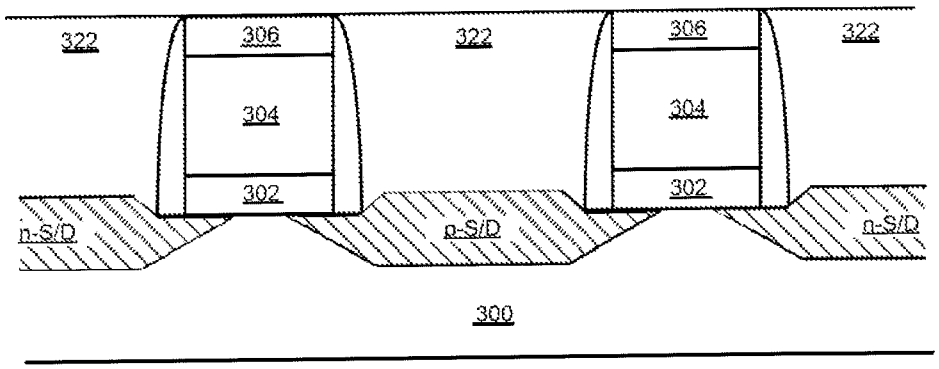


FIG. 5B

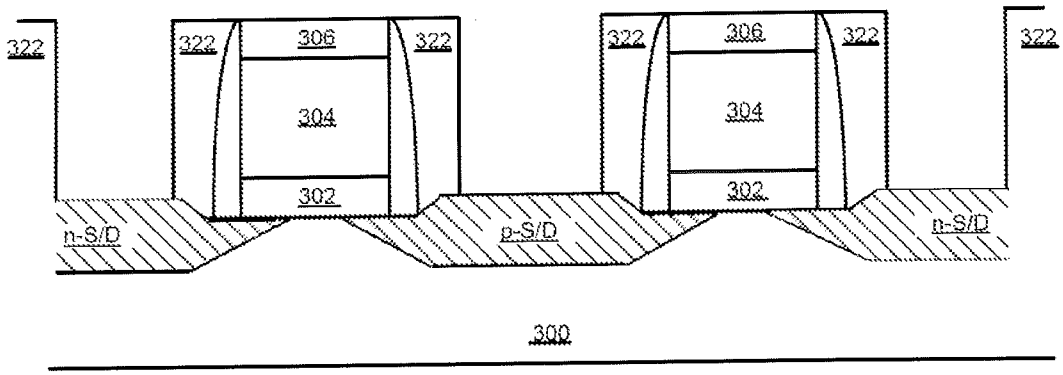


FIG. 5C

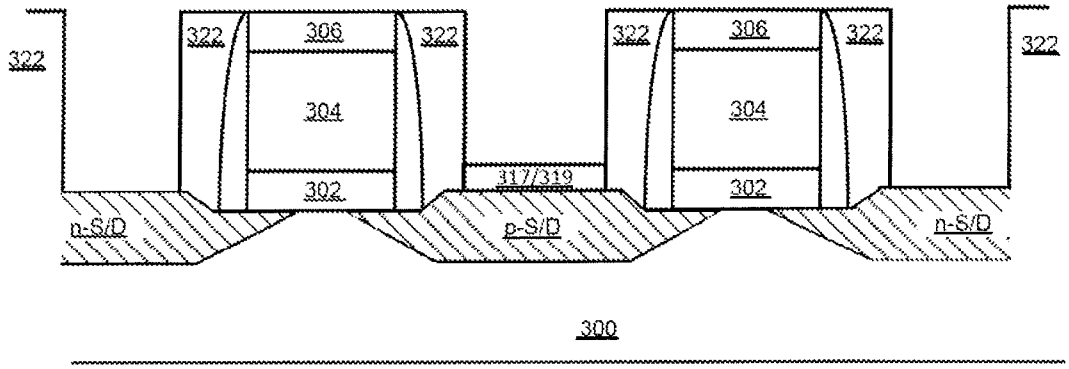


FIG. 5D

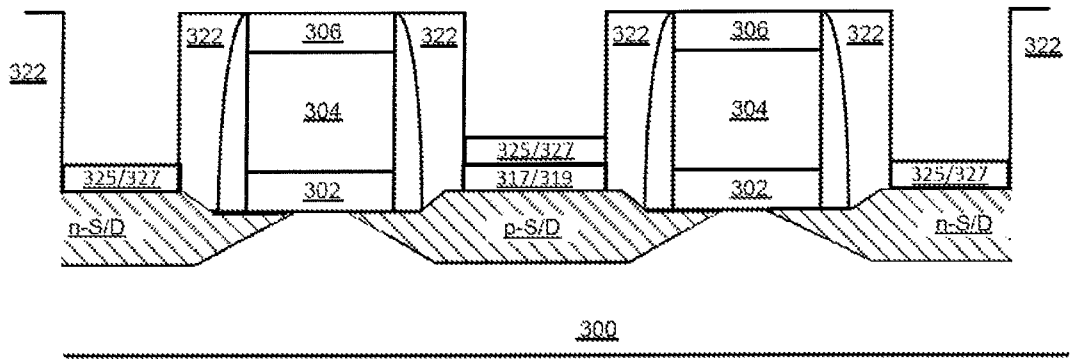


FIG. 5E

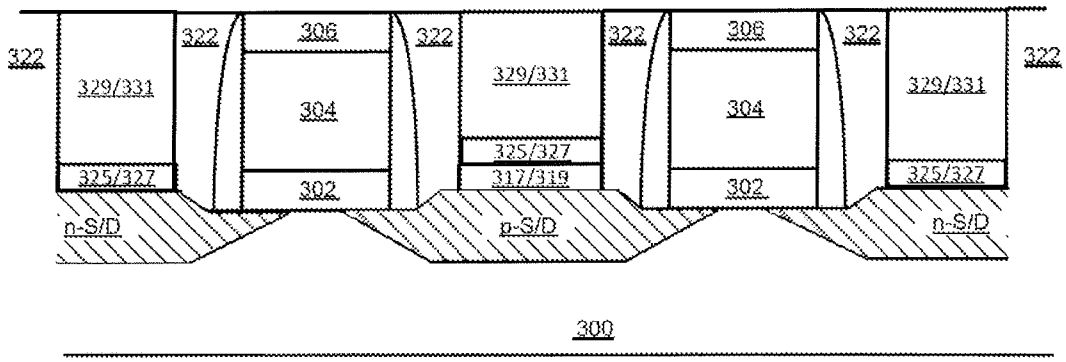


FIG. 5F

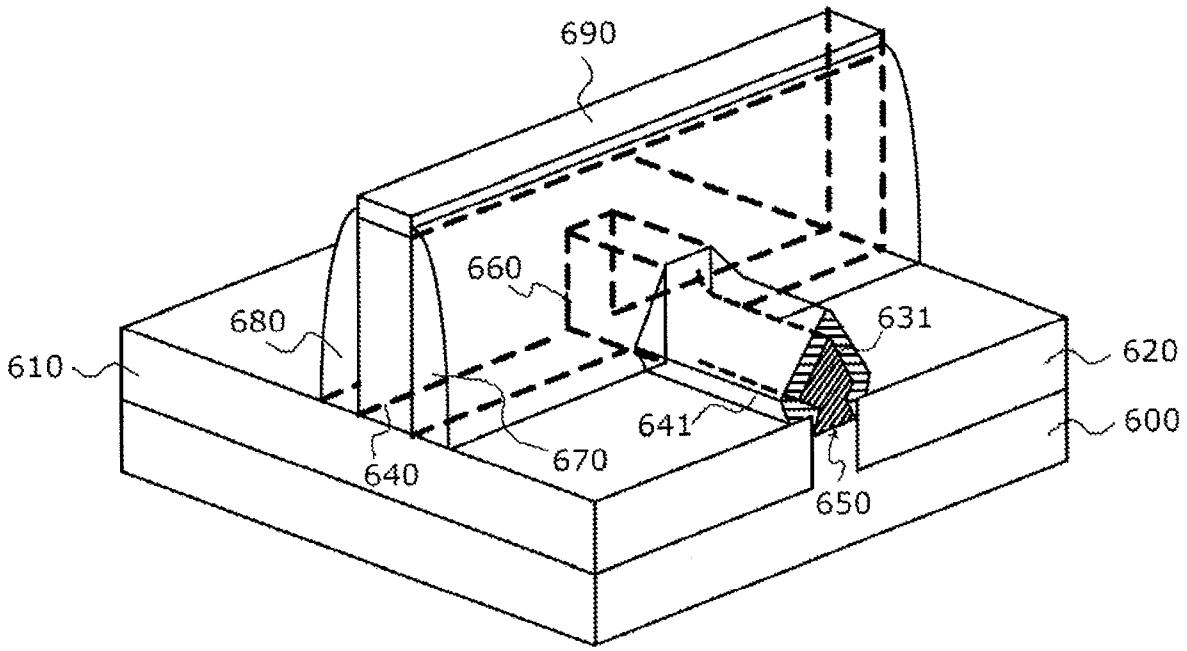


FIG. 6

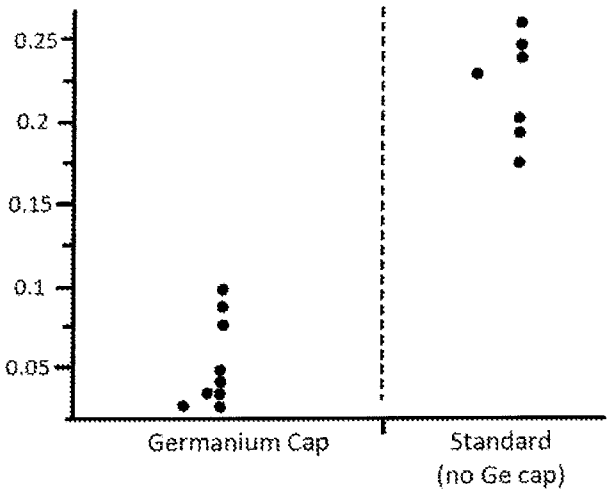


FIG. 7

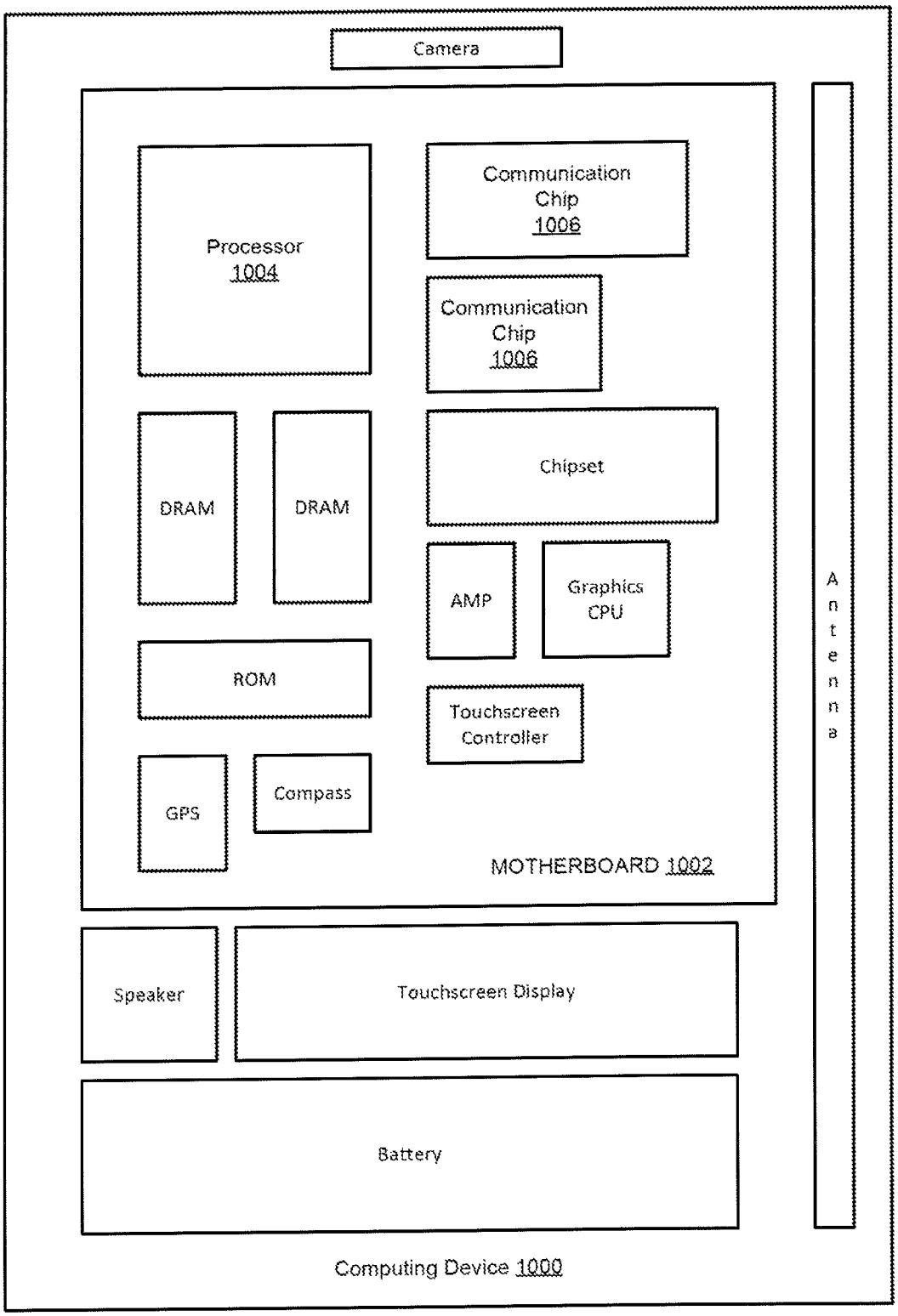

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8