

## Description

This invention relates to a vertical deflection circuit with service mode capability.

To manually adjust the color temperature in a television receiver or a video display apparatus, various circuits in the television receiver are disabled, including the vertical deflection circuit. The vertical deflection circuit is disabled in order to collapse the raster into a single horizontal line. A service switch, that may operate under control of a microcomputer may be used to disable the vertical deflection circuit for preventing the generation of vertical deflection current (see e.g. US-A-4 694 226).

A typical vertical deflection circuit may include a push-pull output stage, and a vertical deflection winding interposed between the output stage and a DC blocking capacitor. During normal operation, a DC voltage is developed in the DC blocking capacitor. The DC voltage in the DC blocking capacitor is controlled in a DC feedback loop and is used for energizing an AC vertical sawtooth generator that generates a sawtooth output signal. The sawtooth signal is coupled to an input terminal of the push-pull output stage.

In accordance with a feature of the invention, a service mode circuit arrangement is provided that maintains the DC blocking capacitor charged during service mode of operation. Maintaining the DC blocking capacitor so charged may be desirable so as to reduce loading of the power supply by the large blocking capacitance during a transition from operation in service mode to operation in normal mode. Excessive loading of the power supply by the capacitor during such transition may cause squегging to occur in certain types of power supplies, disadvantageously, resulting in a disturbed picture on a cathode ray tube (CRT) of the television receiver.

The output stage includes first and second output amplifiers coupled to the vertical deflection winding at an output terminal in a push-pull arrangement. The first and second output amplifiers are respectively coupled to a source of supply voltage and to a common potential, which may be referred to as ground.

In accordance with another feature of the invention, the vertical sawtooth voltage generator includes a second capacitor having a first terminal that is coupled to the DC blocking capacitor. A second terminal of the second capacitor is coupled to ground via a series arrangement of a resistor and a service mode switch when the service mode switch is conductive. During the service mode of operation, the service mode switch that is nonconductive prevents the charging of the second capacitor. The sawtooth signal developed between

the resistor and the second capacitor is coupled to a driver stage for driving the output stage at a vertical rate in a sawtooth manner to generate a sawtooth vertical deflection current and establish a DC operating voltage level in the DC blocking capacitance that is coupled to the output terminal. A DC feedback controls the DC operating voltage in the DC blocking capacitance. Advantageously, the DC feedback loop operates during the service mode so as to maintain the DC blocking capacitor charged.

In accordance with a further feature of the invention, the sawtooth generator includes a second switch operating at a vertical rate during both the normal and service modes of operation. The second switch that is coupled across the second capacitance maintains the frequency response of an AC feedback loop in the deflection circuit substantially the same during both modes of operation. Therefore, advantageously, the frequency response, once optimized for normal mode of operation, is unlikely to cause instability in the AC feedback loop during the service mode of operation.

In accordance with an aspect of the invention, a vertical deflection circuit of a video display apparatus that has normal and service modes of operation includes a vertical deflection winding and an amplifier responsive to a sawtooth signal generated in a sawtooth generator. The amplifier includes a driver stage that is coupled to the deflection winding for generating, during normal operation, a sawtooth deflection current in the deflection winding. The sawtooth signal generator includes a source of a first voltage developed during the normal and during the service modes of operation. It includes a first capacitance coupled to the source of the first voltage. It also includes a source of a first control signal at a frequency that is related to a deflection frequency. A first switch of the sawtooth generator is responsive to the first control signal and coupled to the first capacitance. The first switch operates at a frequency that is related to that of the first control signal during both the normal mode of operation and the service mode operation. The first switch discharges in the normal mode of operation, the first capacitance during a first portion of a given period of the first control signal. A second control signal has a first state that is indicative when the normal mode of operation is required and a second state when the service mode of operation is required. A controllable impedance responsive to the second control signal and coupled via the first capacitance to the source of the first voltage provides, in the normal mode of operation, a current path to a current that charges the first capacitance during a second portion of the given period. The sawtooth signal is produced at a second terminal of the first capacitance. The con-

trollable impedance decouples the current path from the second terminal of the first capacitance when the second control signal is at the second, service mode operation state to prevent the charging of the first capacitance for preventing the generation of the sawtooth signal and the deflection current.

In the Drawing:

The sole FIGURE illustrates a vertical deflection circuit with service mode operation, embodying the invention.

In the illustrated vertical deflection circuit 20 for a television receiver or a video display apparatus, a vertical deflection winding  $L_V$  is coupled to a vertical amplifier output stage 21 at an output terminal A. A current sampling resistor R8 is coupled to deflection winding  $L_V$  at a terminal C, and a DC blocking and S-shaping capacitor  $C_V$  is coupled to resistor R8 at a terminal D.

Vertical amplifier output stage 21 includes a top amplifier transistor Q4 coupled to a +25V DC supply via a diode D2 and a bottom amplifier transistor Q3 coupled to a ground reference potential point through a resistor. A driver stage 22 is coupled to output stage 21 for driving the output stage at a vertical rate in a sawtooth manner to generate a sawtooth vertical deflection current  $i_V$  in vertical deflection winding  $L_V$ .

Driver stage 22 includes an inverting amplifier, driver transistor Q2, and a current source 23 coupled to the collector of the transistor. Driver transistor Q2 drives top output transistor Q4 via a noninverting buffer transistor Q5 and drives bottom output transistor Q3 via an inverting stage U1 and a noninverting buffer transistor Q6. The driver and output stages may be incorporated into an integrated circuit, IC 1, such as the LA7831, manufactured by Sanyo Corporation.

To generate a vertical sawtooth current  $i_V$  in vertical deflection winding  $L_V$ , a vertical ramp generator 26 generates a vertical ramp generating voltage 27 that is AC coupled by a capacitor C2 to the base of an error amplifier transistor Q1. Error amplifier transistor Q1 inverts vertical ramp voltage 27 to develop a vertical input voltage 28 across a collector load resistor R1 of transistor Q1. Input voltage 28 is applied to an input terminal B of driver stage 22 that is coupled to the base of inverting amplifier transistor Q2 via a resistor R27.

Vertical input voltage 28 progressively increases the conduction of transistor Q2 during the vertical trace interval, progressively shunting more of current  $I_1$ , developed by current source 23, away from top output amplifier portion Q5 and Q4. During the first half of trace, output transistor Q4 is conducting, to couple the +25V supply to vertical deflection winding  $L_V$  via diode D2. A decreasing vertical deflection current  $i_V$  flows in deflection

winding  $L_V$  and charges DC blocking capacitor  $C_V$  from the +25V supply via transistor Q4.

During the second half of vertical trace, driver transistor Q2 has been made sufficiently conductive by input voltage 28 to turn off top output transistor Q4 and turn on bottom output transistor Q3. DC blocking capacitor  $C_V$  discharges to ground via vertical deflection winding  $L_V$  and transistor Q3, thereby generating the negative sawtooth portion of vertical deflection current  $i_V$ .

To initiate the vertical retrace interval, input voltage 28 turns off driver transistor Q2, thereby turning off bottom output transistor Q3 and turning on top output transistor Q4. Conventional vertical retrace circuitry, not illustrated in the FIGURE, provides for the retrace of vertical deflection current  $i_V$ .

The operation of output stage 21 in response to vertical input voltage 28, develops a vertical output voltage 29 at output terminal A that is applied to vertical deflection winding  $L_V$ . The DC level,  $V_0$ , established at output terminal A, also establishes substantially the same DC level at terminals C and D. Vertical deflection current  $i_V$  generates an AC sawtooth voltage between terminals C and D, across sampling resistor R8, and generates a parabolic component 30 to the voltage  $V_0$  developed across DC blocking capacitor  $C_V$ .

A DC negative feedback loop from output terminal A to input terminal B stabilizes the average DC operating voltage level at terminal A. The DC voltage at terminal A is coupled via terminal C to the emitter of error amplifier transistor Q1 to establish the DC voltage of the emitter at voltage level  $V_0$ . Voltage level  $V_0$  is compared with a reference voltage level  $V_r$ , that is developed at the base of transistor Q1 by voltage dividing resistors R9, R101 and R10. The level of input voltage 28 is controlled by the conduction of transistor Q1 for stabilizing the DC voltage level  $V_0$  at an operating level that is approximately  $1V_{be}$  above reference voltage level  $V_r$ .

AC negative feedback for scan linearization is provided by coupling the AC sawtooth voltage developed across sampling resistor R8 to the emitter of error transistor Q1 via a voltage dividing network comprising potentiometer R12 and resistors R14 and R15. The AC sawtooth voltage at the emitter of error transistor Q1 is compared with vertical ramp generating voltage 27 that is AC coupled to the base of the transistor in order to develop the AC component of input voltage 28. Deflection current amplitude is adjusted by adjusting the wiper arm of potentiometer R12.

Ramp generator 26, that develops vertical ramp generating voltage 27, comprises an RC integrating network, capacitor C1 and a resistor R11. During normal operation, resistor R11 has a terminal that is coupled to ground via a collector of a

transistor Q9 that is conductive during normal operation. A reset switch, transistor Q7, is coupled across capacitor C1. Voltage  $V_D$  developed across DC blocking capacitor  $C_V$  is applied to the integrating network of capacitor C1 and resistor R11. The DC component of voltage  $V_D$  is integrated by capacitor C1 to generate a downwardly-going ramp of voltage across resistor R11. The AC, parabolic component of voltage  $V_D$  is integrated by capacitor C1 to provide S-shaping of the ramp voltage across resistor R11.

To initiate vertical retrace, ramp capacitor C1 is discharged by making reset transistor Q7 conductive. A vertical reset pulse 36, generated by vertical synchronization circuitry not illustrated in the FIGURE, is applied to the base of a transistor Q8, making the transistor nonconductive during the short reset pulse interval. The collector of transistor Q8 is coupled to a +44V supply by a resistor R16. The collector of transistor Q8 is DC coupled to the base of reset transistor Q7 via a resistor R18. Negative going reset pulse 36 is inverted by transistor Q8 and applied to the base of transistor Q7, to turn transistor Q7 on and discharge capacitor C1. The sharp increase in ramp voltage 27 when capacitor C1 is discharged is coupled to the base of error amplifier transistor Q1 and turns the transistor off to initiate the vertical retrace interval.

A capacitor C5 in series with a resistor R19 across deflection winding  $L_V$  damps deflection winding resonances. A resistor R7 is coupled between output terminal A and the emitter of error amplifier transistor Q1 to compensate for horizontal rate pickup by vertical deflection winding  $L_V$ . A capacitor C6 in series with a resistor R20 is coupled between input terminal B and ground to roll off the gain at higher frequencies, to prevent deflection circuit high frequency oscillation.

During service mode operation of the television receiver which is used, for example, when color temperature is to be manually adjusted, or when degaussing is required, the raster is collapsed vertically by disabling vertical deflection circuit 20.

In accordance with a feature of the invention, a service mode switching circuit 50 disables the generation of vertical deflection current when the service mode of operation is asserted. Service mode switching circuit 50 includes service mode switching transistor Q9 having its collector coupled to a terminal of resistor R11 that is remote from the junction between capacitors C2 and C1. A resistor R100 is coupled between terminal D of capacitor  $C_V$  and the collector of transistor Q9. The emitter of transistor Q9 is coupled to ground.

During the normal mode of television receiver operation, a mode-switching signal 25, that may be conventionally generated, is in the high state, maintaining transistor Q9 in saturated conduction.

Therefore, ramp generator 26 operates in the manner described before.

To assert the service mode of television receiver operation, mode-switching signal 25 is switched to the low state to cutoff conduction in transistor Q9. With transistor Q9 cutoff, the current path via resistor R11 for charging capacitor C1 is opened. Therefore, capacitor C1 can no longer be charged and the plate of capacitor C2 that is coupled to capacitor C1 will be at the level of voltage  $V_D$ . Consequently, generation of ramp voltage 27 ceases. Resistor R100 prevents leakage current from charging capacitor C1.

Due to the DC negative feedback provided by resistors R14, R15 and R12, the DC voltage at each of terminals A, C and D will be maintained at approximately +12.5 volts, that is approximately equal to reference voltage level  $V_r$  plus one  $V_{be}$  voltage of transistor Q1.

Therefore, in accordance with an aspect of the invention, capacitor  $C_V$  will be maintained charged to approximately +12.5 volts during service mode of operation by the operation of transistor Q9. Consequently, when normal mode of operation is resumed, the transient supply current via diode D2 is advantageously smaller than if capacitor  $C_V$  were not already charged.

In accordance with another aspect of the invention, an AC feedback-loop path between the input and output of IC 1 includes capacitor C1 in parallel with switching transistor Q7. Because transistor switch Q7 operates during both the normal and service modes of operation, the frequency response characteristic of the feedback loop is substantially the same in both modes of operations. Therefore, advantageously, the frequency response characteristic once optimized for normal mode of operation, is unlikely to cause instability in the AC feedback-loop during the service mode of operation. Had the AC feedback-loop been unstable during the service mode of operation, an AC signal might have been generated that might have caused a disturbance in the vertical direction in the raster on the CRT screen.

## Claims

1. A vertical deflection circuit of a video display apparatus having normal and service modes of operation, comprising:
  - a vertical deflection winding ( $L_V$ );
  - an amplifier (IC1) responsive to a sawtooth signal (27) and having a driver stage (22) that is coupled to said deflection winding ( $L_V$ ) for generating, during normal operation, a sawtooth deflection current ( $I_V$ ) in said deflection winding ( $L_V$ );
  - a sawtooth signal generator (26) for gen-



transistor Q9 that is conductive during normal operation. A reset switch, transistor Q7, is coupled across capacitor C1. Voltage  $V_D$  developed across DC blocking capacitor  $C_V$  is applied to the integrating network of capacitor C1 and resistor R11. The DC component of voltage  $V_D$  is integrated by capacitor C1 to generate a downwardly-going ramp of voltage across resistor R11. The AC, parabolic component of voltage  $V_D$  is integrated by capacitor C1 to provide S-shaping of the ramp voltage across resistor R11.

To initiate vertical retrace, ramp capacitor C1 is discharged by making reset transistor Q7 conductive. A vertical reset pulse 36, generated by vertical synchronization circuitry not illustrated in the FIGURE, is applied to the base of a transistor Q8, making the transistor nonconductive during the short reset pulse interval. The collector of transistor Q8 is coupled to a +44V supply by a resistor R16. The collector of transistor Q8 is DC coupled to the base of reset transistor Q7 via a resistor R18. Negative going reset pulse 36 is inverted by transistor Q8 and applied to the base of transistor Q7, to turn transistor Q7 on and discharge capacitor C1. The sharp increase in ramp voltage 27 when capacitor C1 is discharged is coupled to the base of error amplifier transistor Q1 and turns the transistor off to initiate the vertical retrace interval.

A capacitor C5 in series with a resistor R19 across deflection winding  $L_V$  damps deflection winding resonances. A resistor R7 is coupled between output terminal A and the emitter of error amplifier transistor Q1 to compensate for horizontal rate pickup by vertical deflection winding  $L_V$ . A capacitor C6 in series with a resistor R20 is coupled between input terminal B and ground to roll off the gain at higher frequencies, to prevent deflection circuit high frequency oscillation.

During service mode operation of the television receiver which is used, for example, when color temperature is to be manually adjusted, or when degaussing is required, the raster is collapsed vertically by disabling vertical deflection circuit 20.

In accordance with a feature of the invention, a service mode switching circuit 50 disables the generation of vertical deflection current when the service mode of operation is asserted. Service mode switching circuit 50 includes service mode switching transistor Q9 having its collector coupled to a terminal of resistor R11 that is remote from the junction between capacitors C2 and C1. A resistor R100 is coupled between terminal D of capacitor  $C_V$  and the collector of transistor Q9. The emitter of transistor Q9 is coupled to ground.

During the normal mode of television receiver operation, a mode-switching signal 25, that may be conventionally generated, is in the high state, maintaining transistor Q9 in saturated conduction.

Therefore, ramp generator 26 operates in the manner described before.

To assert the service mode of television receiver operation, mode-switching signal 25 is switched to the low state to cutoff conduction in transistor Q9. With transistor Q9 cutoff, the current path via resistor R11 for charging capacitor C1 is opened. Therefore, capacitor C1 can no longer be charged and the plate of capacitor C2 that is coupled to capacitor C1 will be at the level of voltage  $V_D$ . Consequently, generation of ramp voltage 27 ceases. Resistor R100 prevents leakage current from charging capacitor C1.

Due to the DC negative feedback provided by resistors R14, R15 and R12, the DC voltage at each of terminals A, C and D will be maintained at approximately +12.5 volts, that is approximately equal to reference voltage level  $V_r$  plus one  $V_{be}$  voltage of transistor Q1.

Therefore, in accordance with an aspect of the invention, capacitor  $C_V$  will be maintained charged to approximately +12.5 volts during service mode of operation by the operation of transistor Q9. Consequently, when normal mode of operation is resumed, the transient supply current via diode D2 is advantageously smaller than if capacitor  $C_V$  were not already charged.

In accordance with another aspect of the invention, an AC feedback-loop path between the input and output of IC 1 includes capacitor C1 in parallel with switching transistor Q7. Because transistor switch Q7 operates during both the normal and service modes of operation, the frequency response characteristic of the feedback loop is substantially the same in both modes of operations. Therefore, advantageously, the frequency response characteristic once optimized for normal mode of operation, is unlikely to cause instability in the AC feedback-loop during the service mode of operation. Had the AC feedback-loop been unstable during the service mode of operation, an AC signal might have been generated that might have caused a disturbance in the vertical direction in the raster on the CRT screen.

## Claims

1. A vertical deflection circuit of a video display apparatus having normal and service modes of operation, comprising:
  - a vertical deflection winding ( $L_V$ );
  - an amplifier (IC1) responsive to a sawtooth signal (27) and having a driver stage (22) that is coupled to said deflection winding ( $L_V$ ) for generating, during normal operation, a sawtooth deflection current ( $i_v$ ) in said deflection winding ( $L_V$ );
  - a sawtooth signal generator (26) for gen-



erating said sawtooth signal (27), said sawtooth signal generator further comprising;

a source ( $C_V$ ) of a first voltage ( $V_D$ ) developed during said normal and during said service modes of operation;

a first capacitance (C1) coupled to said source ( $C_V$ ) of said first voltage;

a source of a first control signal (36) at a frequency that is related to a deflection frequency;

a first switch (Q7) responsive to said first control signal (36) and coupled to said first capacitance (C1), said first switch (Q7) operating at a frequency that is related to that of said first control signal (36) during both said normal mode of operation and said service mode operation, for discharging, in said normal mode of operation, said first capacitance (C1) via said first switch (Q7) during a first portion of a given period of said first control signal (36);

a source of a second control signal (25) having a first state that is indicative when said normal mode of operation is required and a second state when said service mode of operation is required; and

a controllable impedance (Q9) responsive to said second control signal (25) and coupled via said first capacitance (C1) to said source ( $C_V$ ) of said first voltage ( $V_D$ ) for providing, in said normal mode of operation, a current path to a current that charges said first capacitance (C1) during a second portion of said given period to produce said sawtooth signal (27) at a terminal (D) of said first capacitance (C1), and for decoupling said current path from said terminal (D) of said first capacitance (C1) when said second control signal (25) is at said second, service mode operation state to prevent the charging of said first capacitance (C1) for preventing the generation of said sawtooth signal (27) and said deflection current ( $i_V$ ).

2. A circuit according to Claim 1 characterized in that said source of said first voltage ( $V_D$ ) comprises a DC blocking capacitance ( $C_V$ ) that is DC coupled to said driver stage (22) via said deflection winding for developing said first voltage ( $V_D$ ) across said DC blocking capacitance ( $C_V$ ).

3. A circuit according to Claim 2 characterized in that said first voltage ( $V_D$ ) is a DC voltage and wherein said controllable impedance (Q9) provides said current path that conducts a DC current from said DC blocking capacitance ( $V_D$ ) via said first capacitance (C1) during said second portion of said given period in said normal operation.

4. A circuit according to Claim 1 characterized in that said first switch (Q7) is coupled in parallel with said first capacitance (C1) for discharging said first capacitance (C1) therethrough during said first portion of said given period.

5. A circuit according to Claim 1 characterized in that said controllable impedance comprises a second switch (Q9) responsive to said second control signal (25) and a first resistance (R11) coupled in series with said second switch (Q9), said second switch (Q9) being nonconductive in said service mode of operation to prevent said first capacitance (C1) from charging via said first resistance (R11).

6. A circuit according to Claim 5 characterized by, a second resistance (R100) having a first terminal coupled to a junction of said first capacitance (C1) and said source ( $C_V$ ) of said first voltage ( $V_D$ ), said second resistance (R100) having a second terminal that is coupled to a junction terminal between said second switch (Q9) and said first resistance (R11).

7. A circuit according to Claim 1 characterized by, a second DC blocking capacitance (C2) having a first terminal that is coupled to a terminal of said first capacitance (C1) that is remote from said source ( $C_V$ ) of said first voltage ( $V_D$ ) and a second terminal that is coupled to an input terminal of said amplifier (IC1) for coupling said sawtooth signal to said amplifier (IC1).

8. A circuit according to Claim 1 characterized by, a deflection current sampling resistor (R8) coupled to said deflection winding ( $L_V$ ) and an error amplifier (Q1) responsive to said sawtooth signal (27) and to a signal that is developed across said sampling resistor (R8) for generating an AC error signal in accordance with a difference therebetween that is coupled to said input terminal (B) of said amplifier.

9. A circuit according to Claim 1 characterized in that a first terminal (D) of said first capacitance (C1) is coupled to an output terminal (A) of said amplifier (IC1) and a second terminal of said first capacitance (C1) is coupled to an input terminal (B) of said amplifier (IC1) such that an AC feedback signal path from said output to said input terminal of said amplifier (IC1), that includes said first switch (Q7) and said first capacitance (C1), has substantially the same characteristic during both normal and service modes of operation.



## Patentansprüche

1. Vertikalablenkschaltung eines Videoanzeigegerätes mit einer Normal- und einer Einstellungsbetriebsart, umfassend:

eine Vertikalablenkspule ( $L_V$ );  
einen auf ein Sägezahnsignal (27) ansprechenden Verstärker (IC1), der eine Treiberstufe (22) aufweist, die mit der genannten Ablenkspule ( $L_V$ ) verbunden ist, um im Normalbetrieb einen

sägezahnförmigen Ablenkstrom ( $i_V$ ) in der genannten Ablenkspule ( $L_V$ ) zu erzeugen;  
einen Sägezahngenerator (26) zur Erzeugung des genannten Sägezahnsignals (27), wobei der genannte Sägezahngenerator darüber hinaus umfaßt:

eine Quelle ( $C_V$ ) einer ersten Spannung ( $V_D$ ), die im genannten Normalbetrieb und im genannten Einstellungsbetrieb erzeugt wird; einen ersten Kondensator (C1), der mit der genannten Quelle ( $C_V$ ) der genannten ersten Spannung verbunden ist;

eine Quelle eines ersten Steuersignals (36) mit einer Frequenz, die zur Ablenkfrequenz in Beziehung steht;

einen ersten Schalter (Q7), der auf das genannte erste Steuersignal (36) anspricht und mit dem genannten ersten Kondensator (C1) verbunden ist, wobei der genannte erste Schalter (Q7) sowohl im genannten Normalbetrieb, als auch im genannten Einstellungsbetrieb bei einer Frequenz arbeitet, die zu der des genannten ersten Steuersignals (36) in Beziehung steht, um im genannten Normalbetrieb in einem ersten Abschnitt einer betrachteten Periode des genannten ersten Steuersignals (36) den genannten ersten Kondensator (C1) über den genannten ersten Schalter (Q7) zu entladen;

eine Quelle eines zweiten Steuersignals (25), das einen ersten Zustand hat, der maßgeblich ist, wenn der genannte Normalbetrieb eingestellt ist, und einen zweiten Zustand, wenn der genannte Einstellungsbetrieb eingestellt ist; und

eine steuerbare Impedanz (Q9), die auf das genannte zweite Steuersignal (25) anspricht und über den genannten ersten Kondensator (C1) an die genannte Quelle ( $C_V$ ) der genannten ersten Spannung ( $V_D$ ) angeschlossen ist, um in der genannten Normalbetriebsart einem Strom einen Stromweg zu bieten, der den genannten ersten Kondensator (C1) während eines zweiten Abschnitts der genannten betrachteten Periode auflädt, um das genannte Sägezahnsignal (27) an einem Anschluß (D) des genannten ersten Kondensators (C1) zu erzeugen, und um den genannten Stromweg vom

genannten Anschluß (D) des genannten ersten Kondensators (C1) zu entkoppeln, wenn sich das genannte zweite Steuersignal (25) im genannten zweiten, dem Zustand der Einstellungsbetriebsart, befindet, um die Ladung des genannten ersten Kondensators (C1) zu verhindern, um die Erzeugung des genannten Sägezahnsignals (27) und des genannten Ablenkstromes ( $i_V$ ) zu verhindern.

2. Schaltung gemäß Patentanspruch 1, dadurch gekennzeichnet, daß die genannte Quelle der genannten ersten Spannung ( $V_D$ ) einen Gleichspannungssperrkondensator ( $C_V$ ) enthält, der über die genannte Ablenkspule an die genannte Treiberstufe (22) gleichspannungsmäßig angeschlossen ist, um die genannte erste Spannung ( $V_D$ ) über dem genannten Gleichspannungssperrkondensator ( $C_V$ ) zu erzeugen.

3. Schaltung gemäß Patentanspruch 2, dadurch gekennzeichnet, daß die genannte erste Spannung ( $V_D$ ) eine Gleichspannung ist und worin die genannte steuerbare Impedanz (Q9) den genannten Stromweg sicherstellt, der im genannten zweiten Abschnitt der genannten betrachteten Periode im genannten Normalbetrieb einen Gleichstrom vom genannten Gleichspannungssperrkondensator ( $V_D$ ) über den genannten ersten Kondensator (C1) leitet.

4. Schaltung gemäß Patentanspruch 1, dadurch gekennzeichnet, daß der genannte erste Schalter (Q7) zu dem genannten ersten Kondensator (C1) parallel geschaltet ist, um den genannten ersten Kondensator (C1) im genannten ersten Abschnitt der genannten betrachteten Periode durch diesen zu entladen.

5. Schaltung gemäß Patentanspruch 1, dadurch gekennzeichnet, daß die genannte steuerbare Impedanz einen zweiten Schalter (Q9) enthält, der auf das genannte zweite Steuersignal (25) anspricht, und einen ersten Widerstand (R11), der mit dem genannten zweiten Schalter (Q9) in Reihe geschaltet ist, wobei der genannte zweite Schalter (Q9) in der genannten Einstellungsbetriebsart nichtleitend ist, um zu verhindern, daß der genannte erste Kondensator (C1) über den genannten ersten Widerstand (R11) geladen wird.

6. Schaltung gemäß Patentanspruch 5, gekennzeichnet durch einen zweiten Widerstand (R100), dessen erster Anschluß an eine Verbindung des genannten ersten Kondensators (C1) mit der genannten Quelle ( $C_V$ ) der genannten ersten Spannung ( $V_D$ ) verbunden ist, wobei der



genannte zweite Widerstand (R100) einen zweiten Anschluß aufweist, der an einen Verbindungsanschluß zwischen dem genannten zweiten Schalter (Q9) und dem genannten ersten Widerstand (R11) angeschlossen ist.

7. Schaltung gemäß Patentanspruch 1, gekennzeichnet durch einen zweiten Gleichspannungssperrkondensator (C2), der einen ersten Anschluß aufweist, der mit einem Anschluß des genannten ersten Kondensators (C1) verbunden ist, der von der genannten Quelle ( $C_V$ ) der genannten ersten Spannung ( $V_D$ ) entfernt liegt, und einen zweiten Anschluß, der an einen Eingangsanschluß des genannten Verstärkers (IC1) angeschlossen ist, um das genannte Sägezahnsignal an den genannten Verstärker (IC1) anzulegen.

8. Schaltung gemäß Patentanspruch 1, gekennzeichnet durch einen Abtastwiderstand des Ablenkstromes (R8), der an die Ablenkspule ( $L_V$ ) angeschlossen ist, und einen Fehlerverstärker (Q1), der auf das genannte Sägezahnsignal (27) anspricht und auf ein Signal, das über dem genannten Abtastwiderstand (R8) erzeugt wird, um ein Wechselstromfehlersignal in Übereinstimmung mit einem Unterschied dazwischen zu erzeugen, das an den genannten Eingangsanschluß (B) des genannten Verstärkers angelegt wird.

9. Schaltung gemäß Patentanspruch 1, dadurch gekennzeichnet, daß ein erster Anschluß (D) des genannten ersten Kondensators (C1) mit einem Ausgangsanschluß (A) des genannten Verstärkers (IC1) verbunden ist und ein zweiter Anschluß des genannten ersten Kondensators (C1) mit dem Eingangsanschluß (B) des genannten Verstärkers (IC1), derart, daß ein Rückkopplungsweg eines Gleichspannungssignals vom genannten Ausgang zum genannten Eingangsanschluß des genannten Verstärkers (IC1), der den genannten ersten Schalter (Q7) und den genannten ersten Kondensator (C1) einschließt, im wesentlichen denselben Frequenzgang im Normal- und im Einstellungsbetrieb hat.

#### Revendications

1. Circuit de balayage vertical d'un appareil de visualisation vidéo ayant les modes de fonctionnement normal et service comprenant :  
un enroulement de balayage vertical ( $L_V$ ) ;  
un amplificateur (IC1) sensible à un signal en dents de scie (27) et ayant un étage d'excitation (22) qui est couplé à l'enroulement de

balayage ( $L_V$ ) pour générer, pendant le fonctionnement normal, un courant de balayage en dents de scie ( $i_V$ ) dans ledit enroulement de balayage ( $L_V$ ) ;

un générateur de signal en dents de scie (26) pour générer ledit signal en dents de scie (27), ledit générateur de signal en dents de scie comprenant en outre

une source ( $C_V$ ) d'une première tension ( $V_D$ ) formée pendant les modes de fonctionnement mentionnés normal et service ;

un premier condensateur (C1) coupé à ladite source ( $C_V$ ) de ladite première tension ;

une source d'un premier signal de commande (36) à une fréquence qui est en relation avec une fréquence de balayage ;

un premier commutateur (Q7) sensible au premier signal de commande mentionné (36) et couplé au dit premier condensateur (C1), ledit premier commutateur (Q7) fonctionnant à une fréquence qui est en relation avec celle du premier signal de commande mentionné (36) pendant les deux modes de fonctionnement mentionnés, le mode normal et le mode service, pour décharger, dans ledit mode de fonctionnement normal, ledit premier condensateur (C1) par l'intermédiaire du premier commutateur mentionné (Q7) pendant une première portion d'une période donnée du premier signal de commande mentionné (36);

une source d'un second signal de commande (25) ayant un premier état qui est indicatif lorsque ledit mode de fonctionnement normal est requis, et un second état lorsque ledit fonctionnement en mode service est requis et une impédance qui peut être commandée (Q9) sensible au second signal de commande mentionné (25) et couplée, par l'intermédiaire du premier condensateur mentionné (C1) à ladite source ( $C_V$ ) de ladite première tension ( $V_D$ ) pour créer, dans ledit mode de fonctionnement normal, un trajet de courant pour un courant qui charge ledit premier condensateur (C1) pendant une seconde portion de ladite période donnée pour produire ledit signal en dents de scie (27) à une borne (D) du premier condensateur mentionné (C1) et pour découpler ledit trajet de courant de ladite borne (D) du premier condensateur mentionné (C1) lorsque ledit second signal de commande (25) est dans le second état de fonctionnement mentionné, en mode service, pour empêcher de charger le premier condensateur mentionné (C1) pour empêcher la génération du signal en dents de scie mentionné (27) et du courant de balayage mentionné ( $i_V$ ).



2. Circuit selon la revendication 1, caractérisé en ce que ladite source de ladite première tension ( $V_D$ ) comprend un condensateur d'arrêt à courant continu ( $C_V$ ) qui est couplé en courant continu à l'étage d'excitation mentionné (22) par l'intermédiaire de l'enroulement de balayage mentionné pour former ladite première tension ( $V_D$ ) par ledit condensateur d'arrêt à courant continu ( $C_V$ ).

3. Circuit selon la revendication 2, caractérisé en ce que ladite première tension ( $V_D$ ) est une tension continue et dans lequel l'impédance mentionnée qui peut être commandée ( $Q_9$ ) crée ledit trajet de courant qui conduit un courant continu du condensateur d'arrêt à courant continu mentionné ( $V_D$ ) par l'intermédiaire du premier condensateur mentionné ( $C_1$ ) pendant ladite seconde portion de ladite période donnée dans le mode de fonctionnement normal mentionné.

4. Circuit selon la revendication 1, caractérisé en ce que ledit premier commutateur ( $Q_7$ ) est couplé en parallèle avec ledit premier condensateur ( $C_1$ ) pour décharger ledit premier condensateur ( $C_1$ ) à travers celui-ci pendant ladite première portion de ladite période donnée.

5. Circuit selon la revendication 1, caractérisé en ce que ladite impédance qui peut être commandée comprend un second commutateur ( $Q_9$ ) sensible au second signal de commande mentionné (25) et une première résistance ( $R_{11}$ ) couplée en série avec ledit second commutateur ( $Q_9$ ), ledit second commutateur ( $Q_9$ ) n'étant pas conducteur pendant le fonctionnement dans ledit mode service pour empêcher que le premier condensateur ( $C_1$ ) ne se charge par l'intermédiaire de ladite première résistance ( $R_{11}$ ).

6. Circuit selon la revendication 5, caractérisé par une seconde résistance ( $R_{100}$ ) ayant une première borne couplée à une jonction du premier condensateur mentionné ( $C_1$ ) et de ladite source ( $C_V$ ) de ladite première tension ( $V_D$ ), ladite seconde résistance ( $R_{100}$ ) ayant une seconde borne qui est coupée à une borne de jonction entre ledit second commutateur ( $Q_9$ ) et ladite première résistance ( $R_{11}$ ).

7. Circuit selon la revendication 1, caractérisé par un second condensateur d'arrêt à courant continu ( $C_2$ ) ayant une première borne qui est couplée à une borne du premier condensateur mentionné ( $C_1$ ) qui est éloignée de ladite sour-

ce ( $C_V$ ) de ladite première tension ( $V_D$ ) et une seconde borne qui est coupée à une borne d'entrée de l'amplificateur mentionné ( $IC_1$ ) pour couper ledit signal en dents de scie à l'amplificateur mentionné ( $IC_1$ ).

8. Circuit selon la revendication 1, caractérisé par une résistance d'échantillonnage de courant de balayage ( $R_8$ ) couplée à l'enroulement de balayage mentionné ( $L_V$ ) et un amplificateur d'erreur ( $Q_1$ ) sensible au signal en dents de scie mentionné (27) et à un signal qui est formé par ladite résistance d'échantillonnage ( $R_8$ ) pour générer un signal d'erreur à courant alternatif conformément à une différence entre les deux qui est couplée à ladite borne d'entrée ( $B$ ) de l'amplificateur mentionné.

9. Circuit selon la revendication 1, caractérisé en ce qu'une première borne ( $D$ ) du premier condensateur mentionné ( $C_1$ ) est couplée à une borne de sortie ( $A$ ) de l'amplificateur mentionné ( $IC_1$ ) et une seconde borne du premier condensateur mentionné ( $C_1$ ) est couplée à une borne d'entrée ( $B$ ) de l'amplificateur mentionné ( $IC_1$ ) de telle manière qu'un trajet de réaction d'un signal à courant alternatif de ladite borne de sortie à ladite borne d'entrée de l'amplificateur mentionné ( $IC_1$ ), qui inclut ledit premier commutateur ( $Q_7$ ) et ledit premier condensateur ( $C_1$ ), a substantiellement la même courbe pendant les deux modes de fonctionnement, le mode normal et le mode service.