CLAIMS

1. A semiconductor die, comprising: a first doped region; a second doped region; a first contact over the first doped region; a second contact over the second doped region, wherein the first contact and the second contact are in a first contact middle of line (MOL) layer of the semiconductor die; an interconnect formed from the first contact MOL layer, wherein the interconnect is spaced apart from the first contact and the second contact in a first lateral direction, and the interconnect extends in a second lateral direction that is perpendicular to the first lateral direction; a first bridge between the first contact and the interconnect, wherein the first bridge electrically couples the first contact to the interconnect; a second bridge between the second contact and the interconnect, wherein the second bridge electrically couples the second contact to the interconnect; a first metal line formed from a first interconnect metal layer; and a first via electrically coupling the interconnect to the first metal line, wherein the first and second contacts are formed from the first contact MOL layer, and the first and second bridges are formed from a second MOL layer.

2. The semiconductor die of claim 1, wherein the first doped region comprises an N-type doped region, and the second doped region comprises a P-type doped region.

3. A semiconductor die, comprising: a first doped region; a second doped region; a first contact over the first doped region; a second contact over the second doped region, wherein the first contact and the second contact are in a first contact middle of line (MOL) layer of the semiconductor die; an interconnect formed from the first contact MOL layer, wherein the interconnect is spaced apart from the first contact and the second contact in a first lateral direction, and the interconnect extends in a second lateral direction that is perpendicular to the first lateral direction; a first bridge between the first contact and the interconnect, wherein the first bridge electrically couples the first contact to the interconnect; a second bridge between the second contact and the interconnect, wherein the second bridge electrically couples the second contact to the interconnect; a first metal line formed from a first interconnect metal layer; a first via electrically coupling the interconnect to the first metal line; a gate; a gate contact over the gate; a second metal line formed from the first interconnect metal layer; and a second via electrically coupling the gate contact to the second metal line, wherein the first metal line and the second metal line extend along a common line, and the first metal line and the second metal line are spaced apart by a gap.

4. The semiconductor die of claim 3, wherein the first metal line and the second metal line extend in a same lateral direction.

5. A semiconductor die, comprising: a first doped region; a second doped region; a first contact over the first doped region; a second contact over the second doped region, wherein the first contact and the second contact are in a first contact middle of line (MOL) layer of the semiconductor die; an interconnect formed from the first contact MOL layer, wherein the interconnect is spaced apart from the first contact and the second contact in a first lateral direction, and the interconnect extends in a second lateral direction that is perpendicular to the first lateral direction; a first bridge between the first contact and the interconnect, wherein the first bridge electrically couples the first contact to the interconnect; a second bridge between the second contact and the interconnect, wherein the second bridge electrically couples the second contact to the interconnect; a first metal line formed from a first interconnect metal layer; a first via electrically coupling the interconnect to the first metal line; a gate; a gate contact over the gate; a second metal line formed from the first interconnect metal layer; a second via electrically coupling the gate contact to the second metal line; an input metal line formed from a second interconnect metal layer; a third via electrically coupling the second metal line to the input metal line; an output metal line formed from the second interconnect metal layer; and a fourth via electrically coupling the first metal line to the output metal line.

6. The semiconductor die of claim 5, wherein the first doped region comprises an N-type doped region of an NFET, and the second doped region comprises a P-type doped region of a PFET.

7. The semiconductor die of claim 5, wherein the first metal line and the second metal line extend in the first lateral direction, and the input metal line and the output metal line extend in the second lateral direction.

8. The semiconductor die of claim 1, further comprising: a second metal line formed from the first interconnect metal layer; and a second via electrically coupling the interconnect to the second metal line.

9. The semiconductor die of claim 8, further comprising: an output metal line formed from a second interconnect metal layer; a third via electrically coupling the first metal line to the output metal line; and a fourth via electrically coupling the second metal line to the output metal line.

10. The semiconductor die of claim 9, wherein the first metal line and the second metal line extend in the first lateral direction, and the output metal line extends in the second lateral direction.

11. A semiconductor die, comprising: an N-type field effect transistor (NFET) having a drain; a P-type field effect transistor (PFET) having a drain, wherein the NFET and the PFET have a common gate, and the NFET and the PFET are interconnected to form an inverter; an interconnect formed from a first middle of line (MOL) layer, wherein the interconnect electrically couples the drain of the NFET to the drain of the PFET; a first metal line formed from a first interconnect metal layer; a first via electrically coupling the interconnect to the first metal line; a gate contact over the gate, wherein the gate contact is formed from a second MOL layer; a second metal line formed from the first interconnect metal layer; and a second via electrically coupling the gate contact to the second metal line; wherein the first metal line and the second metal line extend along a common line, and the first metal line and the second metal line are spaced apart by a gap.

12. The semiconductor die of claim 1, wherein the first and second bridges extend in the first lateral direction.

13. The semiconductor die of claim 12, wherein the first and second contacts, the first and second bridges, and the interconnect are coplanar.