Method for Treatment of a Temporarily Bonded Product Wafer

Specification

The invention relates to a method and a device for treatment of a temporarily bonded wafer.

Novel, three-dimensional integrated circuits require reliable methods for handling of thin wafers in order to be able to successfully transport the thin wafers through the necessary product processes on the wafer back. The method of temporary bonding had become established in past years. In it the product wafer with a fully or partially finished first main surface is mounted on a carrier by means of a suitable method, especially by means of adhesive technology. Here this first main surface points in the direction of the carrier wafer. The product wafer is then thinned by means of known grinding techniques. After this thinning process other production steps are carried out on the back of the thin wafer. In the past, processes in which high thermal stresses were produced in the wafer, such as for example abrupt heating and/or cooling, led to problems. Often the wafer acquired dimples which made further processing impossible. The dimples are at the same time sites on which the adhesive used for fixing of thin wafers runs and thus the adhesive thickness is not uniform,

Wafer thinning on backgrind tapes (BG tape), therefore not stable carrier substrates, is known. Here the wafer is usually only thinned by means of grinding methods. There is no further working on the wafer back. At least in this case complex structures such as wiring lines or the like are no longer produced. In this region it is conventional to thin the wafers by means of a succession of coarse and fine grinding processes. These grinding processes however generally leave damage to the crystal structure on the ground wafer surface. This damage leads to stresses. Therefore, in this

domain possibilities for eliminating this damaged layer have been researched in recent years. The result is so-called "stress relief processes". But in order to be able to bypass these processes, manufacturers of grinding systems and grinding tools such as for example the Disco company in Japan have also worked on grinding wheels which eliminate the necessity of stress relief. One very popular product in this domain is for example the so-called Polygrind grinding wheel which makes it possible to saw the wafers immediately after thinning and to deliver them into the final chip packaging (called "packaging" in the industry).

The second relevant domain is the domain of thinning of wafers which are mounted on rigid carrier substrates. In this domain the wafers are likewise thinned to the desired target thickness by means of coarse and fine grinding methods. Typically target thicknesses of less than 100 μm are desirable. But recently wafers are being thinned preferably to 75 or 50 μm. It is expected in the future that the wafers will be more radically thinned to 30, 20 or even 10 μm. In this range the detailed process sequence in thinning of the wafer has been conventionally determined by the necessary surface quality. Often the backthinning process ends with the use of fine grinding processes employing the Polygrind grinding wheels. In this domain to date intentionally chosen processes have not been used to improve the surface quality for further working, especially in thermal applications. This is among others also the case because the rigid carrier was regarded as a sufficient means to adequately support and keep flat the thin wafer during the following process.

Embodiments of this invention devise a device and a method with which further handling is facilitated or enabled with increasingly thinner, temporarily fixed product wafers, especially for following chemical processes.

According to a first aspect, there is provided a method for treatment of a product wafer temporarily bonded on a carrier wafer with the following steps:

- bonding a processed side of the product wafer to the carrier wafer,
- grinding and/or backthinning of the product wafer on one flat side facing away from the carrier wafer to a product wafer thickness D of < 150 μm, especially < 100 μm, preferably < 75 μm, even more preferably < 50 μm, especially preferably < 30 μm, and
- surface treatment of the flat side with means for reducing an especially structural intrinsic stress of the product wafer.

According to a second aspect, there is provided a device for treatment of a product wafer temporarily bonded on a carrier wafer with the following features:

- means for bonding a processed side of the product wafer to the carrier wafer,
- means for grinding and/or backthinning of the product wafer, and
- means for reducing an especially structural intrinsic stress of the product wafer.

According to a third aspect, there is provided a device for executing the above method.

All combinations of at least the two features given in the specification, the claims and/or the figures also fall within the framework of embodiments of the invention. At the given value ranges, values within the indicated limits will also be disclosed as boundary values and will be claimed in any combination.

Embodiments of the invention relate to a method for avoiding the aforementioned dimples in thinning of wafers and thus ensuring the quality of the temporarily bonded wafers during the process flow. If the surface defects were not avoided, problems would arise in the further processing.

The phenomenon of dimples has become a serious problem only in the recent past. The main reason for this should be the circumstance that only now are very small target thicknesses (see above) desirable for thin wafers. If the wafers become thinner, the intrinsic stiffness of the thin wafers decreases, as a result of which the stress (intrinsic stress) which arises due to crystal defects according to the findings of the applicant continues to be counteracted only with a less stable wafer. Rather wafers in this thickness range are very pliable and flexible.

It is pointed out that only recently has this type of carrier technology for processing of ultrathin wafers been used to produce mainly stacked dies or so-called "3D packages".

Especially unfavorable conditions in conjunction with dimple formation arise when, as the thickness of the wafers decreases, they also have increasing topography on the front and are to be embedded in the adhesive located between the carrier and product wafer. This topography for wafers with little topography is less than 10 μm, typically less than 20 μm; this results in adhesive thicknesses from 10 to 30 μm in this case. Here it should be noted that conventionally the adhesive thickness is chosen to be roughly 10 μm thicker than the height of the topography. For wafers with high topography, topography heights of > 30 μm, often with > 50 μm, but typically with > 70 μm

and in many cases with > 100 μm can be expected.

The higher adhesive thickness in conjunction with the very thin wafers results in that even slight stress in the wafer is sufficient to cause dimples. This is a phenomenon which occurs mainly for thermoplastic adhesives which lose viscosity at elevated temperature. This represents requirements which cannot be found in the case of conventional (prior art) backgrinding on BG tape. The higher adhesive thickness enables easier flow of the adhesive; this, associated with the very low intrinsic stiffness of the product wafer, promotes dimple formation.

The advantage as per embodiments of the invention consist in that surface defects in backthinning of temporarily bonded wafers can be completely avoided; this is a significant improvement in the quality of the final product. Furthermore this is associated with a performance improvement of the production process since the dimples no longer occur even at higher temperatures to which the wafers are generally still subject in the production process.

Since dimple formation is also dependent on temperature (since with rising temperature the viscosity of thermoplastic adhesives decreases), the temperature range in which the wafers can be processed can be widened by embodiments of this invention. Mainly in PECVD processes in which higher temperatures are used and in which by the action of plasma additional thermal energy is delivered into the wafer, dimple formation must be completely stopped. It has already been demonstrated that embodiments of this invention in fact stops dimple formation. Ultrathin wafers with this type of stacked structures are generally processed above 50°C, especially above 75°C and in particular above 100°C, with which embodiments of the indicated invention becomes indispensable to avoid dimple formation.

Therefore embodiments of the invention are based on the idea of setting the stress of the thin wafer after grinding in a dedicated manner. Here the thin wafer is mounted on a carrier by means of known

methods. This carrier wafer can fundamentally consist of any material with the corresponding mechanical properties. But preferably silicon, glass and certain ceramic materials are used. One main feature here is based on the carrier having a thermal coefficient of expansion which is matched/as identical as possible to that of the product wafer (for example, silicon) both in spots and also with respect to the characteristic of the coefficient over the temperature range. Here it should be mentioned as a preferred version that the product wafer with the already processed side is adhesiveed onto the carrier wafer using a thermoplastic or at least largely thermoplastic adhesive. One example of this adhesive is the HT 10.10 Material from Brewer Science Inc., Rolla, Missouri, USA. Then the wafer is thinned by means of grinding methods. This thinning process takes place from the interplay of coarse and fine grinding processes. The decisive part as per embodiments of the invention is to subject the wafer to a further suitable process which makes it possible to remove the layer with the damaged crystal structure either entirely or partially in a controlled manner. Furthermore it is pointed out that the crystal structure can be defective not only on the surface, but also to a few µm underneath the surface, therefore the defects are present over a great depth, especially deeper than 0.5 µm, 1 µm, 3 µm, 5 µm and even 10 µm.

It is therefore not enough to remove only a few layers of atoms to remove the defects near the surface.

In partial removal it is possible to set the stress of the wafer in a dedicated manner and thus to compensate for possible intrinsic stresses of the wafer which could be present for example as a result of the layer on the active side. Thus the wafer no longer arches during subsequent processes with a high thermal stress.

Suitable processes for removal of this damaged layer are:

- polishing processes - for example the "dry polish process" from Disco,
- wet etching processes which are carried out by means of suitable chemicals,
- drying processes,
- a combination of the aforementioned processes.

Embodiments of the invention consist in a process flow, characterized in that

- a carrier wafer is temporarily bonded to a structure wafer via an adhesion material
- aftertreatment of the structure wafer takes place after backthinning
- aftertreatment of the structure wafer is a combination of cleaning and chemical mechanical polishing (CMP), characterized in that in CMP the surface roughness produced by brittle fracture, the cracks and the built-in intrinsic stresses are reduced or completely eliminated
- due to the resulting smoother surface fewer structure defects are present which are used at higher temperatures finally as a starting point for the aforementioned surface defects (dimples)
- due to CMP the intrinsic stresses in the structure wafer are dramatically smaller than in the structure wafers which have been thinned by grinding
- due to the lower intrinsic stresses a local elastic kinking and/or plastic deformation of the very thin structure wafer into the underlying adhesion layer, mainly at higher temperatures, is prevented
- without these surface defects (dimples) the quality of the structure wafer is extremely enhanced
- the controlling factor 0.5 µm, 1 µm, 5 µm, and 10 µm.

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- the controlling factor 0.5 µm, 1 µm, 3 µm, 5 mµ, and 10 µm.

All combinations of at least the two features given in the specification, the claims and/or the figures also fall within the framework of embodiments of the invention. At the given value ranges, values within the indicated limits will also be disclosed as boundary values and will be claimed in any combination.

Other advantages, features and details of the invention will become apparent from the

following description of preferred exemplary embodiments and using the drawings.

Figure 1 shows a surface of a temporarily bonded product wafer after a grinding process according to the prior art (C-SAM photograph),

Figure 2 shows a surface of a temporarily bonded product wafer after treatment according to this invention (C-SAM photograph).

The figures show that the product wafer as shown in Figure 1 has distinct dimples, whereas the product wafer shown in figure 2 has practically no dimples.

Claims

1. Method for treatment of a product wafer temporarily bonded on a carrier wafer with the following steps:

- bonding a processed side of the product wafer to the carrier wafer,
- grinding and/or backthinning of the product wafer on one flat side facing away from the carrier wafer to a product wafer thickness D of < 150 μm, especially < 100 μm, preferably < 75 μm, even more preferably < 50 μm, especially preferably < 30 μm, and
- surface treatment of the flat side with means for reducing an especially structural intrinsic stress of the product wafer.

2. Method as claimed in Claim 1, wherein surface treatment takes place in an independent process which is separated, especially in space, from backthinning.

3. Method as claimed in one of Claims 1 or 2, wherein the means for reducing the intrinsic stress are characterized by at least one of the following features:

- dry polishing of the flat side
- wet etching of the flat side
- dry etching of the flat side.

4. Method as claimed in one of the preceding claims, wherein the intrinsic stress of the product wafer can be set by the means for reducing the intrinsic stress.

5. Method as claimed in one of the preceding claims, wherein the carrier wafer, especially at a certain and/or over a temperature range of the temperature of the carrier wafer has a coefficient of expansion which is essentially identical to the coefficient of expansion of the product wafer.

6. Method as claimed in one of the preceding claims, wherein the product wafer with its contact side which is opposite the flat side is temporarily connected to the carrier wafer using an at least in part, especially predominantly, thermoplastic adhesive.

7. Method as claimed in one of the preceding claims, wherein the means for reducing the intrinsic stress are made such that they remove at least partially a defined layer thickness S of a crystal structure of the flat side which has been damaged especially by grinding and/or backthinning.

8. Method as claimed in one of the preceding claims, wherein the intrinsic stress of the product wafer is set by the means for reducing the intrinsic stress such that the product wafer arches toward the carrier wafer during a following thermal process.

9. Method as claimed in Claim 6, wherein the product wafer of the contact side has topographies which are embedded into the adhesive.

10. Method as claimed in one of the preceding claims, wherein after surface treatment a thermal process step follows especially at temperatures > 50°C, preferably > 75°C, preferably > 100°C.

11. Method as claimed in one of the preceding claims, wherein the thermal method step is an especially chemical gas phase deposition method step.

12. Method as claimed in Claim 7, wherein the layer thickness is $S < 10$ µm, especially < 5 µm, preferably < 3 µm, even more preferably < 1 µm, especially preferably < 0.5 µm.

13. Device for treatment of a product wafer temporarily bonded on a carrier wafer with the following features:

- means for bonding a processed side of the product wafer to the carrier wafer,
- means for grinding and/or backthinning of the product wafer, and
- means for reducing an especially structural intrinsic stress of the product wafer.

14. Device for executing a method as claimed in one of claims 1 to 12.