G00002

ABSTRACT

A METHOD TO FORM A LOW PARASITIC CAPACITANCE PSEUDO-SOI CMOS DEVICE

A method of forming a pseudo-SOI device having elevated source/drain (S/D) regions that can be extended for use as local interconnect is described. Shallow trench isolation (STI) regions separating adjacent active regions are provided within a semiconductor substrate. Polysilicon gate electrodes and associated S/D extensions are fabricated in and on the substrate in the active regions wherein a hard mask layer overlies each of the gate electrodes. Dielectric spacers are formed on sidewalls of each of the gate electrodes. A polysilicon layer is deposited overlying the gate electrodes and the substrate. The polysilicon layer is polished back with a polish stop at the hard mask layer. The polysilicon layer is etched back whereby the polysilicon layer is recessed with respect to the gate electrodes. Thereafter, the polysilicon layer is etched away overlying the STI regions where a separation between adjacent active areas is desired. If a local interconnect is desired between adjacent active areas, the polysilicon layer is not etched away overlying the STI region separating those active areas. The hard mask layer is removed. Ions are implanted and driven in to form elevated S/D regions within the polysilicon layer adjacent to the gate electrodes to complete formation of transistors having elevated S/D regions.

FIGURE 12

162162