CLAIMS

1. A circuit for receiving data, comprising:

a first amplification module, configured to: receive an enable signal, a first feedback signal, a second feedback signal, a data signal, a first reference signal, and a second reference signal; when the enable signal is at a first level, in response to a sampling clock signal and on a basis of the first feedback signal, select the data signal and the first reference signal for a first comparison and output a first signal pair as a result of the first comparison, or in response to the sampling clock signal and on a basis of the second feedback signal, select the data signal and the second reference signal for a second comparison and output a second signal pair as a result of the second comparison; and when the enable signal is at a second level, perform the first comparison in response to the sampling clock signal, and output the first signal pair; wherein, a level of the first feedback signal is opposite to a level of the second feedback signal, the first signal pair comprises a first signal and a second signal, and the second signal pair comprises a third signal and a fourth signal;

wherein the first amplification module comprises: an amplification unit, provided with a first node, a second node, a third node and a fourth node, the first node being for outputting the first signal, the second node being for outputting the second signal, the third node being for outputting the third signal, and the fourth node being for outputting the fourth signal, and configured to receive the data signal, the first reference signal, and the second reference signal; a first N-channel metal oxide semiconductor (NMOS) transistor and a second NMOS transistor, the first NMOS transistor being provided with one terminal connected to the first node and another terminal connected to one terminal of the second NMOS transistor, another terminal of the second NMOS transistor being connected to the second node, a gate of one of the first NMOS transistor and the second NMOS transistor being configured to receive a first complementary feedback signal, a gate of the

other one of the first NMOS transistor and the second NMOS transistor being configured to receive the enable signal, and a level of the first complementary feedback signal being opposite to the level of the first feedback signal; and a third NMOS transistor and a fourth NMOS transistor, the third NMOS transistor being provided with one terminal connected to the third node and another terminal connected to one terminal of the fourth NMOS transistor, another terminal of the fourth NMOS transistor being connected to the fourth node, a gate of one of the third NMOS transistor and the fourth NMOS transistor being configured to receive a second complementary feedback signal, a gate of the other one of the third NMOS transistor and the fourth NMOS transistor being configured to receive the enable signal, and a level of the second complementary feedback signal being opposite to the level of the second feedback signal; and

a second amplification module, configured to receive output signals of the first amplification module as an input signal pair, perform an amplification processing on a voltage difference of the input signal pair, and output a first output signal and a second output signal as a result of the amplification processing.

2. The circuit for receiving data according to claim 1, wherein the first amplification module further comprises:

a fifth NMOS transistor and a sixth NMOS transistor, the fifth NMOS transistor being provided with one terminal connected to the first node and another terminal connected to one terminal of the sixth NMOS transistor, another terminal of the sixth NMOS transistor being connected to the second node, a gate of one of the fifth NMOS transistor and the sixth NMOS transistor being configured to receive the first complementary feedback signal, and a gate of the other one of the fifth NMOS transistor and the sixth NMOS transistor being configured to receive the enable signal.

3. The circuit for receiving data according to claim 2, wherein a gate of the first NMOS transistor is configured to receive the enable signal, and a gate of the second NMOS transistor is configured to receive the first complementary feedback signal, wherein a channel width of the first NMOS transistor is greater than a channel width of the second NMOS transistor; a gate of the fifth NMOS transistor is configured to receive the first complementary feedback signal, and a gate of the sixth NMOS transistor is configured to receive the enable signal, wherein a channel width of the fifth NMOS transistor is smaller than a channel width of the sixth NMOS transistor; and

the channel width of the fifth NMOS transistor is equal to the channel width of the second NMOS transistor; the channel width of the sixth NMOS transistor is equal to the channel width of the first NMOS transistor; and a channel length of the first NMOS transistor, a channel length of the second NMOS transistor, a channel length of the fifth NMOS transistor, and a channel length of the sixth NMOS transistor are all equal.

4. The circuit for receiving data according to claim 1, wherein the first amplification module further comprises:

a seventh NMOS transistor and an eighth NMOS transistor, the seventh NMOS transistor being provided with one terminal connected to the third node and another terminal connected to one terminal of the eighth NMOS transistor, another terminal of the eighth NMOS transistor being connected to the fourth node, a gate of one of the seventh NMOS transistor and the eighth NMOS transistor being configured to receive the second complementary feedback signal, and a gate of the other one of the seventh NMOS transistor and the eighth NMOS transistor being configured to receive the enable signal.

5. The circuit for receiving data according to claim 4, wherein a gate of the third NMOS transistor is configured to receive the enable signal, and a

gate of the fourth NMOS transistor is configured to receive the second complementary feedback signal, wherein a channel width of the third NMOS transistor is greater than a channel width of the fourth NMOS transistor; a gate of the seventh NMOS transistor is configured to receive the second complementary feedback signal, and a gate of the eighth NMOS transistor is configured to receive the enable signal, wherein a channel width of the seventh NMOS transistor is smaller than a channel width of the eighth NMOS transistor; and

the channel width of the seventh NMOS transistor is equal to the channel width of the fourth NMOS transistor; the channel width of the eighth NMOS transistor is equal to the channel width of the third NMOS transistor; and a channel length of the third NMOS transistor, a channel length of the fourth NMOS transistor, a channel length of the seventh NMOS transistor, and a channel length of the eighth NMOS transistor are all equal.

6. The circuit for receiving data according to claim 1, wherein the sampling clock signal comprises a first sampling clock signal and a second sampling clock signal; and the amplification unit comprises:

a first comparison circuit, provided with the first node and the second node, and configured to receive the data signal and the first reference signal and perform the first comparison in response to the first sampling clock signal;

a clock generation circuit, configured to receive the enable signal and an original sampling clock signal and output the second sampling clock signal, wherein when the enable signal is at the first level, a phase of the second sampling clock signal is opposite to a phase of the original sampling clock signal, and when the enable signal is at the second level, the second sampling clock signal is a logic high-level signal; and

a second comparison circuit, provided with the third node and the fourth node, and configured to: receive the data signal and the second reference

signal; when the enable signal is at the first level, perform the second comparison in response to the second sampling clock signal; and when the enable signal is at the second level, turn on a connection path between the third node and a ground terminal, and turn on a connection path between the fourth node and the ground terminal.

7. The circuit for receiving data according to claim 6, wherein the first comparison circuit comprises:

a first current source, connected between a power supply node and a fifth node and configured to provide a current to the fifth node in response to the first sampling clock signal;

a first comparison unit, connected to the first node, the second node, and the fifth node, and configured to receive the data signal and the first reference signal, perform the first comparison when the first current source provides the current to the fifth node, and output the first signal and the second signal; and

a first reset unit, connected to the first node and the second node and configured to reset the first node and the second node in response to the first sampling clock signal; and

the second comparison circuit comprises:

a second current source, connected between the power supply node and a sixth node and configured to provide a current to the sixth node in response to the second sampling clock signal;

a second comparison unit, connected to the third node, the fourth node, and the sixth node, and configured to receive the data signal and the second reference signal, perform the second comparison when the second current source provides the current to the sixth node, and output the third signal and the fourth signal; and

a second reset unit, connected between the third node and the fourth node and configured to reset the third node and the fourth node in response to the second sampling clock signal.

8. The circuit for receiving data according to claim 7, wherein the first current source comprises:

a first P-channel metal oxide semiconductor (PMOS) transistor, connected between the power supply node and the fifth node and provided with a gate for receiving the first sampling clock signal; and

the second current source comprises:

a second PMOS transistor, connected between the power supply node and the sixth node and provided with a gate for receiving the second sampling clock signal;

the first comparison unit comprises:

a third PMOS transistor, connected between the first node and the fifth node and provided with a gate for receiving the data signal; and

a fourth PMOS transistor, connected between the second node and the fifth node and provided with a gate for receiving the first reference signal; and

the second comparison unit comprises:

a fifth PMOS transistor, connected between the third node and the sixth node and provided with a gate for receiving the data signal; and

a sixth PMOS transistor, connected between the fourth node and the sixth node and provided with a gate for receiving the second reference signal;

the first reset unit comprises:

a ninth NMOS transistor, connected between the first node and the ground terminal and provided with a gate for receiving the first sampling clock signal; and

a tenth NMOS transistor, connected between the second node and the ground terminal and provided with a gate for receiving the first sampling clock signal; and

the second reset unit comprises:

an eleventh NMOS transistor, connected between the third node and the ground terminal and provided with a gate for receiving the second sampling

clock signal; and

a twelfth NMOS transistor, connected between the fourth node and the ground terminal and provided with a gate for receiving the second sampling clock signal.

9. The circuit for receiving data according to claim 6, wherein the clock generation circuit comprises:

a first NAND gate circuit, provided with one input terminal for receiving the original sampling clock signal, the other input terminal connected to a power supply node, and an output terminal for outputting the first sampling clock signal; and

the clock generation circuit comprises:

a second NAND gate circuit, provided with one input terminal for receiving the original sampling clock signal, the other input terminal for receiving the enable signal, and an output terminal for outputting the second sampling clock signal.

10. The circuit for receiving data according to claim 1, wherein the second amplification module comprises:

a first input unit, connected to a seventh node and an eighth node, and configured to receive the first signal pair for a third comparison and provide a signal to the seventh node and a signal to the eighth node respectively as a result of the third comparison;

a second input unit, connected to the seventh node and the eighth node, and configured to receive the second signal pair for a fourth comparison and provide a signal to the seventh node and a signal to the eighth node respectively as a result of the fourth comparison; and

a latch unit, connected to the seventh node and the eighth node, and configured to amplify and latch a signal of the seventh node and a signal of the eighth node, and output the first output signal and the second output

signal respectively through a first output node and a second output node.

11. The circuit for receiving data according to claim 10, wherein the first input unit comprises:

a thirteenth NMOS transistor, provided with a drain connected to the seventh node, a source connected to a ground terminal, and a gate for receiving the first signal; and

a fourteenth NMOS transistor, provided with a drain connected to the eighth node, a source connected to the ground terminal, and a gate for receiving the second signal; and

the second input unit comprises:

a fifteenth NMOS transistor, provided with a drain connected to the seventh node, a source connected to the ground terminal, and a gate for receiving the third signal; and

a sixteenth NMOS transistor, provided with a drain connected to the eighth node, a source connected to the ground terminal, and a gate for receiving the fourth signal.

12. The circuit for receiving data according to claim 10, wherein the latch unit comprises:

a seventeenth NMOS transistor and a seventh PMOS transistor, a gate of the seventeenth NMOS transistor and a gate of the seventh PMOS transistor being both connected to the second output node, a source of the seventeenth NMOS transistor being connected to the seventh node, a drain of the seventeenth NMOS transistor and a drain of the seventh PMOS transistor being both connected to the first output node, and a source of the seventh PMOS transistor being connected to a power supply node; and

an eighteenth NMOS transistor and an eighth PMOS transistor, a gate of the eighteenth NMOS transistor and a gate of the eighth PMOS transistor being both connected to the first output node, a source of the eighteenth

NMOS transistor being connected to the eighth node, a drain of the eighteenth NMOS transistor and a drain of the eighth PMOS transistor being both connected to the second output node, and a source of the eighth PMOS transistor being connected to the power supply node.

13. The circuit for receiving data according to claim 12, wherein the second amplification module further comprises:

a third reset unit, connected between the power supply node and an output terminal of the latch unit and configured to reset the output terminal of the latch unit.

14. The circuit for receiving data according to claim 13, wherein the third reset unit comprises:

a ninth PMOS transistor, connected between the first output node and the power supply node and provided with a gate for receiving an original sampling clock signal; and

a tenth PMOS transistor, connected between the second output node and the power supply node and provided with a gate for receiving the original sampling clock signal.

15. The circuit for receiving data according to claim 1, further comprising:

a first inverter circuit, configured to receive the first feedback signal and output the first complementary feedback signal; and

a second inverter circuit, configured to receive the second feedback signal and output the second complementary feedback signal.

16. The circuit for receiving data according to claim 15, wherein the first inverter circuit comprises a first inverter; and the second inverter circuit comprises a second inverter; and

the first inverter circuit comprises a third NAND gate, and the third NAND gate is provided with two input terminals for respectively receiving the first feedback signal and the enable signal and an output terminal for outputting the first complementary feedback signal; and the second inverter circuit comprises a fourth NAND gate, and the fourth NAND gate is provided with two input terminals for respectively receiving the second feedback signal and the enable signal and an output terminal for outputting the second complementary feedback signal.

17. A system for receiving data, comprising:

a plurality of cascaded data transmission circuits, wherein each of the data transmission circuits comprises the circuit for receiving data according to any one of claims 1-16, and a latch circuit connected to the circuit for receiving data;

an output signal of a previous stage data transmission circuit is used as a feedback signal of a next stage data transmission circuit; and

an output signal of a last stage data transmission circuit is used as a feedback signal of a first stage data transmission circuit.

18. The system for receiving data according to claim 17, wherein the circuit for receiving data receives data in response to the sampling clock signal; and the system for receiving data comprises four cascaded data transmission circuits, and the sampling clock signals of the circuits for receiving data of adjacent stages have a phase difference of 90 degrees.

19. The system for receiving data according to claim 17, wherein the first output signal and the second output signal outputted by the second amplification module of a previous stage circuit for receiving data are used as the feedback signal of a next stage circuit for receiving data; or, a signal outputted by a previous stage latch circuit is used as the feedback signal of

the next stage circuit for receiving data.

20. A memory device, comprising:

a plurality of data ports; and

a plurality of systems for receiving data according to any one of claims 17-19, each of the systems for receiving data corresponding to one of the data ports.