SEMICONDUCTOR MEMORY DEVICE

ABSTRACT

According to one embodiment, a semiconductor memory device includes a plurality of memory cell array layers that include a first surface and a second surface opposite to the first surface and do not include a substrate and that include a plurality of memory cells arranged 3-dimensionally in a memory cell array region and a surface wiring layer embedded in the first surface or/and the second surface. The surface wiring layer of each of the memory cell array layers is formed to overlap the first surface when viewed in a direction vertical to the first surface, and the surface wiring layers are bonded to each other so that the plurality of memory cell array layers are stacked.

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