SEMICONDUCTOR STRUCTURE, AND METHODS FOR FABRICATING SAME

Technical field and prior art

The field of the invention is that of manufacturing semiconductor components or elements, in particular silicon on insulator (SOI) components or elements.

A SOI structure typically includes a silicon layer containing the components as such and beneath which is formed a buried silicon oxide layer which provides insulation against stray currents and charges originating from ionized particles. It also provides good isolation of adjacent components formed in the same silicon layer, and in particular a significant reduction in the stray capacitance between adjacent components. It rests on a silicon substrate which provides a mechanical support.

The surface silicon layer typically has a thickness of around 10 nanometers (nm) to 1000 nm, for example, and the oxide layer typically has a thickness of the order of a few hundred nm (for example 400 nm) or more.

The thickness can vary, in particular the thickness of the silicon layer. Silicon layers of different thickness characterize fully depleted (FD) SOI components, which have a surface silicon layer from approximately 20 nm to approximately 40 nm thick, and partially depleted (PD) SOI components, in which the thickness of the surface silicon layer is greater than approximately 70 nm.

Silicon oxide layers with different thicknesses provide different degrees of isolation, different leakage currents, different voltage ratings, and different equivalent capacitances, values of all of which parameters can be chosen by the developer.

Different thicknesses can suit different applications, in particular applications to logic and other digital circuits and power applications.

The PD SOI technology is preferred for some applications or functions and the FD SOI technology or

the bulk (silicon substrate) technology is preferred for other applications.

Furthermore, there is at present a need for components and structures integrating these different techniques, i.e. components or structures integrating, on the same substrate, bulk (silicon substrate) areas, SOI areas and/or FD SOI and PD SOI areas, with different thicknesses of the surface silicon layers and/or different thicknesses of the buried oxide layers. This applies in particular to the field of microsystems integrating sensors or accelerometers, for example, and to the field of "one chip systems" which integrate a plurality of functions in the same chip.

The great majority of SOI components are currently of the homogeneous type.

Techniques for producing SOI components with alternating bulk and SOI areas are nevertheless known in the art.

Figures 1A and 1B show diagrammatically a first technique for producing SOI components or elements. It includes a first step of using a technique known in the art to produce an SOI component 2 onto which an etching mask 4 is deposited (see Figure 1A).

An etching step then produces alternating bulk areas 6, 8 and SOI areas 10, 12, 14 (see Figure 1B).

That technique cannot be used at present to produce on the same substrate SOI areas having different thickness silicon layers and/or different thickness oxide layers.

Nor can it be used at present to produce components integrating FD SOI areas and PD SOI areas on the same substrate or to provide electrical continuity between bulk areas and the surface silicon layer in the SOI areas.

Finally, the structure obtained is not planar.

Figure 2 shows diagrammatically another technique known in the art for producing SOI components.

It uses the separation by implanted oxygen (SIMOX) technique: areas 16, 18 of silicon dioxide are obtained by implanting O++ ions through a mask 20. That produces a structure including a thin surface film of monocrystalline silicon isolated from the mass of the substrate. However, the layer of oxide produced in that way is again a uniform layer: at present that technique cannot be used to produce layers with different thicknesses in the same substrate.

The second technique is also subject to other problems.

First of all, non-homogeneous stresses and stresses occur in the substrate, as confirmed in the paper by S. Bagchi *et al.* published in the proceedings of the IEEE International SOI Conference, October 1999, p. 121-122, "Defect Analysis of Patterned SOI Material".

Slight swellings or differences in flatness are observed on the surface above the implanted areas 16, 18.

The wafer bonding technique is also known in the art, but cannot at present be used to produce SOI areas with different thicknesses.

The problem therefore exists of finding a technique for producing, on the same substrate, a semiconductor component, element or structure having two or more semiconductor on insulator areas having different thicknesses of the surface semiconductor material layer and/or different thicknesses of the dielectric material layer, or for producing, on the same substrate, a semiconductor component or element or a semiconductor structure integrating bulk (semiconductor material substrate) areas and semiconductor on insulator areas and/or semiconductor material surface layer thicknesses differing from one area to another and/or dielectric thicknesses differing from one area to another.

The problem also exists of finding a technique for producing, on the same substrate, an SOI component, element or structure having two or more SOI areas having

different thicknesses of the surface silicon layer and/or different thicknesses of the oxide layer or for producing, on the same substrate, a semiconductor component or element or an SOI semiconductor structure integrating bulk (silicon substrate) areas, SOI areas and/or FD SOI and PD SOI areas with surface silicon thicknesses differing from one area to another and/or dielectric thicknesses differing from one area to another.

A component, element or structure obtained by the above method should preferably be planar and provide electrical continuity between different areas of different kinds or thicknesses, and in particular between the different surface semiconductor material or silicon areas or layers.

A further problem that arises in the above kind of system is that of avoiding or reducing the stresses and dislocations that occur when the SIMOX technique is used.

A still further problem is that of being able to produce semiconductor components having buried dielectric elements individually connected by buried conductive elements, the dielectric elements taking the form of buried layers, possibly of varying thickness, and being situated under surface semiconductor layers, the thickness of which can also vary.

A yet further problem is that of finding new techniques for producing semiconductor substrates having buried dielectric layers or areas.

Summary of the invention

The invention firstly provides a method of producing a semiconductor structure, the method comprising:

- forming in a first semiconductor material substrate a first dielectric area having a first thickness and a second dielectric area having a second thickness which can be different from the first thickness,

- assembling said first substrate with a second semiconductor material substrate, and

- thinning one or both substrates.

Assembling the two substrates forms a single or monolithic component or substrate having a surface semiconductor material layer providing electrical continuity.

Using a step of assembling substrates avoids the dislocations and stresses observed with techniques known in the art, such as the SIMOX technique, and the swelling and differences in flatness observed on the surface above implanted areas.

The single component may include dielectric areas alternating with bulk or semiconductor substrate areas.

Forming in the same component two dielectric areas with different thicknesses, each of which thicknesses may be uniform, can suit different requirements.

The first and second dielectric areas may consist of different dielectric materials.

A third dielectric area may be formed in the first substrate having a third thickness which may be different from the first thickness and/or the second thickness.

One embodiment of the method may include forming in the second substrate a first dielectric area of the second substrate, which may be of uniform thickness.

It may further include forming in the second substrate a second dielectric area of the second substrate, which may have a non-zero thickness, which may be uniform and different from the thickness of the first dielectric area of the second substrate.

If the semiconductor material is silicon, an SOI structure is obtained.

A metal or conductive land or portion or a doped area may also be produced, establishing a connection between two or more dielectric areas.

The invention also provides a method of producing a semiconductor structure, the method comprising:

- forming in a first semiconductor material substrate a dielectric material dielectric area,

- assembling said substrate with a second semiconductor material substrate, and

- thinning either or both substrates, leaving a surface layer of semiconductor material on the dielectric material layer, a first area of said surface layer having a first thickness and a second area of said surface layer having a second thickness different from the first thickness.

This produces a structure having a varying thickness of the surface semiconductor layer.

A substrate may be thinned by forming a weakened plane or layer, for example:

- by implanting atoms or ions in the first or second substrate; the implanted ions may be hydrogen ions, but other substances may be used, including co-implanting hydrogen and helium (H/He) atoms, or

- by forming a layer of porous silicon in the case of silicon.

Thinning may also be achieved by polishing or etching.

Thinning the substrate may be followed by a finishing step such as a localized or overall step of thinning by polishing, etching or sacrificial oxidation, for example, or a step of localized or overall thickening of the silicon film, for example by epitaxial growth.

The invention further provides a method of producing a semiconductor structure, the method comprising:

- a first step of forming in a semiconductor substrate, for example by ion implantation or by a deposition and/or oxidation technique, a first dielectric area of a first dielectric material having a first thickness, and

- a second step of forming in the same substrate, by ion implantation, a second dielectric area of a second

dielectric material having a second thickness, which may be different from the first thickness.

This again produces dielectric areas in the same substrate which may have different thicknesses, but with no step of fracturing a substrate and with no step of assembling two substrates if both steps use ion implantation.

In all embodiments, the first and second dielectric areas may consist of different dielectric materials.

The different dielectric areas may therefore be made from one or more dielectric materials such as, for example, silicon dioxide (SiO_2), silicon nitride (Si_3N_4), diamond, sapphire, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), lanthanum oxide (La_2O_3), or yttrium oxide (Y_2O_3).

The invention further provides a semiconductor structure comprising, in a semiconductor substrate:

- a first area in a semiconductor material surface layer under which is formed a first buried dielectric layer, referred to as the first dielectric layer, of a first dielectric material, and

- a second area in the semiconductor material surface layer under which is formed a second buried dielectric layer, referred to as the second dielectric layer; the thicknesses of the first and second semiconductor surface layers may be non-zero and different from each other and/or the thicknesses of the first and second dielectric layers may be non-zero and different from each other.

This semiconductor structure may include a third area of the semiconductor material surface layer under which is formed a buried dielectric layer referred to as the third dielectric layer. The thickness of the third area of the semiconductor layer may be different from the thicknesses of the first and second areas of the semiconductor layer. The thickness of the third dielectric layer may be different from the thicknesses of

the first and second dielectric layers.

One or more of the dielectric areas may have a size of at least one square micrometer or less than one square micrometer.

One of the first, second, and, where applicable, third areas of the semiconductor layer may be an FD SOI layer and another of these areas may be a PD SOI layer.

One of the first, second, and where applicable, third areas of the semiconductor layer may have thickness from 10 nm to 70 nm and another of these semiconductor material surface layers may have thickness from 50 nm to 250 nm.

The invention further provides a semiconductor component having the above structure, a first electronic component formed in the semiconductor layer on top of the first dielectric layer and a second electronic component in the semiconductor layer on top of the second dielectric layer or where applicable on top of the third dielectric layer, wherein the first and/or second electronic components may be a transistor, for example an MOS transistor.

In an embodiment, in a semiconductor element of the above kind, a first portion of a transistor is produced in the first area of the semiconductor layer and a second portion of the same transistor is produced in the second area of the semiconductor layer.

Brief description of the figures

- Figures 1a to 2 show prior art methods of producing SOI components,
- Figures 3A - 7B show different embodiments of the invention,
- Figures 8A - 9D show different methods that can be used in the context of the invention,
- Figures 10A and 10B show another embodiment of the invention without bonding of substrates,
- Figures 11A and 11B show another embodiment of the invention with a varying thickness surface silicon layer,

- Figures 12A and 12B show another embodiment of the invention,

- Figures 13A and 13B show another aspect of the invention with a conductive land formed in the dielectric layers, and

- Figure 14 shows the production of two transistors in different areas of an SOI substrate conforming to the invention.

Detailed description of embodiments of the invention

Figures 3A and 3B show diagrammatically a first embodiment of a method according to the invention.

In a first semiconductor (for example silicon) substrate 30, dielectric (for example silicon oxide SiO_2) areas or layers 32a, 32b, 32c, 34a, 34b are formed having different thicknesses, typically of the order of a few hundred nm, for example from 100 nm to 500 nm. The thicknesses can be as high as a few tens of thousands of nm and thus from 100 nm to 5000 nm, for example. Different techniques can be used to produce these dielectric areas. They are described below, with reference to Figure 8A and the subsequent figures.

In a second semiconductor substrate 40, a thin layer 42 substantially parallel to a surface 41 of the substrate 40 is formed by implanting atoms or ions. This forms a weakened or fracture layer or plane delimiting in the volume of the substrate 40 a lower region 45 intended to constitute a thin film and an upper region 43 constituting the mass of the substrate 40. Hydrogen is usually implanted, but other substances can be used, or atoms of hydrogen and helium (H/He) can be coimplanted.

The two substrates 30 and 40 prepared in the above manner are then assembled by a wafer bonding technique or by adherent contact, for example by molecular adhesion or by bonding. With regard to these techniques, see Q.Y. Tong and U. Gosele "Semiconductor Wafer Bonding" (Science and Technology), Wiley Interscience Publications.

A portion of the substrate 40 is then detached by treatment causing a fracture along the weakened plane 42. An example of this technique is described in the paper by A.J. Auberton-Hervé *et al.* "Why can Smart-Cut change the future of microelectronics ?" in International Journal of High Speed Electronics and Systems, Vol. 10, No. 1 (2000), p. 131-146.

A semiconductor component, element or structure is formed in this way, having (see Figure 3B):

- a thin, non-zero thickness first dielectric area, which can be of uniform width or extension (in an extension direction $\underline{x}$), and a second dielectric area, thicker than the first, whose thickness can be uniform, and of non-zero width or extension (in the direction $\underline{x}$),

or

- an alternation (or any other form of juxtaposition) of thin, non-zero thickness dielectric areas 32a, 32b, 32c, each of non-zero width or extension 1a, 1b, 1c (in the direction $\underline{x}$), and a plurality of dielectric areas 34a, 34b thicker than the areas 32a, 32b, 32c, each having a non-zero width or extension l'a, l'b (in the direction $\underline{x}$).

One or more semiconductor substrate (bulk) areas can also be formed within the above kind of alternation.

This produces a planar hybrid substrate. Diverse electronic components can then be formed in the semiconductor surface layer 45.

In another embodiment, shown in Figures 4A and 4B, a first substrate is a semiconductor material substrate 130 and the second semiconductor substrate 140 is obtained by forming a juxtaposition (or an alternation or any other distribution) of dielectric (for example SiO_2) areas 144a, 144b, 144c having a first thickness and silicon oxide areas 146a, 146b having a second thickness greater than the first thickness.

The dielectric areas are from 10 nm to 100 nm, from 100 nm to 500 nm or from 100 nm to 5000 nm thick, for

example.

Ion implantation then forms a weakened plane or layer 142 similar to the plane or layer 42 described above. The plane or layer 142 delimits a surface semiconductor film 145.

Because the H+ ions encounter different thicknesses of dielectric or silicon oxide on their trajectory, the layer 142 is not necessarily situated at a uniform thickness relative to the surface 147 of the substrate 140, as shown in Figure 4A. In some cases, the beam of ions ignores the variations in the thickness of the dielectric or silicon oxide.

The two substrates 130 and 140 prepared in this way are then assembled using one of the techniques already mentioned above (wafer bonding, bonding or adherent contact, for example by molecular adhesion).

A portion of the substrate 140 is then eliminated or detached by a treatment that causes a fracture along the weakened area or plane 142, as already described with reference to Figure 3B, leaving the layer or film 145 on the buried dielectric or oxide layer.

Fracturing the substrate in which the weakened layer is formed (the portion situated on the opposite side to the assembly interface of the two substrates) can be followed by a finishing step, for example a thinning step to flatten out irregularities caused by the possibly varying depth of the layer 142, for example by polishing, in particular mechanical/chemical polishing, etching, or sacrificial oxidation. A localized or overall step of thickening the silicon film is equally possible, for example by epitaxial growth.

A semiconductor component or element or a substrate is thus formed having (see Figure 4B):

- a thin, non-zero thickness dielectric layer (in this example a layer of oxide SiO_2), whose thickness can be uniform, of non-zero width or extension (in an extension direction $\underline{x}$), and a thicker dielectric area (in

this example an area of oxide SiO_2), whose thickness can be uniform, and of non-zero width or extension (in the direction $\underline{x}$), or

- an alternation (or any other form of juxtaposition) of thin, non-zero thickness dielectric layers (for example SiO_2 layers) 144a, 144b, 144c, whose thickness can be uniform, each of non-zero width or extension (in the direction $\underline{x}$), and thicker dielectric layers (in this example SiO_2 layers) 146a, 146b, whose thickness can be uniform, and each of non-zero width or extension (in the direction $\underline{x}$).

One or more silicon or semiconductor substrate (bulk) areas can also be formed within the above kind of alternation.

Thus a planar hybrid substrate is again obtained. The substrate can also have thin semiconductor or silicon surface areas and thicker semiconductor or silicon surface areas. Diverse electronic components can therefore be produced on the same substrate in the silicon or semiconductor surface layer 145, and in particular components using different technologies, for example FP SOI components and PD SOI components.

In a further embodiment, shown in Figures 5A and 5B, a first substrate is an unprocessed semiconductor (for example silicon) substrate 230 in which dielectric (for example SiO_2) areas 232a, 232b are produced alongside unprocessed silicon areas. These dielectric areas have thicknesses from 10 nm to 100 nm, from 100 nm to 500 nm or from 100 nm to 5000 nm, for example.

A second substrate 240 is obtained by implanting atoms or ions, for example hydrogen ions, forming a layer 242 similar to the layers 42 and 142 described above.

The two substrates 230 and 240 prepared in this way are then assembled using one of the techniques already mentioned (wafer bonding, bonding or adherent contact, for example by molecular adhesion).

The portion of the substrate 240 on the side

opposite the face 241 at which the substrates are assembled is then eliminated or detached, as already described above in connection with Figure 3B.

This forms a hybrid planar semiconductor structure or semiconductor component or element (see Figure 5B) having an alternation (or any other form of juxtaposition or distribution) of dielectric areas 232a, 232b (in this example oxide SiO_2 areas), which can have different thicknesses, and unprocessed silicon or semiconductor areas.

Diverse electronic components can then be produced in the semiconductor or silicon surface layer 245, in particular in the portion of the layer on top of the dielectric or silicon oxide areas.

In a further embodiment, shown in Figures 6A and 6B, a first substrate is an unprocessed silicon or semiconductor substrate 330 and the second substrate 340 is obtained by forming a juxtaposition of dielectric or silicon oxide areas 344a, 344b and unprocessed silicon or semiconductor areas and then implanting ions, for example hydrogen ions, to form a layer 342 similar to the layer 42 described above. As already explained above in connection with Figure 4a, because the ions encounter different thicknesses of dielectric or silicon oxide on their trajectory, the layer 342 is not necessarily situated at an uniform thickness relative to the surface 341 of the substrate 340.

The two substrates 340 and 330 prepared in this way are then assembled using one of the techniques already mentioned (wafer bonding, bonding or adherent contact, for example by molecular adhesion).

A portion of the substrate 340 is then eliminated, as already described above in connection with Figure 3B. A finishing thinning or thickening step, as already described above in connection with Figure 4B, flattens out irregularities caused by the varying depth of the layer 342.

This forms a hybrid planar semiconductor structure or semiconductor element, substrate or component (Figure 6B) having an alternation (or any other form of juxtaposition or distribution) of dielectric areas 344a, 344b (in this example oxide SiO_2 areas), which can have different thicknesses, and unprocessed silicon or semiconductor areas.

Diverse electronic components can then be produced in the silicon or semiconductor surface layer, in particular in the portion of the layer on top of the dielectric or silicon oxide areas 344a, 344b.

Any combination of the techniques described above can be envisaged. In particular, any juxtaposition of dielectric or silicon dioxide areas with different thicknesses and/or silicon or semiconductor surface areas with different thicknesses and/or dielectric or silicon dioxide areas and silicon or semiconductor substrate areas can be produced in the same substrate or component.

In this way it is possible to produce a continuous dielectric or silicon dioxide layer having an alternation or succession of thinner areas, possibly of uniform thickness, and thicker areas, also possibly of uniform thickness.

Accordingly, in the example shown in Figures 7A and 7B, a first substrate 430 is an unprocessed silicon or semiconductor substrate in which is formed a juxtaposition (or alternation or any other form of distribution) of dielectric or silicon oxide areas 432a, 432b having a particular first thickness, thinner dielectric or silicon oxide areas 434a, 434b, and silicon or semiconductor substrate areas 436. Figure 7B shows only one such silicon area 436, but the same substrate can include several such areas. The oxide areas can be from 10 nm to 100 nm, 100 nm to 500 nm or 10 nm or 100 nm to 5000 nm thick, for example.

The second substrate 440 is obtained by forming a juxtaposition of dielectric or silicon oxide areas 444a,

444b having a particular first thickness, thinner dielectric or silicon oxide areas 448a, 448b, and silicon or semiconductor substrate 446 areas. The thicknesses of the oxide areas or layers can be in the ranges just indicated.

Implanting hydrogen (or other) ions then forms a layer 442 similar to the layer 42 described above. Because the H+ ions encounter different thicknesses of dielectric or silicon oxide on their trajectory, the layer 442 is not necessarily situated at a uniform thickness relative to the surface 441 of the substrate 440, as already indicated above in connection with Figure 4A.

The two substrates 430 and 440 prepared in this way are then assembled by one of the techniques already mentioned above (wafer bonding, bonding or adherent contact, for example by molecular adhesion).

A portion of the substrate 440 is then eliminated or detached, as already described above with reference to Figure 3B. Fracturing the substrate in which the weakened layer is formed (the portion on the opposite side to the assembly interface of the two substrates), can be followed by a finishing step, as already described above in connection with Figure 4B, for example.

This forms a hybrid planar semiconductor element or substrate having (see Figure 7B):

- two or more dielectric or oxide areas 452a, b having two different thicknesses, each of which can be uniform, and possibly a silicon or semiconductor substrate area 456, these two or three areas each having a non-zero width or extension (in an extension direction x), or

- an alternation (or any other form of juxtaposition) of dielectric or oxide areas 452a, b, 454a, b, c, d, 458a, b, and possibly silicon or semiconductor substrate areas 456, the dielectric or oxide areas 452a, b having a first thickness different

from a second thickness of the dielectric or oxide areas 454a, b, c, d, which two thicknesses can be uniform and both different from a third thickness of the areas 458a, b, each of these areas having a non-zero width or extension (in the direction x).

There is also obtained, in the same substrate, an alternation or juxtaposition of different thicknesses of the silicon or semiconductor surface layer.

Instead of this, it is equally possible to produce a dielectric or oxide layer of single or uniform thickness in one of the substrates, for example the substrate 430, the substrate 440 being prepared as indicated above (with one or more dielectric or oxide layers with different thicknesses), assembling the two substrates producing a structure (not shown) also with different dielectric or oxide thicknesses, or a continuous dielectric or oxide layer having different thicknesses, which can be uniform.

Diverse electronic components can then be produced in the silicon or semiconductor surface layer 445, in particular in the portion of the layer on top of the dielectric or silicon oxide areas. Diverse components can also be produced in the different thickness areas of the surface layer 445, thus forming FD SOI and PD SOI components on the same substrate.

A substrate used in the context of the present invention and which can have different thicknesses of silicon dioxide can be produced by a method like that illustrated by Figures 8A-8E.

In Figure 8A, silicon dioxide areas 532a, 532b which are a few hundred nm thick, for example 400 nm thick, are produced on a substrate 530 by LOCOS (locally oxidized silicon) growth through a mask 531, for example a Si_3N_4 mask. These areas can take the form of patches, strips or more complex shapes.

The mask is then removed (Figure 8B), leaving the silicon oxide areas 532a, 532b. Note that, at this stage, the substrate is no longer flat.

It is then possible to carry out a leveling step, for example by mechanical/chemical polishing (Figure 8C), which yields a substrate with silicon dioxide areas 534a, b juxtaposed to the silicon of the substrate itself. The substrate is that shown in Figure 5A or 6A, for example.

In a variant (see Figure 8D), a layer 533 of surface oxidation of the substrate is produced from the Figure 8B structure and the resulting structure (see Figure 8E) is then leveled, for example by mechanical/chemical polishing, to leave a surface oxidation layer 535.

A layer with a thickness of a few hundred nm (for example 300 nm) can be removed in this way, leaving a juxtaposition of silicon dioxide areas with different thicknesses. This type of substrate is shown in Figures 3A, 4A. It is also possible to carry out leveling first (see Figure 8C), followed by surface oxidation (see Figure 8E).

Figures 9A-9D show another method that can be used in the context of the present invention.

In Figure 9A, trenches 632a, 632b are etched, for example dry etched through a mask 634, into a silicon substrate 630 to a depth of a few tens of nm, for example 100 nm.

The mask is then removed (see Figure 9B) after which the surface of the substrate is thermally oxidized or a silicon dioxide layer is deposited, forming a silicon dioxide layer 636 having a thickness of a few hundred nm, for example 400 nm.

It is then possible to carry out a leveling step, for example by mechanical/chemical polishing (see Figure 9C), which yields a substrate having silicon oxide areas 634a, b juxtaposed to the silicon of the substrate itself. The substrate is that shown in Figure 5A or 6A, for example.

In a variant (see Figure 9D), the structure shown in Figure 9B is flattened, but less so than in Figure 9C, leaving a silicon dioxide layer 638 with a thickness of a

few hundred nm, for example approximately 100 nm. This produces a juxtaposition of silicon dioxide areas with different thicknesses on the surface of the silicon substrate 630. This type of substrate is shown in Figures 3A, 4A.

Note the following difference between the two variants shown in Figures 9C and 9D. In the second case (Figure 9D), polishing stops in the oxide (SiO_2) layer. In the first case, the silicon is bared and can serve as a stop layer. Selective polishing methods can then be used.

Methods other than those described above with reference to Figures 8A to 9C can be used, in particular any method using a combination of techniques for depositing oxide or surface oxidation, leveling or etching, yielding a structure such as that shown in Figure 8C, 8E, 9C or 9D, regardless of the order in which these operations are conducted. These processes produce uniform thickness silicon dioxide areas such as the areas 534a, 534b, 634a, 634b or continuous layers of oxide with varying thickness; the thickness is locally uniform except at points or in areas of discontinuity between two different thickness oxide portions.

Note that the areas 532a, 532b, 534a, 534b, 634a, 634b can be any shape, for example in the form of circular patches, or extend linearly in a direction perpendicular to the plane of Figures 8B, 8C and 9C. The same goes for the silicon oxide layers, such as the layers 533, 535, 636, 638. Generally speaking, the structures from Figures 3A-7B can also be considered to extend in a direction perpendicular to their plane.

All the embodiments described above prevent or limit the dislocations and stresses encountered with the prior art technique described with reference to Figure 2.

Figures 10A and 10B show another embodiment of a component or a structure according to the invention. This embodiment uses the SIMOX technique based on

implanting oxygen ions. It also produces a planar hybrid structure or component, although it does not avoid the problems of stresses and dislocations resulting from the use of the Figure 2 technique.

In a first step (see Figure 10A), a mask 200 is used to form a dielectric area in a semiconductor (for example silicon) substrate 205, for example a silicon dioxide area 160, having a first thickness (typically a few hundred nanometers, for example 100 nm or 200 nm).

This is achieved by implanting oxygen ions O++ at a first energy and at a first dose.

In a second step (see Figure 10B), a second mask 210 is used to select another area of the substrate and to implant therein oxygen O++ ions at a second energy and a second dose different from the first energy and/or the first dose used in the first step. This produces in the substrate 205 a silicon dioxide area 180 having a second thickness different from the first thickness (also a few hundred nanometers, for example 400 nm or 500 nm).

The method of Figures 10A and 10B does not use bonding or assembly of substrates, but nevertheless produces a hybrid planar structure or component.

As already indicated above, using the SIMOX technique results in the appearance of non-homogeneous stresses and stresses in the substrate.

Also, swelling or differences in flatness at the surface above the implanted areas are observed.

The buried oxide or dielectric layers produced by the SIMOX technique are of poorer quality and less dense than those obtained using deposition and oxidation techniques.

These buried areas also have breakdown voltages somewhat different from areas produced by the other techniques.

Overall, components obtained by the SIMOX technique are relatively easy to distinguish from those obtained by the other techniques.

The invention can also produce structures having varying surface layer thicknesses, for example by carrying out a step of local thinning of the substrate or of the silicon or semiconductor surface layer 45 (see Figure 3), 145 (see Figure 4B) or 245 (see Figure 5B), or of the layer or the substrate from Figure 6B, as indicated in chain-dotted outline in those Figures, or in Figure 7B.

To be more precise, a local thinning step (for example by etching or sacrificial oxidation) produces a silicon or semiconductor surface layer of varying thickness, with areas 46, 47, 139, 141, 143, 243, 247, 343, 443, 447, 449 having a surface Si thickness less than the thickness of other surface Si or semiconductor areas, or with alternating areas of the surface Si or semiconductor layer having a first thickness alternating with a second thickness different from the first thickness.

After local thinning, the silicon surface layer still provides electrical continuity between the different areas.

In a variant, the thickness of the dielectric or oxide layer is uniform and the thickness of the silicon or semiconductor surface layer varies.

Accordingly, in Figure 11A, a dielectric or silicon dioxide layer 272 with a uniform thickness is produced in a substrate 270 and the substrate 280 is prepared like the substrate 40 from Figure 3A, for example, the weakened layer or plane 274 being similar to the layer 42 in Figure 3A.

The two substrates 270, 280 produced in this way are then assembled, again using a wafer bonding, bonding or adhesion contact technique.

A portion of the substrate 280 is then eliminated by treatment causing fracture along the weakened plane 274.

Local thinning using an etching or sacrificial oxidation method, for example, or local leveling produces

a silicon or semiconductor surface layer of varying thickness, with a first thickness and a second thickness in the areas 276.

The silicon or semiconductor surface layer again provides electrical continuity between the different areas after local thinning.

In this way varying thicknesses can be obtained for the semiconductor or silicon layer, for example from 10 nm to 50 nm or 70 nm in one area and from 50 nm, 70 nm or 80 nm to 250 nm in another area.

Figures 12A and 12B show another embodiment of a component according to the invention. This embodiment uses the surface oxidation or deposition technique described above with reference to Figures 8A to 9C and the SIMOX technique described above with reference to Figures 10A and 10B.

For example, as shown in Figure 12A, a first dielectric area 832, which can include subareas with different thicknesses, is produced in a semiconductor substrate 830, for example as described with reference to Figures 7A and 7B.

As shown in Figure 12B, a mask 810 is then used to produce, by means of ion implantation, in particular by implanting oxygen ions in the case of silicon dioxide, a dielectric area 880 which can have the same thickness as one of the subareas of the area 832 or a different thickness.

The invention also provides a method and a component shown in Figures 13A and 13B.

The method is similar to the methods already described above, for example with reference to Figures 7A and 7B, with alternating or juxtaposed silicon oxide areas 732, 736 with different thicknesses.

Also included is the formation by etching and deposition of conductive or metal lands 753, 754 which, after a connection is established between the two substrates 730, 740, produce a conductive or metal member

or land 760 establishing a conductive connection in and through the dielectric areas.

The conductive material used can be WSi_2, for example.

In a variant, conductive lands can be produced by doping dielectric or semiconductor areas of the substrates 730, 740.

Metal or conductive lands can be formed by any of the methods already described above, in particular in connection with Figures 3A-9C.

Whatever production method is envisaged, a hybrid planar and for example SOI structure, component or substrate is obtained including, on the same substrate, buried dielectric or silicon dioxide areas having different thicknesses and/or silicon or semiconductor surface areas having different thicknesses. The semiconductor surface layer is continuous between the different areas, providing electrical continuity between the different areas.

There can be juxtaposed in this way FD SOI areas and PD SOI areas and substrate (bulk) areas or areas having a semiconductor or silicon surface layer from 10 nm to 50 nm or 70 nm thick, for example, and areas having a semiconductor or silicon surface layer from 50 nm, 70 nm or 80 nm to 250 nm thick, for example.

The components, in particular the electronic components, for example transistors, produced in the substrate can then employ different technologies.

Thus Figure 14 shows a portion of a substrate such as that obtained as described with reference to Figure 4B or Figure 7B and in which two MOS transistors 910, 920 each having a gate 912, 922, a drain 916, 926 and a source 914, 924 are produced. The thicker or thinner silicon areas under these transistors produce a fully depleted (FD) SOI component 910 and a partially depleted (PD) SOI component 920.

It is also possible to have an FD area under one

portion of a transistor, for example under its gate and its drain, and a PD area under another portion of the same transistor, for example under its source.

The different areas obtained, for example FD or PD areas, can have a size of 1 square millimeter (mm^2) or more, necessitating no submicron technology for forming the buried oxide layers.

Submicron technologies can be used to produce smaller areas, less than 1 mm^2, for example of the order of a few square micrometers (μm^2) or a few tens of μm^2. For example, it is possible to produce specific areas under the drain and/or source and/or gate areas of a transistor, for example a specific area under the gate 912 of the MOS transistor 910 in Figure 12, the areas situated under the drain and the source of the same transistor being of a different kind because of a different oxide thickness and/or a different silicon layer thickness.

The invention has been described with the material SiO_2 as the insulator in an SOI structure. It nevertheless applies to other dielectric materials, such as Si_3N_4, diamond and sapphire, for example. It also applies to any material with a high coefficient K, such as those described in MRS Bulletin, March 2002, Vol. 27, No. 3, "Alternative Gate Dielectrics for Microelectronics"; such material include, for example, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3) and yttrium oxide (Y_2O_3), and are preferably used to produce thin layers, i.e. layers with a thickness of a few tens of nm, for example from 10 nm to 50 nm.

It is equally possible to produce one or more dielectric areas of a first dielectric material and one or more dielectric areas of a second dielectric material different from the first material.

Thus the areas 534a and 534b in Figure 8C can be of a different kind from each other, and likewise the areas 634a and 634b in Figure 9C or the areas 160 and 180 in

Figure 10C. From this starting point, all combinations are possible using one of the methods described above.

All the above methods, except for the method described with reference to Figures 8A to 8E, can then be used for dielectrics that are not oxides (for example diamond). Deposition techniques are then used.

A weakened plane can be formed by methods other than ion implantation. Thus is it is also possible to produce a layer of porous silicon, as described in the paper by K. Sataguchi *et al.* "ELTRAN® by Splitting Porous Si Layers", Proceedings of the 9th International Symposium on Silicon-on-Insulator Tech. And Device, 99-3, The Electrochemical Society, Seattle, p. 117-121 (1999).

Polishing or etching techniques can be used for thinning the substrates 40, 140, 240, 340, 440, 280, 740 without using ion implantation and without creating a weakened plane.

Finally, the above description relates to the use of silicon as the basic semiconductor material. Other semiconductor materials (for example SiGe, SiC, AsGa, InP, GaN) can be used instead of silicon, the invention applying equally to forming semiconductor on insulator structures (possibly with conductive lands as in Figure 13B).

CLAIMS

1. A method of producing a semiconductor structure, the method comprising:

- forming in a first semiconductor material substrate (30, 140, 230, 340, 430, 732) a first dielectric area (32a-c, 144a-c, 232a-b, 344a-b, 436, 736) having a first thickness and a second dielectric area having a second thickness,

- assembling said first substrate with a second semiconductor material substrate (40, 240, 440), and

- thinning one or both substrates.

2. A method according to claim 1, wherein the first thickness and the second thickness are different.

3. A method according to claim 1, wherein the first thickness and the second thickness are the same.

4. A method according to any one of claims 1 to 3, wherein the first area and the second area are separated by a semiconductor area (245, 436).

5. A method according to any one of claims 1 to 4, wherein the first dielectric area and the second dielectric area consist of two different dielectric materials.

6. A method according to any one of claims 1 to 5, including forming in said first substrate a third dielectric area (432a-b) having a third thickness.

7. A method according to claim 6, wherein the third thickness is different from the first thickness and from the second thickness.

8. A method according to claim 6 or claim 7, wherein the third dielectric area consists of a material different

from the material of the first dielectric area and/or the material of the second dielectric area.

9. A method according to any preceding claim, including forming in the second substrate (440) a first dielectric area (448a-b) of the second substrate.

10. A method according to claim 9, including forming in the second substrate a second dielectric area (444a-b) of the second substrate.

11. A method according to claim 10, wherein the second dielectric area of the second substrate has a thickness different from that of the first dielectric area of the second substrate.

12. A method according to claim 10 or claim 11, wherein the first dielectric area and the second dielectric area of the second substrate consist of two different materials.

13. A method of producing a semiconductor structure, the method comprising:

- forming in a first semiconductor material substrate (270) a dielectric material dielectric area (272),
- assembling said substrate with a second semiconductor material substrate (280), and
- thinning either or both substrates, leaving a surface layer (275) of semiconductor material on the dielectric area, a first area of said surface layer having a first thickness and a second area (276) of said surface layer having a second thickness different from the first thickness.

14. A method according to any one of claims 1 to 13, wherein the two substrates are assembly by molecular

adhesion.

15. A method according to any one of claims 1 to 14, wherein either substrate or each substrate is thinned by forming a weakened area or layer.

16. A method according to claim 15, wherein the weakened area or layer is produced by forming a layer of porous silicon.

17. A method according to claim 15, wherein a weakened area or layer is formed by implanting ions in the first substrate or the second substrate.

18. A method according to claim 17, wherein the ions implanted are hydrogen ions or a mixture of hydrogen ions and helium ions.

19. A method according to any one of claims 1 to 14, wherein the thinning step uses a polishing or etching process.

20. A method according to any one of claims 1 to 19, wherein the dielectric areas are formed by deposition.

21. A method according to any one of claims 1 to 19, wherein the dielectric areas are formed by surface oxidation.

22. A method according to any one of claims 1 to 20, wherein the dielectric materials are chosen from silicon nitride (Si_3N_4), diamond and sapphire.

23. A method according to any one of claims 1 to 21, wherein the dielectric materials are chosen from silicon dioxide (SiO_2), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), lanthanum oxide (La_2O_3) and

yttrium oxide (Y_2O_3).

24. A method according to any one of claims 1 to 23, wherein thinning either or both substrates is followed by a finishing step.

25. A method according to claim 24, wherein the finishing step includes local thinning or local thickening of the substrate.

26. A method according to any one of claims 1 to 25, including a step of forming a conductive or metal portion (752, 754, 760) or a doped area providing a conductive connection between two or more dielectric areas.

27. A method of producing a semiconductor structure, the method comprising:

- a first step of forming in a semiconductor substrate (205) a first dielectric area (160) of a first dielectric material having a first thickness, and
- a second step of forming in the same substrate, by ion implantation, a second dielectric area (180) of a second dielectric material having a second thickness.

28. A method according to claim 27, wherein the second thickness is different from the first thickness.

29. A method according to claim 27 or claim 28, wherein the first step uses ion implantation.

30. A method according to claim 29, wherein ion implantation is effected at different energies and/or doses in the first step and in the second step.

31. A method according to any one of claims 27 to 30, wherein the dielectric material of the second dielectric area is chosen from silicon dioxide (SiO_2) and silicon

nitride (Si_3N_4).

32. A method according to claim 27, wherein the first step of forming the first dielectric area uses deposition and/or surface oxidation.

33. A method according to claim 32, wherein the dielectric material of the first dielectric area is chosen from silicon dioxide (SiO_2), silicon nitride (Si_3N_4), diamond, sapphire, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), lanthanum oxide (La_2O_3) and yttrium oxide (Y_2O_3).

34. A method according to any one of claims 1 to 33, wherein the semiconductor material is silicon, silicon carbide (SiC), gallium arsenide (ArGa), gallium nitride (GaN), SiGe or indium phosphide (InP).

35. A method according to any one of claims 1 to 34, wherein the semiconductor structure is an SOI structure.

36. A method according to any one of claims 27 to 35, including a step of local thinning of a surface layer of semiconductor material.

37. A semiconductor structure comprising, in a semiconductor substrate, a surface layer of semiconductor material and, under said surface layer:

- a first buried dielectric layer (32a-c, 144a-c, 434a-b, 458a-b), referred to as the first dielectric layer, of a first dielectric material, and
- a second buried dielectric layer (34a-b, 146a-b, 432a-b, 454a-c), referred to as the second dielectric layer, the thicknesses of the first and second dielectric layers being different.

38. A structure according to claim 37, wherein the

thicknesses of the respective surface semiconductor layers on top of the first and second dielectric layers are different.

39. A semiconductor structure according to claim 37 or claim 38, including a third buried dielectric layer (452a-b) referred to as the third dielectric layer.

40. A semiconductor structure according to claim 39, wherein the thickness of the semiconductor layer on top of the third dielectric layer is non-zero and different from the thicknesses of the respective semiconductor layers on top of the first and second dielectric layers and/or the thickness of the third dielectric layer is non-zero and different from the thicknesses of the first and second dielectric layers.

41. A semiconductor structure according to any one of claims 37 to 40, wherein the first and/or second dielectric layers are obtained by deposition and/or surface oxidation.

42. A semiconductor structure according to any one of claims 37 to 41, wherein the first and/or second dielectric layers are obtained by ion implantation.

43. A semiconductor structure according to any one of claims 37 to 42, wherein one or more of the dielectric areas has an area of at least one square micrometer.

44. A semiconductor structure according to any one of claims 37 to 42, wherein one or more of the dielectric areas has an area of at most one square micrometer.

45. A semiconductor structure according to any one of claims 37 to 44, wherein the semiconductor area portion on top of the first dielectric area or the second

dielectric area and where applicable the third dielectric area is of the FD SOI type and the semiconductor area portion on top of another of said areas is of the PD SOI type.

46. A semiconductor structure according to any one of claims 37 to 45, wherein the semiconductor area portion on top of the first dielectric area or the second dielectric area and where applicable on top of the third dielectric area has a thickness from 10 nm to 70 nm and a conductive area portion on top of another of the same dielectric areas has a thickness from 50 nm to 250 nm.

47. A semiconductor component having a structure according to any one of claims 37 to 46, and a first electronic component (910) formed in the semiconductor layer on top of the first dielectric layer and a second electronic component (920) in the semiconductor layer on top of the second dielectric layer or where applicable on top of the third dielectric layer.

48. A semiconductor component according to claim 47, wherein the first and/or second electronic component is a transistor.

49. A semiconductor component having a structure according to any one of claims 37 to 46, wherein a first portion of a transistor is produced in the semiconductor layer on top of the first dielectric layer and a second portion of the same transistor is produced on top of the second dielectric layer.

50. A semiconductor component according to claim 47 or claim 49, wherein the transistor is an MOS transistor.