A CIRCUIT AND METHOD FOR CONFIGURING AND REGISTERING A CRYPTOGRAPHIC DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of cryptography. More particularly, the present invention relates to a circuit and method for configuring and registering a cryptographic device.

2. Description of Art Related to the Invention

Currently, many individuals are using personal computers to store and to transmit sensitive information (e.g., confidential, proprietary, etc.) in a digital format. For example, credit card account information occasionally may be transmitted over the Internet to purchase good(s) and/or service(s). Likewise, bank account numbers and bank account balances are transmitted using on-line banking. Due to the sensitive nature of this information, measures have been taken to protect the "integrity" of the information outside the physical confines of the computer; namely, to guarantee that the information has not been altered without authorization. However, such measures fail to protect information within the computer.

As described in U.S. Patent No. 5,539,828 assigned to Intel Corporation, Assignee of the present application, information may be protected within a computer by utilizing cryptographic hardware. The cryptographic hardware includes an integrated circuit (IC) package containing processing logic and dedicated, non-volatile (NV) memory in the IC package (referred to as "device NV memory"). Typically, the cryptographic hardware undergoes an exhaustive configuration phase at a manufacturing facility in which the device NV memory is

configured to contain unique cryptographic information necessary for secure functionality of the cryptographic device such as, for example, a public/private key pair and a digital certificate.

This type of architecture will realize a few disadvantages as cryptographic techniques become more advanced. One disadvantage is that larger, more costly packages will be required because larger amounts of device NV memory will be necessary in order to store greater amounts of cryptographic information. Hence, it would be cost efficient to substantially mitigate the amount of NV memory placed in the cryptographic device in favor of NV memory located elsewhere in the system which is referred to as "system NV memory" herein. Examples of system NV memory include hard disk, NV memory placed on a motherboard or daughter card, etc.

Currently, system NV memory can not be used. The reason is that a reliable, cost-effective technique has not been developed for ensuring that system NV memory, configured and programmed with cryptographic information unique to a certain cryptographic hardware, will be implemented within an electronic system having that cryptographic hardware.

SUMMARY OF THE INVENTION

A method for configuring and/or registering a cryptographic device. With respect to one embodiment of the configuration scheme, a device serial number is loaded into a non-volatile memory of the cryptographic device. Internal to the cryptographic device, a key is generated and loaded into the non-volatile memory of the cryptographic device.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which:

Figure 1 is an illustrative block diagram of an electronic system including a multi-chip module employed as a bridge element.

Figure 2 is a block diagram of a preferred embodiment of the multi-chip module optimally shown as the bridge element of Figure 1.

Figure 3 is an illustrative embodiment of the processing subsystem of Figure 1 including the cryptographic device.

Figure 4 is an illustrative embodiment of a substrate of Figure 3.

Figure 5 is an illustrative flowchart of the configuration scheme performed by the cryptographic device of Figure 2.

Figure 6 is an illustrative flowchart of the registration scheme performed by the cryptographic device of Figure 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention relates to a system and technique for configuring a cryptographic device to utilize non-resident, non-volatile (NV) memory and for registering the cryptographic device from a remote location. In the following description, some terminology is used in general to describe certain features of the present invention. For example, an "electronic system" is generally defined as any hardware product having information processing functionality such as, for example, a computer, a facsimile machine and a printer. "Information" is generally defined as one or more bits of data, address, and/or control information.

In addition, the following terminology is used to identify various types of cryptographic information. A "key" which is an

encoding and/or decoding parameter used by conventional cryptographic functions such as a symmetric key cryptographic function (e.g., a Data Encryption Standard "DES" based function) or a public-key cryptographic function (e.g., a Rivest, Shamir and Adleman (RSA) based function). A "digital certificate" is generally defined as any information (e.g., a public key) used for user authentication. The information is encrypted with a private key (PRKCA) of a certification authority, namely any person or entity in a position of trust to guarantee or sponsor the digital certificate such as a bank, governmental entity, trade association, original equipment manufacturer, and the like.

Referring to Figure 1, an illustrative embodiment of an electronic system 100 employing the present invention is shown. In this embodiment, the electronic system 100 comprises a chipset 110 interconnecting a number of subsystems. Examples of these subsystems may include, but are not limited or restricted to a processing subsystem 120, a memory subsystem 130, and an input/output (I/O) subsystem 140. Collectively, these subsystems 120, 130 and 140 control the functionality of electronic subsystem 100.

More specifically, as an illustrative embodiment, processing subsystem 120 includes at least one central processing unit (CPU) 121. CPU 121 is connected to chipset 110 via a host bus 122. The memory subsystem 130 usually includes one or more banks of volatile memory (not shown) such as any type of dynamic random access memory (DRAM), and/or static random access memory (SRAM). It is contemplated, however, that system NV memory may be used in memory subsystem 130 in lieu of or in addition to volatile memory.

Furthermore, I/O subsystem 140 includes "n" peripheral device(s) 141_1-141_n ("n" is a positive whole number) which are coupled to an I/O bus 142. Examples of a peripheral device include a mass

storage device 1411 (e.g., a hard disk drive, a digital tape drive, a floppy disk drive, and a digital versatile disk "DVD" player).

To provide cryptographic functionality, a cryptographic device 150 may be connected to chipset 110 through a dedicated bus 160. Of course, as alternative system embodiments, cryptographic device 150 may be placed in communication with another bus in computer 100 such as host bus 121 or another processor-based bus like a backside bus (not shown), or perhaps I/O bus 142.

Referring to Figures 2, an illustrative embodiment of cryptographic device 150 of Figure 1 is shown. Cryptographic device 150 includes an integrated circuit (IC) device 200 contained within a package 205 which protects IC device 200 from damage and harmful contaminants. IC device 200 comprises a processing unit 210 integrated with a small amount of device NV memory 215. Optionally, a random number generator 220 may be implemented within package 205 as a separate device connected to processing unit 210 through an internal bus 225 (as shown) or integrated within processing unit 210. Random number generator 220 is used to produce one or more keys when cryptographic device 150 is operating in a configuration mode.

Although the embodiment of the cryptographic device 150 shown in Figure 2 may be implemented as a co-processor, it is contemplated that a variety of different embodiments could be selected. For example, cryptographic device 150 may be implemented within a disk controller, on a "smart" card (a form fraction shaped like a credit card but having a micro-controller), or within a cartridge-like processor package including CPU 121 as described below in Figures 3-4. Other alternative embodiments may include incorporating the functionality of the cryptographic device into a chipset or within CPU 121.

Referring to Figure 3, a perspective view of an alternative system embodiment, implementing cryptographic device 150 within a

processing subsystem 120, is shown. IC components (including cryptographic device 150) are placed on a processor substrate 300 formed from any type of material upon which IC components (not shown) can be attached through well-known techniques (e.g., solder connection, etc.). The processor substrate 300 is substantially covered by a rectangular-shaped package 310 in order to protect the IC components from damage or harmful contaminants. Processor substrate 300 includes a connector 320, preferably adapted to establish a mechanical and electrical connection with a motherboard for example. As shown, connector 320 may include a standard male edge connector (as shown) or perhaps a female edge connector.

As shown in Figure 4, the IC components of processor substrate 300 include, but are not limited or restricted to CPU 121, memory 330 and cryptographic device 150. For communications with CPU 121, cryptographic device 150 may be placed on (i) a backside bus which is usually connected with memory 330, (ii) a front-side bus which is usually connected with external connector 320, or (iii) a dedicated internal bus. Of course, placement of this cryptographic device 150 is arbitrary so long as latency and other requisite conditions are maintained. Although not shown, discrete components (e.g., capacitors, oscillators, resistors, inductors, etc.) are attached to processor substrate 300 in a selected manner to, among other things, maximize routability and decrease length of communication lines between these IC components.

Referring now to Figure 5, a preferred embodiment of a configuration scheme utilized by the cryptographic device is shown. At manufacture, the cryptographic device undergoes a configuration phase in order to load only a limited amount of cryptographic information into its integrated device NV memory. One embodiment for the configuration phase involves the use of a certification system including (i) a programming mechanism having a device carrier sized to

accommodate the cryptographic device, and (ii) a database (e.g., a server, personal computer, mainframe, etc.) which receives cryptographic information from the programming mechanism. To avoid obscuring the present invention, only the function operations of the programming mechanism will be described.

When turned-on, the programming mechanism initially supplies power and provides predetermined control information into appropriate leads of the cryptographic device via the device carrier. This control information places the cryptographic device into a configuration mode (Step 400). After being placed in the configuration mode, the cryptographic device initially receives a unique device serial number (DSER) from the programming mechanism (Step 405). Normally sized with a sufficient number of bits to avoid duplication (e.g., 32 or 64 bits), DSER is stored in the integrated device NV memory of the cryptographic device and is provided to the database (Step 410). DSER is used by the database as an index for a table of pointers. Each pointer is responsible for addressing one or more locations in memory which contain cryptographic information uniquely associated with the cryptographic device identified by its DSER.

Additionally, by supplying power to the cryptographic device, the random number generator is powered to produce random numbers used in generating a unique symmetric key (SK) and a public/private key pair (Step 415). The public key (PUK) is exported to the database without undergoing any modification (Step 420). However, the private key (PRK) is encrypted using an encryption algorithm (e.g., DES pre-loaded in memory of the cryptographic device), and thereafter, exported to the database (Step 425). More specifically, PRK is encrypted with SK (producing $E_{SK}(PRK)$) before being exported to the database. As a result, the cryptographic device contains a minimal amount of cryptographic information, namely SK and DSER, while an indexed location of database includes the majority of the cryptographic information.

Optionally, as represented by dashed lines, it is contemplated that a digital certificate associated with PUK and DSER may be loaded into the database at a later time, potentially even after the cryptographic device has been sent to an original equipment manufacturer (OEM) for placement in the electronic system (Step 430). The digital certificate includes at least PUK encrypted with a private key of the manufacturer in this embodiment, which could be used for subsequent authentication of the cryptographic device. It is contemplated, however, that DSER may be included in the digital certificate.

After the cryptographic device has been installed into the electronic system having sufficient system NV memory, communications may be established to the database of the manufacturer for registration purposes. This registration scheme does not require a secure communication channel because PRK has been encrypted. Registration may be performed by any downstream customer, including an OEM before shipment of the electronic system to the end user, or the end user. For the later case, the electronic system may be loaded with system software having a registration subroutine. During initialization of the electronic system by system software, the registration subroutine would assist in establishing communications with the database in order to retrieve and download cryptographic information unique to the electronic system. This registration scheme may be transparent to the end user or may require active participation by the end user in agreeing to certain terms and conditions (e.g., releasing the manufacturer from liability, etc.).

Referring now to Figure 6, an illustrative embodiment of the registration scheme between the database of the manufacturer and the downstream customer (OEM, end user, etc.) is shown. First, a communication channel has to be established between the database and the electronic system implemented with the cryptographic device (Step 600). This may be accomplished over the Internet, through a dedicated

phone line or over any other communication link. Next, the electronic system transmits a message, including DSER obtained from its cryptographic device, to the database over the communication channel (Step 605). The database receives the message and utilizes DSER as an index in searching for cryptographic information associated with the cryptographic device identified by DSER (Step 610). This cryptographic information (PUK, E_{SK}(PRK), and digital certificate) is transmitted over the communication channel to the electronic system and loaded into system NV memory of the electronic system (Steps 615-620). Thus, the cryptographic device now is fully functional to support public-key cryptography because it has access to its PUK and PRK because E_{SK}(PRK) can be decrypted with SK already integrated in its device NV memory.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed is:

1. A method for configuring a cryptographic device comprising the steps of:

loading a device serial number into a non-volatile memory of the cryptographic device;

generating a symmetric key within the cryptographic device; and

loading the system key into the non-volatile memory of the cryptographic device.

2. The method of claim 1 further comprising the step of:

discontinuing any further loading of information within the non-volatile memory of cryptographic device after the device serial number and the symmetric key have been loaded.

3. The method of claim 1 further comprising the step of:

loading the device serial number into a database remotely located from the cryptographic device.

4. The method of claim 3 further comprising the steps of:

generating at least a public key and a private key within the cryptographic device;

sending the public key to the database;

encrypting the private key with the key to produce an encrypted private key; and

sending the encrypted private key to the database.

5. The method of claim 4 further comprising the steps of:

providing a public key to a certification authority; and



encrypting the public key with a private key of the certification authority to produce a digital certificate; and

sending the digital certificate to the database to accompany the public key and the encrypted private key.

6. The method of claim 1, wherein the device serial number is unique and distinct from device serial numbers for other cryptographic devices.

7. The method of claim 1, wherein the key is a symmetric key.

8. The method of claim 7, wherein the symmetric key is unique and distinct from other symmetric keys associated with the other cryptographic devices.

9. The method of claim 1, wherein the non-volatile memory is integrated within processing logic of the cryptographic device.

10. A method for registering a cryptographic device comprising the steps of:

establishing a communication channel between a database and an electronic system implemented with the cryptographic device, the cryptographic device including non-volatile memory storing a key and a device serial number;

transmitting a message to the database, the message including the device serial number contained in the cryptographic device; and

receiving a public key and a private key encrypted with the key associated with the cryptographic device.

11. The method of claim 10 further comprising the step of:



loading the public key and the private key encrypted with the key into a non-volatile memory element of the electronic system.

12. The method of claim 10, wherein the communication channel is not secure.

13. The method of claim 10, wherein the key is a symmetric key.

14. The method of claim 10, wherein prior to the receiving step, the method further comprising the steps of:

receiving the message including the device serial number by the database;

using the device serial number as a lookup index; and

transmitting the public key and the private key encrypted with the key to the electronic system.

15. The method of claim 10 further comprising the step of :

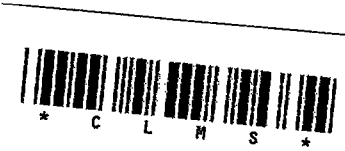
receiving a digital certificate being the public key encrypted with a private key of a certification authority.

16. A system comprising:

a chipset;

a non-volatile memory element coupled to the chipset; and

a cryptographic device coupled to the chipset, the cryptographic device including processing logic having a small amount of device non-volatile memory, the non-volatile memory containing a device serial number and a symmetric key.



17. The system of claim 16, wherein the non-volatile memory includes at least a public key associated with the cryptographic device and a private key encrypted with the symmetric key.

18. The system of claim 16, wherein the system is capable of establishing communications with a database to load the public key and the encrypted private key into the non-volatile memory.

19. A processing subsystem comprising:
a substrate;
a processor coupled to the substrate;
a cryptographic device coupled to the substrate; and
a bus interconnecting the processor and the cryptographic device.

20. The processing subsystem of claim 19, wherein the cryptographic device includes
a processing unit;
a non-volatile memory integrated into the processing unit, the non-volatile memory includes a key and device serial number; and
a random number generator.

21. The processing subsystem of claim 19, wherein the random number generator of the cryptographic device is integrated within the processing unit.

22. The processing subsystem of claim 19, wherein the bus is a backside bus.

23. The processing subsystem of claim 19 further comprising a plastic cartridge generally enclosing the substrate with exception to a connector located on an edge of the substrate.

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