

PATENT SPECIFICATION

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(54) DIGITAL REMOTE CONTROL FOR ELECTRONIC SIGNAL RECEIVERS

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with remote control adjustment of electronic signal receivers and more particularly to a system for providing substantially simultaneous remote actuation of a plurality of control functions in a color television receiver.

Remote control tuning of television receivers has, in the past, been accomplished in many different ways. In one type of known system, a remote control transmitter is utilized to transmit a different ultrasonic frequency signal for actuation of each selected remote control function. Thus, where eight functions are to be controlled (e.g., volume up and down, color up and down, tint plus or minus, channel up and down), eight different frequencies in the vicinity, for example, of 30 to 40 KHz are transmitted and received in the ultrasonic remote control system. The use of a plurality of ultrasonic frequencies requires that the remote control receiver have a relatively large bandwidth. A receiver with a relatively large bandwidth is generally more susceptible to extraneous noise signals than one with a narrower bandwidth. Further, receiving and transmitting transducers having relatively broad bandwidth generally have a lower sensitivity than their narrow bandwidth counterparts, thus requiring the transmitter to expend a relatively large amount of energy to effect reliable signal reception.

According to the present invention there

is provided a remote control system for a television receiver which provides substantially simultaneous control of a plurality of television receiver functions in response to coded instruction signals from a remote location, comprising a remote control transmitter, each of a corresponding plurality of remote controls of the remote control transmitter being capable of being set to any of a plurality of operating conditions, the remote control transmitter being responsive to said remote controls to produce bi-phase coded instruction signals; and wherein a remote control receiver is responsive to said bi-phase coded instruction signals from said remote control transmitter which are binary coded control function signals representative of desired operating conditions of said television receiver functions to be controlled.

A second aspect of the invention provides a remote control receiver for use in a remote control system, for receiving coded instruction signals which comprise remote control binary instruction signals together with a predetermined verification pattern, and clock pulse decoding information in the form of serially encoded bi-phase level binary instruction signals; said remote control receiver comprising: receiving means for receiving said coded instruction signals; decoding means for extracting said remote control binary instruction signal from said serially encoded bi-phase level binary instruction signals; authenticating means coupled to said decoding means for comparing each remote control binary instruction signal with the previous instruction signal and providing a parallel binary representation of the compared remote control binary instruction signal and a latch signal; and control means responsive to said parallel binary remote control instruction and latch signals for actuating remotely controllable signal receiver

functions.

In accordance with one embodiment of the present invention, a plurality of functions (e.g., eight) are controlled utilizing only two frequencies. The control signal for each separate function is identified according to its position in a sequence of control signals which are accompanied by an identification code.

Furthermore, remote control actuators on the typical remote control transmitter are comprised of two-position (on-off) push-button switches. These switches are generally quite distinct from their associated counterparts on the television receiver. Accordingly, manipulation of the respective controls on the television receiver and on the remote control transmitter for achieving the same results are generally quite different. To simplify operation of the television remote control system, a remote control transmitter is provided having controls that may be manipulated in the same manner as their respective counterparts on the television receiver.

Prior remote control systems have typically been susceptible to erroneous signals caused by multipath reception. Multipath reception is generally caused by reflections of the transmitted signal from different objects in the vicinity of the receiver.

Other problems which have been encountered in prior systems include false triggering of the receiver control circuits by signals generated from such items as jingling keys, the bell in a telephone and harmonic oscillations of the television receiver's horizontal sweep generator.

An embodiment of the present invention which utilizes a relatively narrow transmitting and receiving bandwidth and further is relatively unaffected by extraneous noise signals incorporates two signal processing units, one a transmitter and one a receiver, for use with a remotely controllable electronic signal receiver such as a television receiver which provides control of signal receiver functions in response to coded instruction signals from remote controls. Each of the remote controls is capable of being set to any of a number of operating conditions. Each signal processing unit is responsive to the coded instruction signals from the remote controls and processes them to produce further coded signals. The coded signals from the remote controls are pulse arrangements which represent the ultimate operating condition which the corresponding controlled signal receiver function is to assume.

One signal processing unit is a transmitter incorporating the remote controls. The remote controls each produce digital signals representative of the operating posi-

tion of the remote control, which is the desired signal receiver operating condition. The transmitter also includes a clock generator, a pattern generator which produces an identification signal, a serial encoder for encoding the digital and identification signals at the clock rate, and another encoding arrangement for converting the serially encoded binary instructions into a form including the clock pulses, so that decoding is made easier.

The transmitter embodiment also includes a frequency-shift oscillator which is frequency modulated by the digital information to produce logical ones and zeros of the encoded signals in the form of pulses at two different frequencies. An amplifier and transducer for broadcasting the frequency-modulated binary instruction signals complete the remote control transmitter.

The second signal processing unit is a remote control receiver which is adapted to receive the broadcast coded remote control instruction signals from the transmitter. The remote control receiver receives the frequency-modulated digital transmission and converts it to a digital pulse form. A decoder separates the clock information from the digital instruction signal and identification signal.

The receiver embodiment also includes a means for verifying the authenticity of a transmission sequence by comparing it with the previous sequence. This is done by use of a pattern decoder which identifies each transmission sequence, together with shift registers for storing and remembering the instructions, a comparator for comparing the binary instructions in the registers, and a sequence generator for controlling the comparison. A data register responds to the comparator and stores a digital instruction which has been authenticated. The data register stores the authenticated instruction until receipt of a newly authenticated instruction, and makes the authenticated digital instruction signal available at the receiver output for application to a suitable control function in the television or other signal receiver.

A better understanding of this invention may be derived with reference to the following specification and the drawings of which:

FIGURE 1 is a block diagram of a remote control transmitter embodying the present invention;

FIGURE 2 is a block diagram of a remote control receiver in accordance with the present invention;

FIGURES 3a-3k are representations of waveforms associated with the apparatus of FIGURES 1, 2, 4 and 5;

FIGURE 4 is a schematic diagram of an

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encoder circuit as utilized with the apparatus of FIGURE 1; and

FIGURE 5 is a schematic diagram of a decoder as utilized with the apparatus of FIGURE 2.

With reference to FIGURE 1, a series of, for example, four operator controlled binary code switches 10, 12, 14 and 16 is coupled to a sequential encoder 18. A pattern generator 20 is further coupled to the sequential encoder 18. Signals provided by sequential encoder 18 are coupled to a combined clock and data encoder 22. Signals produced at the output of encoder 22 are coupled to a frequency shift oscillator 26, the output of which is coupled to an output amplifier 28. A clock signal generator 24 is coupled to encoders 18 and 22 for providing digital timing signals. A transducer 30 is coupled to the output of amplifier 28 for transmitting desired messages. A source of supply voltage 32 is coupled through a switch 34 to the respective electrical circuits within the transmitter.

In the operation of the above-described apparatus, binary code switches 10, 12, 14 and 16 are adjusted to select a desired channel and operating levels of, for example, color, volume and brightness. Switches 10 through 16 each produce a binary coded output instruction signal on a respective group of four lines (each group being shown as one line).

This binary coded instruction signal is a pulse arrangement in parallel array, representative of the operating position of the switch 10 to 16 but also representative of the ultimate operating position which the corresponding television receiver function (color, volume and brightness) is to assume. The binary output codes of the respective switches may be changed by adjusting an appropriately connected rotary knob, thumb wheel or sliding member. The type of actuating control (knob, wheel, etc.) on each switch may be selected in accordance with the appropriate counterpart utilized on the television receiver to provide a direct correlation for the viewer between local and remote adjustment of the receiver controls.

Upon adjustment (e.g., rotation) of each of the binary code switches, a binary output signal, for example, representing one of the states 0 through 15, is produced at each switch. The combination of logical ones and zeros produced on the four output lines of each switch may be generated by having contacts associated with each switch for grounding those lines on which a logical zero is desired and coupling the non-grounded lines to a source of supply voltage having a level representative of a logical "one". Binary signals produced by

switches 10, 12, 14 and 16 are ultimately to be utilized to control amplitude levels and channel selection of the remotely operated television receiver. Although switches 10-16 are illustrated as being used to control channel number, color, volume and brightness, other control functions may be substituted or added.

An on-off power control function is derived from the selection switch 10 by utilizing a particular switch output code, for example, four binary zeros to represent the power-off condition. Selection of a channel number other than zero causes the transmitter to broadcast an "on" command together with the selected channel number. Although switches 10-16 are described as having four bits of information and accordingly four output lines, a larger or smaller number of output lines and, therefore, bits of information may also be utilized.

Pattern generator 20 is utilized to produce a preselected binary code pattern which is thereafter used as an identifier code at the end (or beginning) of each transmitted message. This preselected code may consist of a combination of ones and zeros which are distinct from any of the codes produced by the binary code switches 10-16. Illustratively, pattern generator 20 may produce twelve bits of information in the form of two six-bit series, each of five logical ones followed by a logical zero. This pattern may be produced by a generator (20) comprised of twelve output lines having the sixth and twelfth lines coupled to ground (logical zero) and the remaining ten lines coupled to a source of voltage. The level of this latter source of voltage is representative of a logical one.

Sequential encoder 18 is receptive to signals from clock 24 (see FIGURE 3a) and also to codes produced by switches 16-10 and pattern generator 20. Encoder 18 may be comprised of one or more parallel to serial shift registers having a total of at least 32 parallel input lines and stages. The sixteen output lines of switches 16-10 (four lines from each switch) and twelve output lines from generator 20 are respectively coupled to 28 of the 32 register input lines. Illustratively, switch 16 is coupled to input lines 1-4, switch 14 to input lines 6-9, switch 12 to input lines 11-14, switch 10 to input lines 16-19 and generator 20 to input lines 21-32. By applying an appropriate signal to a parallel/serial input line (not shown) of encoder 18, signal information on the 32 parallel input lines are entered into the associated shift register stages. Clock signals from clock 24 cause signal information within the respective shift register stages to sequentially appear at an associated serial output terminal in the order in which they are respectively

positioned (least significant bit first). In other words, the data in register stage 1 appears at the associated serial output terminal first, while the data in stage 32 appears last. The 32 bit serial code may be repeated at the serial output terminal by re-entering the data on the 32 input lines into the associated register stages and applying clock signals. A typical sequentially encoded signal as provided at the output of encoder 18 is illustrated in FIGURE 3b.

With reference to FIGURE 3b, a combination of four, four-bit information commands (clock intervals 1-20) and a twelve-bit identifier pattern (clock intervals 21-32) are generated during the clock intervals of 1-32. The information commands produced by switches 16-10 are respectively illustrated in FIGURE 3b as a binary count of 0001 (decimal 1) beginning at clock interval 1, a binary count of 0011 (decimal 3) beginning at clock interval 6, a binary count of 0111 (decimal 7) beginning at clock interval 11 and a binary count of 1111 (decimal 15) beginning at clock interval 16. An identifier pattern beginning at clock interval 21 follows the information commands (message) and terminates at clock interval 32. An encoder 22 receives the signals provided by the sequential encoder 18 and changes the format of these signals to a form in which both the sequential data signals and the signals from clock 24 may be decoded. A detailed schematic of encoder 22 is illustrated in FIGURE 4.

With reference to FIGURE 4, a JK flip-flop 40 receives data input signals through an inverter 44 to a K input and direct coupled to a J input. An exclusive OR gate 42 has an input coupled to the Q output of flip-flop 40 and further receives inverted clock signals from an inverter 46. Application of data signals such as those illustrated in FIGURE 3b to the data-in terminal and application of the clock signals of FIGURE 3a to the clock-in terminal of this apparatus cause flip-flop 40 to produce the waveform of FIGURE 3c at the associated Q output terminal. An encoded output signal which is bi-phase level coded, as illustrated in FIGURE 3d, is thereafter produced by applying output signals from flip-flop 40 and inverted clock signals from inverter 46 to inputs on exclusive OR gate 42. Modification of the data signals to the bi-phase level coded form shown in FIGURE 3d is desirable in order to facilitate reproduction of the transmitter clock signals in the remote control receiver. A detailed explanation of how the clock signals are recovered from the transmitted signal information is given later with reference to FIGURE 5. For general information on bi-phase level en-

coding, please see the article by Fogarty in Digital Design, June 1975, pages 24-26.

Encoded signals provided at the output of encoder 22 are coupled to frequency shift oscillator 26. Oscillator 26 provides one of two output frequencies in response to application of a logical one or zero at the input terminal. Illustratively, oscillator 26 may provide an output frequency of 37 KHz in response to application of a logical one and 36 KHz in response to application of a logical zero. An output amplifier 28 receives the signals provided by oscillator 26 and provides these signals at a relatively high amplitude to an ultrasonic transducer 30. Transducer 30 may incorporate a piezoelectric element and have a relatively narrow bandwidth and high gain.

Signal transmission from the apparatus of FIGURE 1 is initiated by presetting switches 10-16 to desired positions which the television receiver functions are ultimately to assume and depressing transmit switch 34. When switch 34 is closed, current from battery 32 is coupled to the electrical circuits of the remote control transmitter effecting signal transmission. Once switch 34 is closed, a continuous repetition of message and pattern is transmitted. Subsequent readjustment of switches 10-16 may be made while switch 34 is closed allowing the operator to manipulate the remote control adjustments in substantially the same manner in which the respective counterparts are adjusted at the television receiver.

A remote control receiver suitable for receiving and decoding the signals provided by the transmitter of FIGURE 1 is illustrated in FIGURE 2. This remote control receiver responds to the transmitted binary coded instruction signal which is a pulse arrangement in sequential array representative of the ultimate operating position which the television receiver functions such as color, volume and brightness coupled to the output of the remote control receiver are to assume. With reference to FIGURE 2, an ultrasonic receiving transducer 50 is coupled to a signal decoder 52 which serves to separate the received combined clock and data signals. Clock and data signals provided by decoder 52 are coupled to a first shift register 54. A second shift register 56 receives signals from the first shift register and couples these signals to a third shift register 58. A sequencing generator 60 provides clock signals to the first, second and third shift registers in response to an enabling signal from a pattern decoder 62. A comparator 64 serially compares signals provided at the outputs of registers 56 and 58 and couples a comparison signal to a

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data register 66. Data register 66 receives input signals from shift register 54.

In the operation of the above-described system, signals provided by the transmitter 5 of FIGURE 1 are received by receiving transducer 50. Transducer 50 may be a piezoelectric type having similar characteristics to the one utilized with the transmitter apparatus of FIGURE 1. Signals received by transducer 50 are coupled to decoder 52. Decoder 52 includes frequency detecting apparatus which comprises, for example, a phase-locked loop suitable for phase locking to the transmitted signals and providing bilevel output signals in response to the two different transmitted frequencies. Decoder 52 may further include circuitry for converting the code produced, for example, at the output of encoder 22 of FIGURE 1 (see FIGURE 3d) to the coded sequence provided at the output of sequential encoder 18 (see FIGURE 3b). A decoder circuit suitable for use in decoder 52 is illustrated in schematic form in FIGURE 5.

The apparatus in FIGURE 5 includes a pulse forming circuit comprised of exclusive OR gates 70 and 72. Pulses provided at the output of OR gate 72 are coupled to a monostable multivibrator 74. Signals provided at the output of multivibrator 74 are coupled to a clock input of a D flip-flop 76 and to a second monostable multivibrator 78. Flip-flop 76 further receives data input signals directly at a D input terminal. An AND gate 80 combines signals from flip-flop 76 and multivibrator 78 to produce a desired output signal. The operation of the circuitry in FIGURE 5 can best be shown by way of example.

Illustratively, the signal of FIGURE 3d is received by the apparatus of FIGURE 2 and applied to the inputs of a pulse forming circuit comprised of exclusive OR gates 70 and 72. A pulse train, as shown in FIGURE 3e is produced at the output of gate 72 and this pulse train is utilized to trigger monostable multivibrator 74. Multivibrator 74 has a time constant of t_1 that is adjusted to be greater than one-half and less than one clock interval of the clock in the remote control transmitter (see FIGURE 3a). Signals provided at the Q and $\bar{Q}$ outputs of multivibrator 74 are respectively illustrated in FIGURES 3f and 3g. Inverted signals provided at the $\bar{Q}$ terminal of multivibrator 74 clock the input data to D type flip-flop 76. With the data signals of FIGURE 3d applied to the D input and the signals of FIGURE 3g applied at the clock input (CP), flip-flop 76 respectively produces the waveforms of FIGURES 3h and 3i at the associated Q

and $\bar{Q}$ output terminals.

To facilitate signal decoding, the clock waveform of FIGURE 3a is reproduced in the decoder by supplying one output (FIGURE 3g, $\bar{Q}$) of multivibrator 74 to multivibrator 78. Monostable multivibrator 78 is adjusted to provide a pulse output having a duration t_2 equal to approximately one-half the period of the clock signals illustrated in FIGURE 3a. The output signals of multivibrator 78 are shown in FIGURE 3j. It will be appreciated that the waveforms shown in FIGURE 3j are substantially the same as the clock waveforms illustrated in FIGURE 3a. In order to recover the signal information transmitted by the remote control transmitter, the inverted output signals of flip-flop 76 are combined with the regenerated clock signals from multivibrator 78 in an AND gate 80. The output signals from gate 80 (illustrated in FIGURE 3k) are the same signals as those produced by the sequential encoder 18 of FIGURE 1.

Although an AND gate (80) is illustrated as the combining means of signals from multivibrator 78 and flip-flop 76, combination of these respective signals may be accomplished by, for example, clocking (with multivibrator 78) the $\bar{Q}$ signal of flip-flop 76 directly into an appropriate shift register (e.g., register 54).

Data signals provided by decoder 52 (see FIGURE 3k) are clocked into register 54 (see FIGURE 2) by the clock signal illustrated in FIGURE 3j. When the last 12 bits of signal information shifted into register 54 correspond to a predetermined code, (see pattern of FIGURE 3b, bits 21-32) pattern decoder 62, which is arranged specifically to sense this code, becomes energized enabling sequence generator 60. Sequence generator 60 remains enabled for a one-half clock pulse interval of the transmitted clock signal (see t_2 of FIGURE 3j) and provides, during this interval, both mode and high frequency clock signals to shift registers 54-58 and comparator 64. The high frequency clock signals produced by generator 60 during the t_2 interval are provided in four uninterrupted sub-sequences of 32 pulses each. A 128 pulse sequence is utilized for providing the necessary amount of steps to compare the received signal (message and pattern) with a previously received signal and decide whether or not to enter this signal in an associated output register. In the first sub-sequence (the first 32 pulse interval), generator 60 provides both high frequency clock signals and mode signals to registers 54-58 and only mode signals to comparator 64. Mode signals applied to each register control the coupling of the re-

spective input terminals to either an output terminal of the same register or the preceding stage. When a register input and a register output terminal are coupled together, signal information shifted to the output terminal of this register is reapplied to the input of the register causing the stored signal information to recirculate. Mode signals are applied to comparator 64 to inhibit operation of this comparator except during the second sub-sequence.

Clock and mode signals applied in the first sub-sequence to the respective registers cause register 54 to recirculate the signal information stored within; register 56 to receive information provided at the output terminal of register 54; and register 58 to recirculate the information within. At the end of the first sub-sequence registers 54 and 56 contain the same signal information. Register 58 contains the same signal information as it contained just prior to the first sub-sequence. In the second sub-sequence interval, data in shift register 54 is again recirculated, data in shift register 56 is recirculated and data in shift register 58 is recirculated. Concurrently with the recirculation of data in registers 56 and 58, an appropriate mode signal is applied to comparator 64. Comparator 64 provides a bit by bit comparison of each of the bits of data in registers 56 and 58 including the pattern portion of the signal information. If the data in registers 56 and 58 are identical, a preselect circuit in comparator 64 is set in a first condition.

In the third sub-sequence, data in respective shift registers 54 and 56 are recirculated. Concurrently, the data in register 56 is transferred to shift register 58. At the end of the third sub-sequence, registers 54-58 contain the same data contents. The transfer of data from register 56 to register 58 is in preparation for comparison of a subsequent message and pattern to be received by this apparatus. After sequence generator 60 reaches a count of 96 (the beginning of the fourth sub-sequence), an enable signal from this generator is provided to comparator 64. If the preselect circuitry in comparator 64 is set in a first condition, the enable signal causes comparator 64 to provide a latch signal to register 66. This latch signal remains on for the entire fourth sub-sequence (last 32 bits) allowing signal information in shift register 54 to be transferred in parallel to register 66. If, however, the preselect condition in comparator 64 is in a second condition indicating that the data in registers 56 and 58 are not the same, then no data is transferred to register 66 and the original data therein remains unchanged. Signal information in register 66 represents data which has been

verified as being identical to a previous data transmission. Data in register 66 corresponds in sequence to the sixteen bits of information (four groups of four bits) transmitted by the apparatus of FIGURE 1. The sixteen bits of information correspond respectively to the binary data representative of channel number, color, volume and brightness. Control circuitry (not shown) is coupled to the sixteen data output lines (shown as four) of register 66 and responsively provides, in accordance with the numerical value of each four bit binary group, a desired amount of control over television receiver channel selection, color, volume and brightness.

Although this remote control system has been described as controlling four specific television functions, it will be appreciated that control of other remote functions may similarly be realized. It will further be appreciated by one skilled in the art that the number of remote control functions may be increased or decreased as can the number of bits used to control each function without changing the basic operation of the apparatus.

WHAT WE CLAIM IS:—

1. A remote control system for a television receiver which provides substantially simultaneous control of a plurality of television receiver functions in response to coded instruction signals from a remote location, comprising a remote control transmitter, each of a corresponding plurality of remote controls of the remote control transmitter being capable of being set to any of a plurality of operating conditions, the remote control transmitter being responsive to said remote controls to produce bi-phase coded instruction signals; and wherein a remote control receiver is responsive to said bi-phase coded instruction signals from said remote control transmitter which are binary coded control function signals representative of desired operating conditions of said television receiver functions to be controlled.

2. A remote control system according to Claim 1, in which said bi-phase coded instruction signals include binary remote control instruction signals representative of the operating conditions of said plurality of remote controls and said remote control transmitter including a source of clock signals, encoding means for serially encoding said binary remote control instruction signal in accordance with signals from said source of clock signals, rearranging means for rearranging said serially encoded binary remote control instruction signal in a bi-phase format to include information relating to said clock signal, and means for transmitting said biphasic encoded instruction signal.



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spective input terminals to either an output terminal of the same register or the preceding stage. When a register input and a register output terminal are coupled together, signal information shifted to the output terminal of this register is reapplied to the input of the register causing the stored signal information to recirculate. Mode signals are applied to comparator 64 to inhibit operation of this comparator except during the second sub-sequence.

Clock and mode signals applied in the first sub-sequence to the respective registers cause register 54 to recirculate the signal information stored within; register 56 to receive information provided at the output terminal of register 54; and register 58 to recirculate the information within. At the end of the first sub-sequence registers 54 and 56 contain the same signal information. Register 58 contains the same signal information as it contained just prior to the first sub-sequence. In the second sub-sequence interval, data in shift register 54 is again recirculated, data in shift register 56 is recirculated and data in shift register 58 is recirculated. Concurrently with the recirculation of data in registers 56 and 58, an appropriate mode signal is applied to comparator 64. Comparator 64 provides a bit by bit comparison of each of the bits of data in registers 56 and 58 including the pattern portion of the signal information. If the data in registers 56 and 58 are identical, a preselect circuit in comparator 64 is set in a first condition.

In the third sub-sequence, data in respective shift registers 54 and 56 are recirculated. Concurrently, the data in register 56 is transferred to shift register 58. At the end of the third sub-sequence, registers 54-58 contain the same data contents. The transfer of data from register 56 to register 58 is in preparation for comparison of a subsequent message and pattern to be received by this apparatus. After sequence generator 60 reaches a count of 96 (the beginning of the fourth sub-sequence), an enable signal from this generator is provided to comparator 64. If the preselect circuitry in comparator 64 is set in a first condition, the enable signal causes comparator 64 to provide a latch signal to register 66. This latch signal remains on for the entire fourth sub-sequence (last 32 bits) allowing signal information in shift register 54 to be transferred in parallel to register 66. If, however, the preselect condition in comparator 64 is in a second condition indicating that the data in registers 56 and 58 are not the same, then no data is transferred to register 66 and the original data therein remains unchanged. Signal information in register 66 represents data which has been

verified as being identical to a previous data transmission. Data in register 66 corresponds in sequence to the sixteen bits of information (four groups of four bits) transmitted by the apparatus of FIGURE 1. The sixteen bits of information correspond respectively to the binary data representative of channel number, color, volume and brightness. Control circuitry (not shown) is coupled to the sixteen data output lines (shown as four) of register 66 and responsively provides, in accordance with the numerical value of each four bit binary group, a desired amount of control over television receiver channel selection, color, volume and brightness.

Although this remote control system has been described as controlling four specific television functions, it will be appreciated that control of other remote functions may similarly be realized. It will further be appreciated by one skilled in the art that the number of remote control functions may be increased or decreased as can the number of bits used to control each function without changing the basic operation of the apparatus.

WHAT WE CLAIM IS:—

1. A remote control system for a television receiver which provides substantially simultaneous control of a plurality of television receiver functions in response to coded instruction signals from a remote location, comprising a remote control transmitter, each of a corresponding plurality of remote controls of the remote control transmitter being capable of being set to any of a plurality of operating conditions, the remote control transmitter being responsive to said remote controls to produce bi-phase coded instruction signals; and wherein a remote control receiver is responsive to said bi-phase coded instruction signals from said remote control transmitter which are binary coded control function signals representative of desired operating conditions of said television receiver functions to be controlled.

2. A remote control system according to Claim 1, in which said bi-phase coded instruction signals include binary remote control instruction signals representative of the operating conditions of said plurality of remote controls and said remote control transmitter including a source of clock signals, encoding means for serially encoding said binary remote control instruction signal in accordance with signals from said source of clock signals, rearranging means for rearranging said serially encoded binary remote control instruction signal in a bi-phase format to include information relating to said clock signal, and means for transmitting said biphasic encoded instruction signal.



3. A remote control system according to Claim 2 in which said encoding means includes a pattern generator for producing a predetermined array of binary identification signals, sequencing means for providing repetitive sequences in predetermined order of said binary identification signals produced by said pattern generator and said at least one binary remote control instruction signal in accordance with signals from said clock signal source, and said means for transmitting said bi-phase coded instruction signal includes a frequency-shift oscillator and a transducer.
4. A remote control system according to Claim 2 or 3 in which each of said remote controls comprises a binary code switch having an output line for providing in parallel array a binary code instruction signal representative of the operating condition of said remote control.
5. A remote control system according to Claim 3 or 4 in which said sequencing means comprises a parallel-to-serial shift register having a plurality of inputs receptive to binary code signals, and said pattern generator comprises a plurality of wired logical ones and zeroes arranged in a sequence distinct from said binary code instruction signals provided by said remote controls; and coupling means couple said instruction signals from said remote controls and said pattern generator to said shift register inputs; and said source of clock signals is coupled to said shift register for producing serially encoded data output from said serial shift register.
6. A remote control system according to Claims 2, 3 or 5 in which said rearranging means comprises a bistable multivibrator responsive to said clock and serially encoded binary remote control instruction signals; an inverter for inverting said clock signals; and an exclusive OR gate coupled to the output of said multivibrator and to the output of said inverter for providing bi-phase level coded instruction signals.
7. A remote control system according to Claim 3 or 5 in which said frequency shift oscillator provides output signals at first and second frequencies in response to logical ones and zeros of said bi-phase coded instruction signals.
8. A remote control receiver for use in a remote control system, for receiving coded instruction signals which comprise remote control binary instruction signals together with a predetermined verification pattern, and clock pulse decoding information in the form of serially encoded bi-phase level binary instruction signals; said remote control receiver comprising: receiving means for receiving said coded instruction signals; decoding means for extracting said remote control binary instruction signal from said serially encoded bi-phase level binary instruction signals; authenticating means coupled to said decoding means for comparing each remote control binary instruction signal with the previous instruction signal and providing a parallel binary representation of the compared remote control binary instruction signal and a latch signal; and control means responsive to said parallel binary remote control instruction and latch signals for actuating remotely controllable signal receiver functions.
9. A remote control receiver in accordance with Claim 8 in which said decoding means comprises: impulse generating means coupled to said receiving means for generating impulses in response to logic level transitions in said serially encoded bi-phase level binary instruction signal produced by said receiving means; first pulse generating means coupled to said impulse generating means for generating pulses having a duration of more than one-half and less than the entire duration of one clock interval of said clock pulse decoding information; second pulse generating means coupled to said first pulse generating means for providing reconstituted clock pulses having a duration substantially equal to one clock interval of said clock pulse decoding information; third generating means having inputs receptive to signals from said first pulse generating means and from said receiving means for generating further signals; and combining means for combining said reconstituted clock pulses from said second pulse generating means and said further signals from said third generating means and generating therefrom sequential binary instruction signals.
10. A remote control receiver in accordance with Claims 8 or 9 in which said authenticating means comprises first register means coupled to said decoding means and receiving therefrom reconstituted clock signals and binary instruction signals; identification means responsive to the presence of a said predetermined verification pattern of said binary instruction signal in said first register and producing an enabling signal in response thereto; sequence generating means responsive to said enabling signal and producing in response thereto a high-frequency signal; second register means coupled to said first register means for storing the output of said first register means in response to said high-frequency signal; third register means coupled to said second register means and responsive to said high-frequency signal to produce a memory signal representative of the binary

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instruction signal previously occupying said second register and to store the binary instruction signal occupying said second register means for subsequent use as a
5 memory signal; comparator means coupled to said second and third register means and responsive to said high-frequency signal to compare said binary instruction signals in said second register means with the
10 memory signal in said third register and producing said latch signal when said memory signal and said binary instruction signal are identical.

11. A remote control receiver in
15 accordance with Claim 10 in which said control means comprises data register means coupled to said first register means and to said latch signal to accept said parallel binary instruction signal in said
20 first register means as verified and to make it available as a parallel binary instruction signal.

12. A remote control receiver in
25 accordance with Claim 9 in which said receiving means comprises a transducer for converting transmitted signals into elec-

trical signals; said impulse generating means comprises a first exclusive OR gate coupled to the output of said transducer and a second exclusive OR gate coupled to
30 the output of said transducer and to the output of said first exclusive OR gate; said first and second pulse generating means comprise monostable multivibrators and said third generating means comprises a D
35 type flip-flop; and said combining means comprises an AND gate.

13. A remote control receiver according to any one of Claims 8-12, and substantially as described with reference to
40 Figure 2 or Figures 2 and 5.

14. A remote control system according to any one of Claims 1-7, and including a remote control transmitter substantially as described with reference to Figure 1 or
45 Figures 1 and 4.

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