DIGITALLY-CONTROLLED WIDE RANGE A.G.C.

The present invention relates to automatic gain control circuits which are suitable for use in digital communication systems.

In communications equipment required to operate with a wide range of input signal level, a wide range automatic gain control (a.g.c.) is often incorporated. To permit the rapid resumption of normal operation following a break in transmission, such as would be required when using a data modem operating in a turn-around mode, it would be desirable to be able to preserve the gain value during the break for an indefinite period, which implies the use of digital storage. Digitally-controlled stepped attenuators are well known in the art, but an attenuator of this type designed to provide a wide dynamic range, say of 60dB, with a small incremental step size, say of 0.2dB, would be very complex and expensive.

According to the invention there is provided an automatic gain control circuit for use in a data transmission system, the circuit comprising an amplifier of fixed gain fed by an attenuator comprising a fixed resistive device and an active device whose conductance is varied by a control voltage generator responsive to the amplifier output envelope voltage, the control voltage generator including a digital-to-analog converter which is controlled by a digital counter capable of counting up or down, the counter being controlled by a window comparator arranged to compare the rectified output voltage of

the fixed gain amplifier with upper and lower reference voltage limits, the arrangement being such that when the amplifier voltage deviates beyond either limit, the counter is enabled and the appropriate up or down indication is given causing the counter to be driven from a source of clock pulses to change the conductance of the active device characterised in that means are provided for inhibiting the application of the clock pulses to the counter to freeze the gain of the automatic gain control circuit in the event of a break in transmission until the transmission is restored to normal.

The present invention comprises the digital control of an analogue gain control element which provides the required functions with low complexity and cost.

In order that the invention may be more readily understood, reference is made to the following figures.

Fig. 1 shows a well-known a.g.c. amplifier arrangement (Prior art).

Fig. 2 shows an embodiment of the invention.

The basic prior art a.g.c. amplifier arrangement is shown in Fig. 1 and comprises a fixed high gain amplifier G in tandem with an L-pad attenuator formed by the series resistor R and the transistor T. The conductance of the collector-emitter path of the transistor is a function of the voltage applied to the base, which is derived from the envelope of the amplifier output voltage. By suitable choice of resistor R in association with the choice of

the transistor, an operating range of at least 60dB can be obtained before the transistor departs from linear bidirectional resistive behaviour.

It can be shown, and has been confirmed experimentally, that the conductance of the bipolar transistor when operated in this mode is a logarithmic function of the base voltage over a wide range, and hence that the gain of the arrangement of Fig. 1 is an inverse logarithmic function of the voltage applied to the base of the transistor.

This behaviour forms the basis for the invention, one possible implementation of which is shown in Fig. 2. The voltage applied to the base of the transistor T is produced by a digital-to-analog converter D/AC which is controlled by a digital-up-down counter COUNT.

The counter is controlled by a window comparator WC which compares the rectified output voltage of the amplifier G with a reference voltage level V ref with upper and lower limits. If the output voltage exceeds either limit, the comparator produces counter enable conditions on the appropriate up or down indication lead UEN or DEN in Fig. 2. The counter is then clocked to change the drive to the digital-to-analogue converter D/AC which thereby changes the conductance of the transistor T to increase or decrease the amplifier gain as required. A fixed voltage Vo is added to the control voltage to set the operating range of the digital control within the linear range of operation of the transistor.

This offset voltage Vo will preferably include a temperature dependent component to compensate for temperature variations in the control transistor operation.

The time constant of the a.g.c. response is determined both by the time constant of the smoothing associated with the rectifier RECT, which can be adjusted to suit the waveform of the signal, and by the frequency of the clock controlling the counter C. For example, a high frequency clock can be used initially for rapid acquisition of the signal followed by a low frequency clock to minimise the response of the a.g.c. to message-dependent amplitude variations. In the event of a break in transmission, the clock can be inhibited by lead IL operating on gate GC, when the gain of the a.g.c. will be frozen until the signal is restored and lead IL restored to normal.

CLAIMS

1. An automatic gain control circuit for use in a data transmission system, the circuit comprising an amplifier of fixed gain fed by an attenuator comprising a fixed resistive device and an active device whose conductance is varied by a control voltage generator responsive to the amplifer output envelope voltage, the control voltage generator including a digital-to-analogue converter which is controlled by a digital counter capable of counting up or down, the counter being controlled by a window comparator arranged to compare the rectified output voltage of the fixed gain amplifier with upper and lower reference voltage limits, the arrangement being such that when the amplifier voltage deviates beyond either limit, the counter is enabled and the appropriate up or down indication is given causing the counter to be driven from a source of clock pulses to change the conductance of the active device characterised in that means are provided for inhibiting the application of clock pulses to the counter to freeze the gain of the automatic gain control circuit in the event of a break in transmission until the transmission is restored to normal.

2. An automatic gain control circuit according to claim 1 in which the inhibiting means comprises an AND gate to which the source of clock pulses are applied together with a signal which closes the gate when the means responds to a break in transmission.

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3. An automatic gain control circuit according to claim 2 in which a fixed voltage level is added to the control voltage to compensate for temperature variations in the active device operation.

4. An automatic gain control circuit according to any one of the preceding claims in which the active device is a transistor and the control voltage is applied to the base of the transistor.

5. An automatic gain control circuit substantially as described with reference to Fig. 2 of the accompanying drawings.

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