

Abstract of the DisclosureA REDUCED COMPLEXITY EPR4 POST-PROCESSOR FOR SAMPLED
DATA DETECTION

An EPR4 detector comprises a PR4 Viterbi detector and an EPR4 post-processor for improving estimated output sequence at an output of the PR4 Viterbi. The PR4 Viterbi detector produces digital estimates of coded digital information values into the channel in accordance with a path through a PR4 trellis and produces other path information relating to other paths through the PR4 trellis. The EPR4 post-processor has a PR4 path storage circuit for receiving and storing the estimated sequence of coded digital information values which corresponds to a PR4 path through a sequence of states of an EPR4 trellis; an error-event selection circuit for receiving the other path information from the PR4 Viterbi detector for generating non-overlapping error-events from a set of error-events deviating from the PR4 path through the EPR4 trellis stored in the PR4 path storage circuit, and a path correction circuit connected to the PR4 path storage circuit and to the error-event selection circuit for correcting non-overlapping error-events deviating from the PR4 path through the EPR4 trellis, and for putting out a corrected estimated sequence of coded digital information values. An EPR4 detection method is also disclosed.

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