ABSTRACT

BETTER COPPER CMP PROCESS UTILIZING DUMMY PLUGS IN DAMASCENE PROCESS

A method of fabricating a semiconductor wafer having at least one integrated circuit, the method comprising the following steps. A semiconductor wafer structure having at least an upper and a lower dielectric layer is provided. The semiconductor wafer structure having a bonding pad area and an interconnect area. At least one active interconnect having a first width is formed in the interconnect area, through the dielectric layers. A plurality of adjacent dummy plugs each having a second width is formed in the bonding pad area, through a portion of the dielectric layers. The semiconductor wafer structure is patterned and etched to form trenches through the upper dielectric layer. The trenches surround each of the at least one active interconnect and the dummy plugs whereby the upper dielectric level between the adjacent dummy plugs is removed. A metallization layer is deposited over the lower dielectric layer, filling the trenches at least to the upper surface of the remaining upper dielectric layer. The metallization layer is planarized to remove the excess of the metallization layer forming a continuous bonding pad within the bonding pad area and including the plurality of adjacent dummy plugs, thus forming at least one damascene structure including the at least one respective active interconnect.

Figure 1