

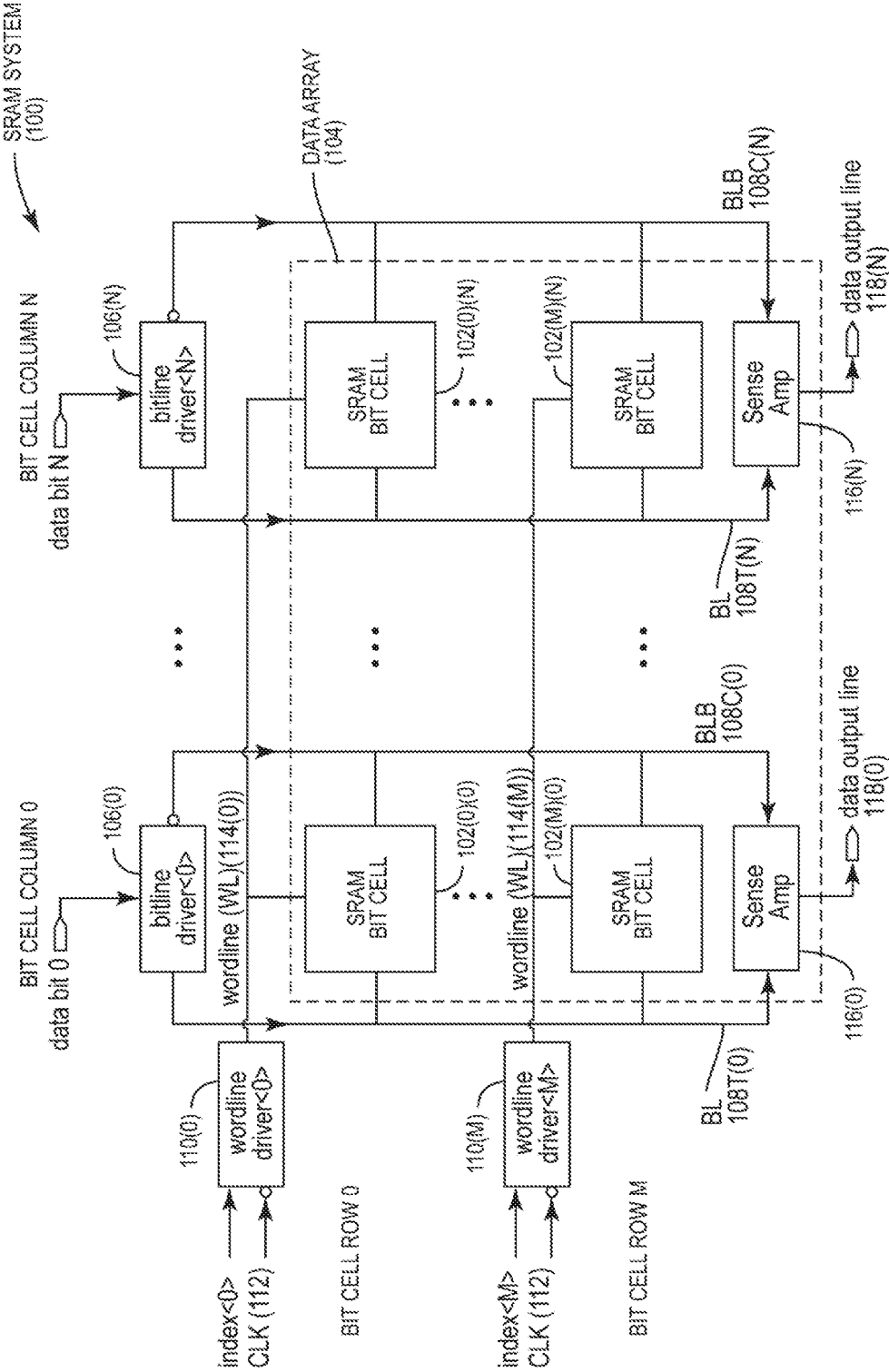
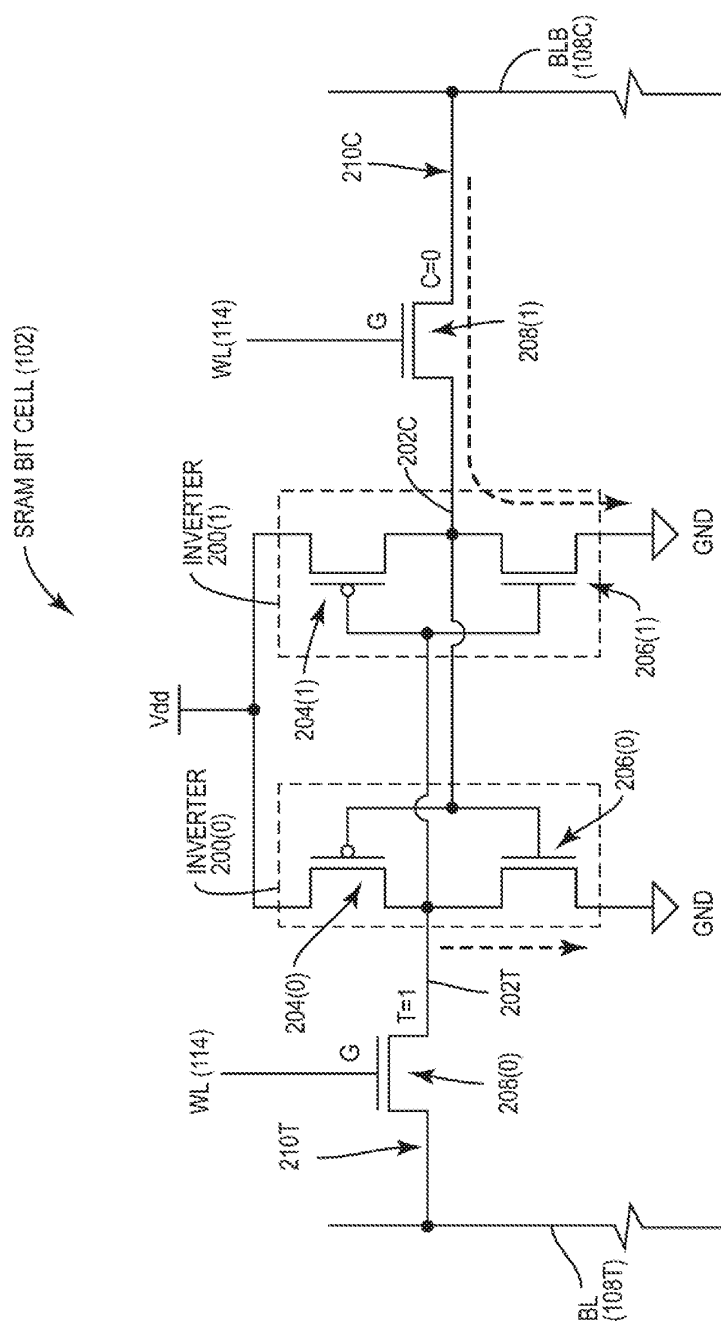
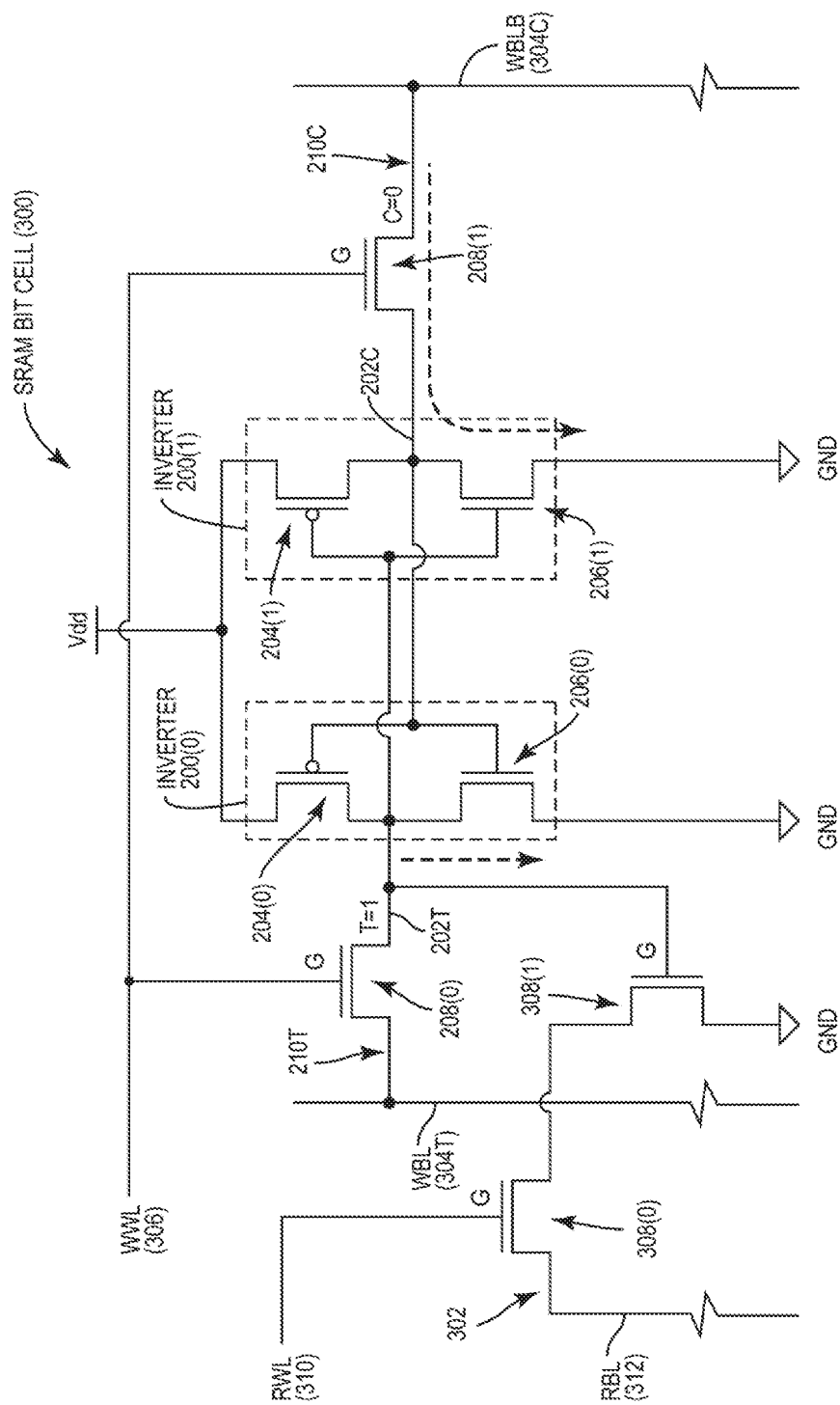


FIG. 1



202



391

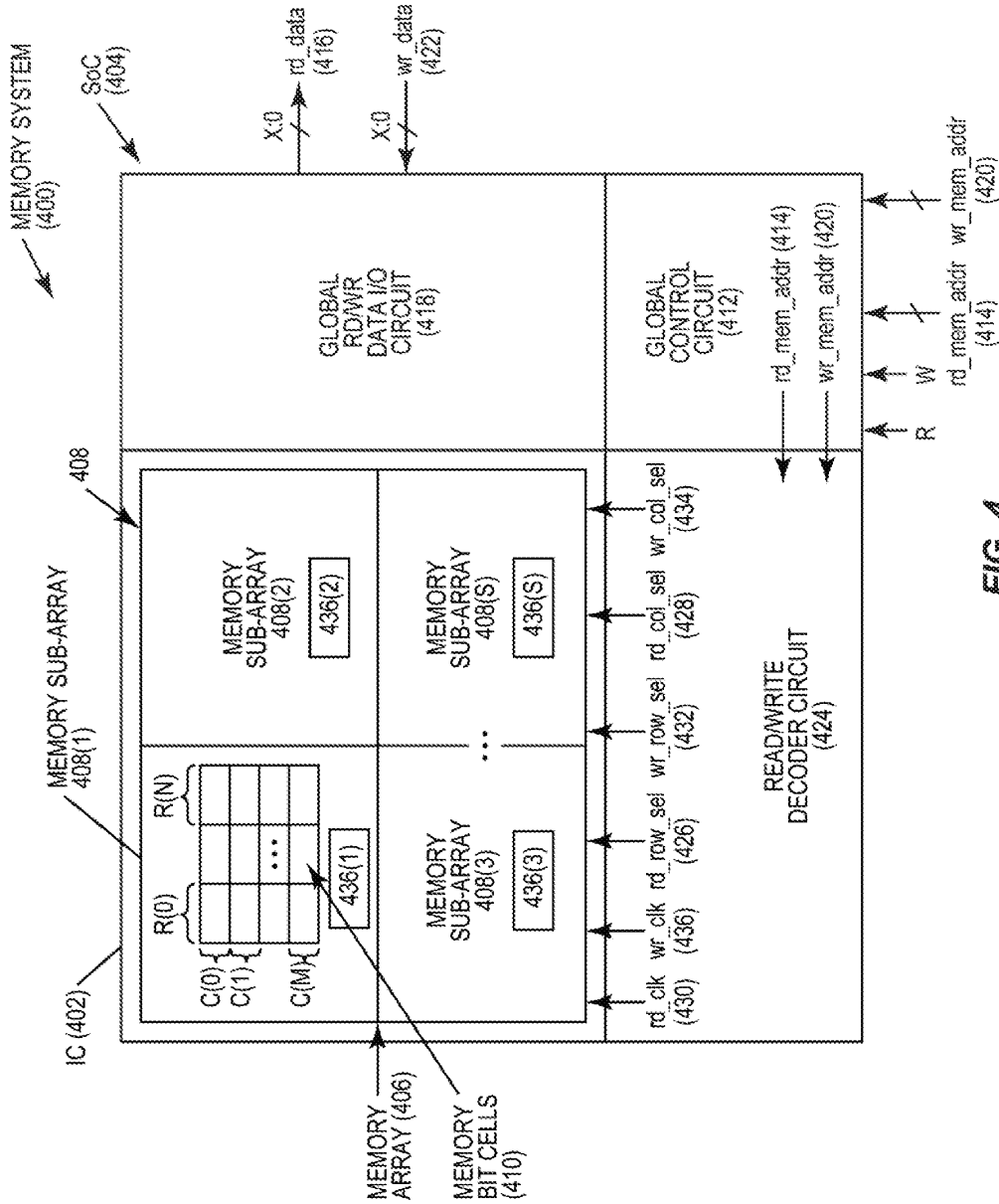


FIG. 4

5/9

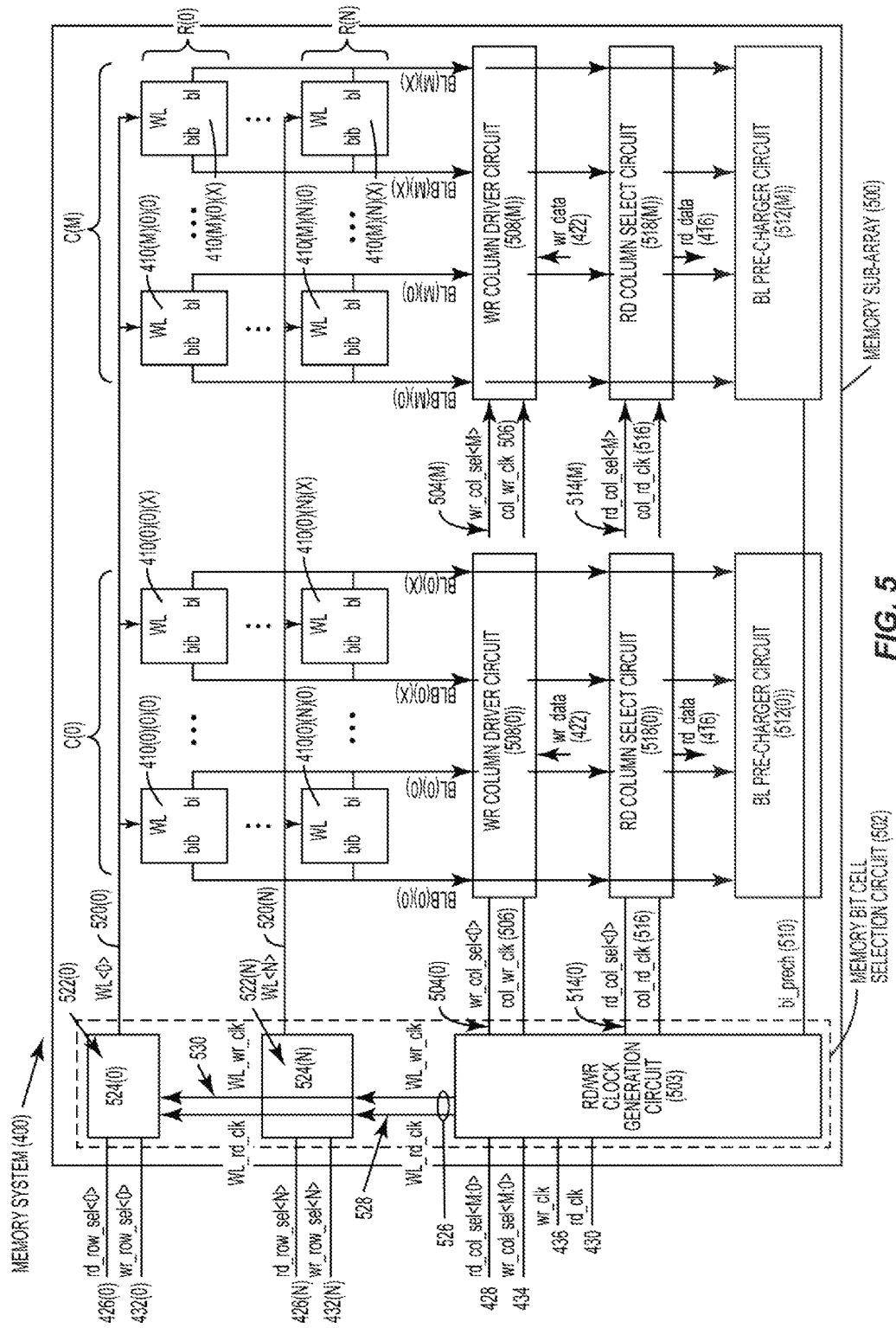


FIG. 5

600 ↗

ADDRESS CONDITION (602)	rd_row_sel (426) match wr_row_sel (432)	rd_row_sel (426) mismatch wr_row_sel (432)
rd_col_sel (428) match wr_col_sel (434)	WRITE SUCCESS AND TO READ BYPASS	WRITE SUCCESS AND READ FAIL
rd_col_sel (428) mismatch wr_col_sel (434)	BOTH READ/WRITE SUCCESS	WRITE SUCCESS AND READ FAIL

FIG. 6

7/9

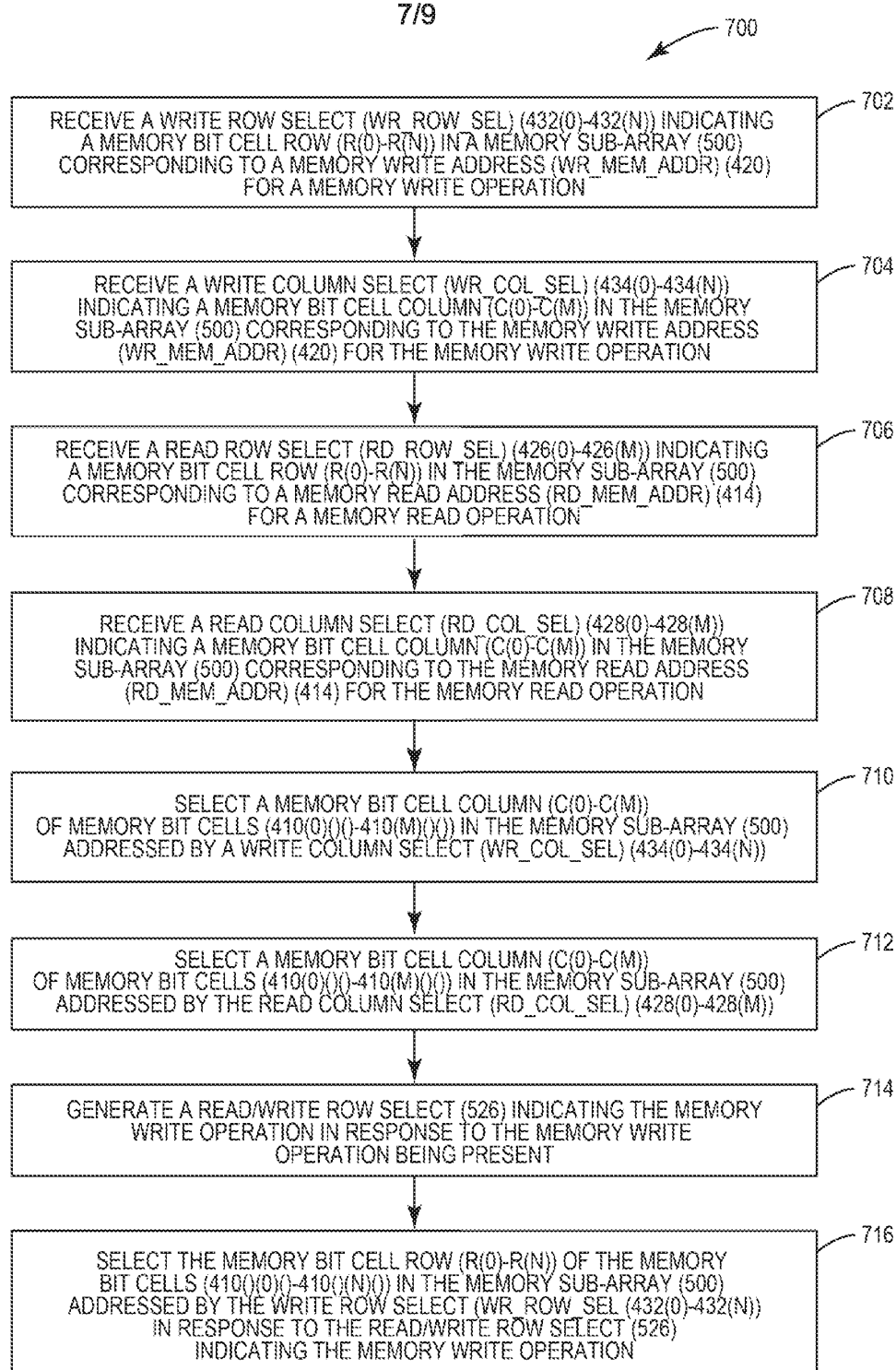


FIG. 7

CLOCK TIMING CONTROL
CIRCUIT (800)

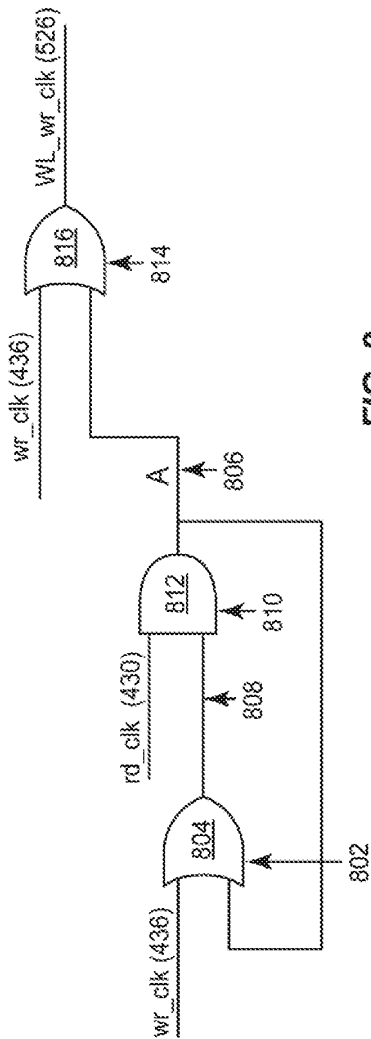


FIG. 8

900

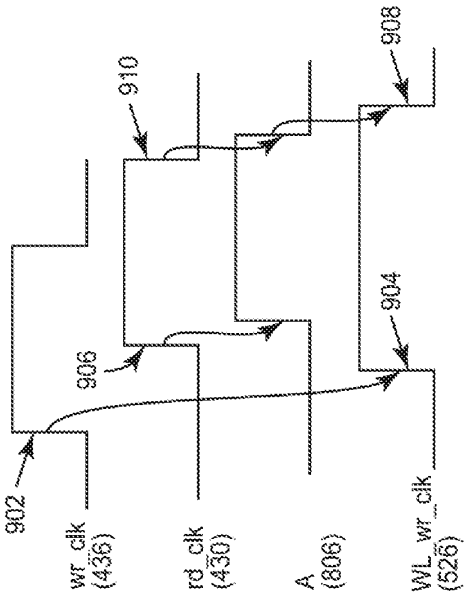


FIG. 9

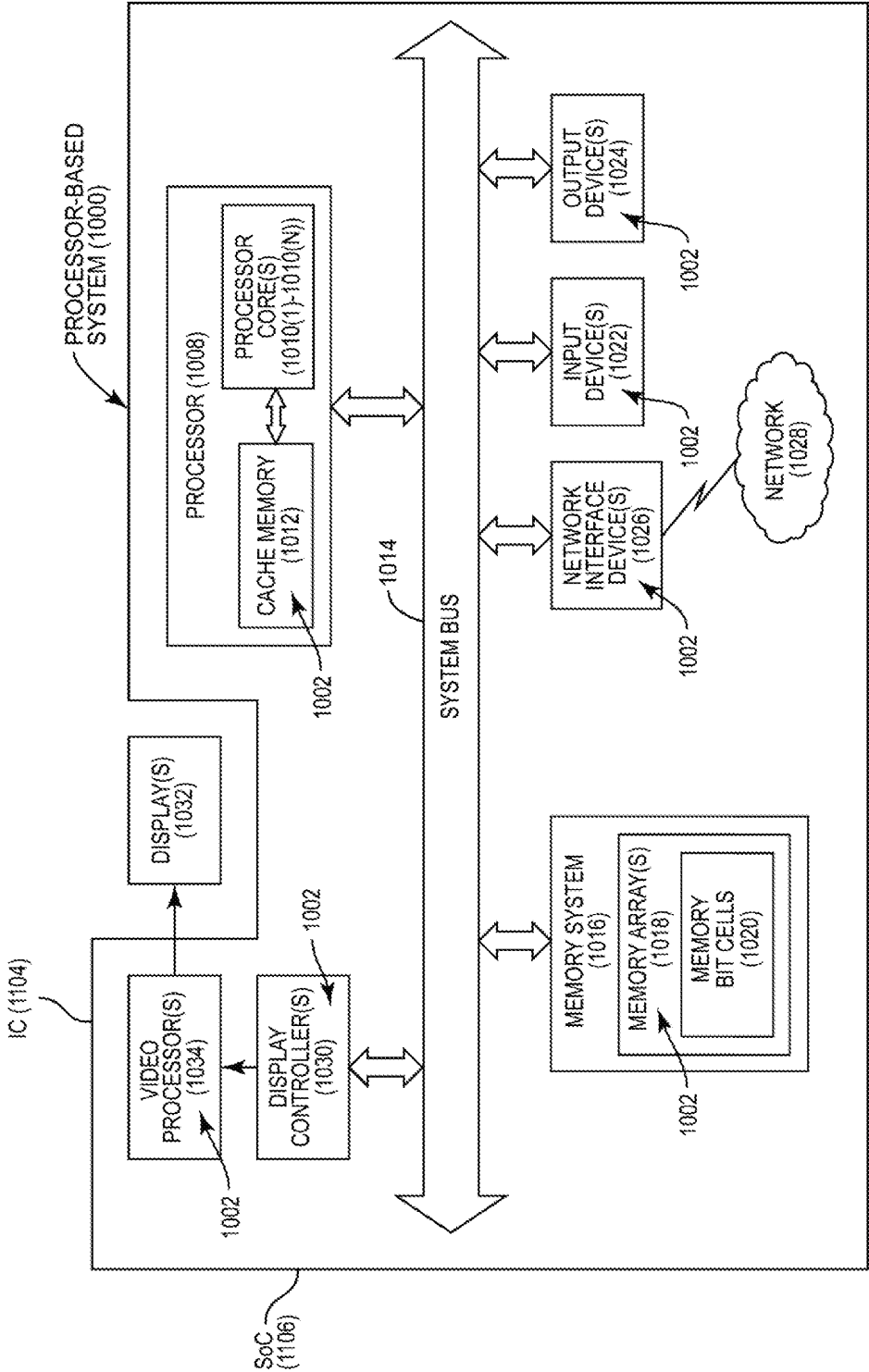


FIG. 10