

Abstract

FIELD PROGRAMMABLE MEMORY ARRAY

A field programmable memory array having a plurality of sub-arrays is provided. Programmable address decoders, programmable hierarchical bit line arrangements, programmable I/O arrangements, among other features, are provided to enable programming of portions of the array into selected modes. The modes may include wide memory, deep memory, FIFO, LIFO, among others. An embodiment of the invention is disclosed wherein the field programmable memory array is integrated with the programmable resources of a field programmable gate array.

Fig. 1A