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NONPLANAR DEVICE WITH STRESS INCORPORATION LAYER AND METHOD OF FABRICATION

BACKGROUND OF THE INVENTION

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1. FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor integrated circuit manufacturing and more specifically to a non-planar transistor having stress incorporation layer.

2. DISCUSSION OF RELATED ART

[0002] In order to increase device performance, silicon on insulator (SOI) transistors have been proposed for the fabrication of modern integrated circuits. Figure 1 illustrates a standard fully depleted silicon on insulator (SOI) transistor 100. SOI transistor 100 includes a single crystalline silicon substrate 102 having an insulating layer 104, such as a buried oxide formed thereon. A single crystalline silicon body 106 is formed on the insulating layer 104. A gate dielectric layer 108 is formed on the single crystalline silicon body 106 and a gate electrode 110 formed on the gate dielectric 108. Source 112 and drain 114 regions are formed in the silicon body 106 along laterally opposite sides of gate electrode 110.

[0003] Fully depleted SOI have been proposed as a transistor structure to take advantage of ideal sub-threshold gradients for optimized on current/off current ratios. In order to achieve ideal subthreshold gradients with transistor 100, the thickness of the silicon body 106 must be about 1/3 the size of the gate length (Lg) of the transistor or Tsi = Lg/3. However, as gate lengths scale especially as they approach 30nm, the need for ever decreasing silicon film thickness (Tsi) makes this approach increasingly impractical. At 30 nanometer gate length, the

thickness required of the silicon body is thought to need to be less than 10 nanometers, and around 6 nanometer for a 20 nanometer gate length. The fabrication of thin silicon films with thicknesses of less than 10 nanometers, is considered to be extremely difficult. On one hand, obtaining wafer uniformity on the order of one nanometer is a difficult challenge. On the other hand, to be able to contact these thin films to form raised source/drain regions to decrease junction resistance, becomes almost impossible since the thin silicon layer in the source/drain regions becomes consumed during the gate etch and various cleans following the gate etch and spacer etch leaving insufficient silicon 106 for silicon to grow on.

[0004] A double gate (DG) device, such as shown in Figures 2A and 2B, have been proposed to alleviate the silicon thickness issue. The double gate (DG) device 200 includes a silicon body 202 formed on an insulating substrate 204. A gate dielectric 206 is formed on two sides of the silicon body 202 and a gate electrode 208 is formed adjacent to the gate dielectric 206 formed on the two sides of the silicon body 202. A sufficiently thick insulating layer 209, such as silicon nitride, electrically isolates the gate electrode 208 from the top of silicon body 202.

[0005] Double gate (DG) device 200 essentially has two gates, one on either side of the channel of the device. Because the double gate device 200 has a gate on each side of the channel, thickness (Tsi) of the silicon body can be double that of a single gate device and still obtain a fully depleted transistor operation. That is, with a double gate device 200 a fully depleted transistor can be formed where Tsi = (2xLg)/3. The most manufacturable form of the double gate (DG) device 200, however, requires that the body 202 patterning be done with photolithography that is 0.7 x smaller than that used to pattern the gate length (Lg) of the device. In order to obtain high density integrated circuits, it is generally desirable to have the most aggressive lithography occur with respect to the gate length (Lg) of the gate

electrode 208. Although, double gate structures double the thickness of the silicon film (since there now is a gate on either side of the channel) these structures, however, are hideously difficult to fabricate. For example, silicon body 202 requires a silicon body etch which can produce a silicon body 202 with an aspect ratio (height to width) of about 5:1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is an illustration of a cross-sectional view of a depleted substrate transitor.

[0007] Figures 2A and 2B illustrate a double gate depleted substrate transistor.

[0008] Figure 3A and 3B is an illustration of a tri-gate transistor having a stress incorporation film in accordance with the present invention.

[0009] Figure 4 is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

[0010] Figures 5A-5E illustrate methods of fabricating a tri-gate transistor with a stress incorporation film in accordance with embodiments of the present invention.

[0011] Figure 6 is a plot which illustrates body heights and body widths which can be used to obtain partially depleted and fully depleted tri-gate transistors having gate lengths (Lg) of 30 nm and 20 nm.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0012] The present invention is a novel tri-gate or non-planar transistor structure with a stress incorporating layer and its method of fabrication. In the following description numerous specific details are set forth in order to provide a thorough understanding in the present invention. In other instances, well-known semiconductor process and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

[0013] The present invention is novel non-planar or tri-gate transistor structure and its method of fabrication. The tri-gate transistor includes a stress film formed around the channel region of the device to provides a stress to the channel region to improve carrier mobility. Greater carrier mobility results in increased transistor drive current. In an embodiment of the present invention, the stress film is formed beneath the channel region so that it completely surrounds the channel. By completely surrounding the channel region with the stress film, the stress film provides stress to all sides of the channel, thereby providing stress over a large area and maximizing and improving device performance. The film stress properties, such a type of stress (i.e., compressive or tensile) and the amount of stress can be varied in order to optimize performance for different transistor types (e.g., PMOS and NMOS).

[0014] In an embodiment of the present invention, the tri-gate transistor is a semiconductor on insulator (SOI) transistor. The tri-gate transistor is ideal for use in fully depleted substrate transistor applications. The tri-gate transistor includes a thin semiconductor body formed on an substrate, the substrate can be an insulating substrate or a semiconductor substrate. A gate dielectric is formed on the top surface and the sidewalls of the semiconductor body. A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and is formed adjacent to the gate dielectric formed on the sidewalls of the

semiconductor body. Source and drain regions are formed in the semiconductor body on opposite sides of the gate electrode. Because the gate electrode and the gate dielectric surround the semiconductor body on three sides, the transistor essentially has three separate channels and gates. The gate "width" of a transistor is equal to the sum of each of the three sides of the semiconductor body. Larger "width" transistors can be formed by connecting several tri-gate transistors together.

[0015] Because there are three separate channels formed in the semiconductor body, the semiconductor body can be fully depleted when the transistor is turned "ON", thereby enabling the formation of a fully depleted transistor with gate lengths of less than 30 nanometers without requiring the use of ultra-thin semiconductor bodies or requiring photolithographic patterning of the semiconductor bodies to dimensions less than the gate length (Lg) of the device. That is, the structure of the tri-gate transistor of the present invention enables a fully depleted transistor to be fabricated where the thickness of the semiconductor body and width of the semiconductor body are equal to the gate length of the device. Because the novel tri-gate transistor of the present invention can be operated in a fully depleted manner, the device is characterized by ideal (i.e., very sharp) subthreshold slope and a reduced drain induced barrier lowering (DIBL) short channel effect of less than 100mV/V and ideally about 60 mV/V which results in a lower leakage current when the device is turned "OFF" resulting in lower power consumption.

[0016] An example of a tri-gate transistor 300 with stress incorporation film in accordance with an embodiment of present invention as illustrated in Figure 3A and 3B. (Figure 3B is a cross-sectional view of Figure 3A taken through the gate electrode 324 of one of the semiconductor bodies 308.) Tri-gate transistor 300 is formed on an substrate 302. In an embodiment of the present invention, substrate 302 is an insulating substrate which includes a lower monocrystalline

silicon substrate 304 upon which is formed in insulating layer 306, such as a silicon dioxide film. Tri-gate transistor 300, however, can be formed on any well-known insulating substrate such as substrates formed from silicon dioxide, nitrides, oxides, and shappires. In an embodiment of the present invention, the substrate 302 can be a semiconductor substrate, such as but not limited to monocrystalline silicon substrate and gallium arsenide substrate.

[0017] Tri-gate transistor 300 includes a semiconductor body 308 and typically a plurality of semiconductor bodies 308 formed on insulator 306 of insulating substrate 302. Semiconductor body 308 can be formed of any well-known semiconductor material in which carrier mobility can be enhanced by applying a stress to the semiconductor, such as but not limited to silicon (Si) and silicon germanium (Si_xGe_y) where the Ge content is less than about 25%. Three-five (III-V) semiconductors, such as gallium arsenide (GaAs), InSb, GaP, and GaSb may also benefit from applying a stress to them. It is thought that direct band gap materials may not benefit from applying a stress thereto, while non-direct band gaps will benefit. Semiconductor body 308 is formed of a material which can be reversibly altered from an insulating state to a conductive state by applying external electrical controls. Semiconductor body 308 is ideally a single crystalline film when the best electrical performance of transistor 300, is desired. For example, semiconductor body 308 is a single crystalline film when transistor 300 is used in high performance applications, such as in a high density circuit, such as a microprocessor. Semiconductor body 308, however, can be a polycrystalline film when transistor 300 is used in applications requiring less stringent performance, such as in liquid crystal displays. Insulator 306 insulates semiconductor body 308 from monocrystalline silicon substrate 302. In an embodiment of the present invention, semiconductor body 308 is a single crystalline silicon film. Each semiconductor body or bodies 308 has a pair of laterally opposite sidewalls 310 and 312 separated by a distance which defines a

semiconductor body width 314. Additionally, each semiconductor body 308 has a top surface 316 opposite a bottom surface 318 formed on substrate 302. The distance between the top surface 316 and the bottom surface 318 defines a body height 320. In an embodiment of the present invention the body height 320 is substantially equal to the body width 314. In an embodiment of the present invention, the body 308 has a width 314 and height 320 less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, the body height 320 is between ½ the body width 314 to 2 times the body width 314.

[0018] Tri-gate transistor 300 has a gate dielectric layer 322. Gate dielectric layer 322 is formed on and around three sides of each of the semiconductor bodies 308 as shown in Figure 3A and 3B. Gate dielectric layer 322 is formed on or adjacent to sidewall 312, on top surface 316 and on or adjacent to sidewall 310 of body 308 as shown in Figure 3. Gate dielectric layer 322 can be any well-known gate dielectric layer. In an embodiment of the present invention, the gate dielectric layer is a silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) or a silicon nitride (Si_3N_4) dielectric layer. In an embodiment of the present invention, the gate dielectric layer 322 is a silicon oxynitride film formed to a thickness of between 5-20Å. In an embodiment of the present invention, gate dielectric layer 322 is a high K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentaoxide (Ta_2O_5), titantium oxide (TiO_2), hafnium oxide (HfO_2), $HfSiO_xN_y$, zirconium oxide (ZrO_2) and lanthanum oxide LaO_2). Gate dielectric layer 322 can be other types of high K dielectricS, such as but not limited to PZT.

[0019] Tri-gate device 300 has a gate electrode 324. Gate electrode 324 is formed on and around gate dielectric layer 322 as shown in Figure 3A and 3B. Gate electrode 324 is formed on or adjacent to gate dielectric 322 formed on sidewall 312 of semiconductor body 308, is formed on gate dielectric 322 formed on the top surface 316 of semiconductor body 308, and is formed adjacent to or

on gate dielectric layer 322 formed on sidewall 310 of semiconductor body 308. Gate electrode 324 has a pair of laterally opposite sidewalls 326 and 328 separated by a distance which defines the gate length (Lg) 330 of transistor 300. In an embodiment of the present invention the laterally opposite sidewalls 326 and 328 of the gate electrode 324 run in a direction perpendicular to the laterally opposite sidewalls 310 and 312 of semiconductor body 308.

[0020] Gate electrode 324 can be formed of any suitable gate electrode material. In an embodiment of the present invention to gate electrode 324 comprises of polycrystalline silicon doped to a concentration density between $1x10^{19}$ atoms/cm^3 – $1x10^{21}$ atoms/cm^3. In an embodiment of the present invention the gate electrode can be a metal gate electrode, such as but not limited to, tungsten, tantalum, titanium, and their nitrides or alloys of various metallic systems. In an embodiment of the present invention the gate electrode is formed from a material having a work function between 3.9-5.3 eV. It is to be appreciated, the gate electrode 324 need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

[0021] Tri-gate transistor 300 has a source region 330 and a drain region 332. Source region 330 and drain region 332 are formed in semiconductor body 308 on opposite sides of gate electrode 324 as shown in Figure 3A. The source region 330 and the drain region 332 are formed of the same conductivity type such as N-type or P-type conductivity. In an embodiment of the present invention source region 330 and drain region 332 have a doping concentration of between $1x10^{19}$ and $1x10^{21}$ atoms/cm^3. Source region 330 and drain region 332 can be formed of uniform concentration or can include subregions of different concentrations or doping profiles such as tip regions (e.g., source/drain extensions). In an embodiment of the present invention when transistor 300 is a symmetrical transistor, source region 330 and drain region 332 will have the same doping

concentration and profile. In an embodiment of the present invention when tri-gate transistor 300 is formed as an asymmetric transistor then the doping concentration and profile of the source region 330 and the drain region 332 may vary in order to obtain a particular electrical characteristic.

[0022] The portion of semiconductor body 308 located between source region 330 and drain region 332, defines the channel region 350 of transistor 300. The channel region 350 can also be defined as the area of the semiconductor body 308 surrounded by the gate electrode 324. At times however, the source/drain region may extend slightly beneath the gate electrode through, for example, diffusion to define a channel region slightly smaller than the gate electrode length (Lg). In an embodiment of the present invention channel region 350 is intrinsic or undoped monocrystalline silicon. In an embodiment of the present invention, channel region 350 is doped monocrystalline silicon. When channel region 350 is doped it is typically doped to a conductivity level of between $1x10^{16}$ to $1x10^{19}$ atoms/cm3. In an embodiment of the present invention, when the channel region is doped it is typically doped to the opposite conductivity type of the source region 330 and the drain region 332. For example, when the source and drain regions are N-type conductivity the channel region would be doped to p type conductivity. Similarly, when the source and drain regions are P type conductivity the channel region would be N-type conductivity. In this manner a tri-gate transistor 300 can be formed into either a NMOS transistor or a PMOS transistor respectively. Channel region 350 can be uniformly doped or can be doped non-uniformly or with differing concentrations to provide particular electrical and performance characteristics. For example, channel regions 350 can include well-known "halo" regions, if desired.

[0023] By providing a gate dielectric and a gate electrode which surrounds the semiconductor body on three sides, the tri-gate transistor is characterized in having three channels and three gates, one (g1) which extends between the

source and drain regions on side 312 of silicon body 308, a second (g2) which extends between the source and drain regions on the top surface 316 of silicon body 308, and the third (g3) which extends between the source and drain regions on the sidewall 310 of silicon body 308 as shown in Figure 3A and Figure 3B. The gate "width" (Gw) of transistor 300 is the sum of the widths of the three channel regions. That is, the gate width of transistor 300 is equal to the height 320 of silicon body 308 at sidewall 310, plus the width of silicon body of 308 at the top surface 316, plus the height 320 of silicon body 308 at sidewall 312. Larger "width" transistors can be obtained by using multiple devices coupled together (e.g., multiple silicon bodies 308 surrounded by a single gate electrode 324 as shown in Figure 3A).

[0024] As stated above the gate "width" of transistor 300 is equal to the sum of the three gate width created from semiconductor body 308 of transistor 300. In order to fabricate the transistors with larger gate widths, transistor 300 can include an additional or multiple semiconductor bodies or fingers 308 as shown in Figure 3A. Each semiconductor body 308 has a gate dielectric layer 322 formed on its top surface and sidewalls as shown in Figure 3A and Figure 3B. Gate electrode 324 is formed on and adjacent to each gate dielectric 322 on each of the semiconductor bodies 308. Each semiconductor body 308 also includes a source region 330 and a drain region 332 formed in the semiconductor body 308 on opposite sides of gate electrode 324 as shown in Figure 3A. In an embodiment of the present invention each semiconductor body 308 is formed with the same width and height (thickness) as the other semiconductor bodies 308. In an embodiment of the present invention each source regions 330 and drain regions 332 of the semiconductor bodies 308 are electrically coupled together by the semiconductor material used to form semiconductor body 308 to form a source landing pad 460 and a drain landing pad 480 as shown in Figure 3A. Alternatively, the source regions 330 and drain regions 332 can be coupled together by higher levels of

metalization (e.g., metal 1, metal 2, metal 3...) used to electrically interconnect various transistors 300 together into functional circuits. The gate width of transistor 300 as shown in Figure 3A would be equal to the sum of the gate width created by each of the semiconductor bodies 308. In this way, the tri-gate transistor 300 can be formed with any gate width desired.

[0025] Additionally, as shown in Figure 3A and Figure 3B, the tri-gate device of the present invention includes a film 360 which imparts a stress to the channel region 350 of the device. By applying a proper stress to the channel region, the mobility of the carriers (i.e., electrons or holes) for the device can be increased and the device performance improved. In an embodiment of the present invention, stress incorporating film 360 is formed on and around exposed portions of semiconductor body 308 as shown in Figure 3A and Figure 3B. Additionally, in an embodiment of the present invention, the stress incorporating film 360 is formed over and around the gate electrode 324. In an embodiment of the present invention, the stress incorporating film 360 is formed directly on exposed top portion 322 of silicon body 308 as well as directly on or adjacent to sides 310 and 312 of semiconductor body 360. Additionally, in an embodiment of the present invention, the stress incorporating film 360 is also formed directly on and adjacent to gate electrode 324.

[0026] Additionally, in an embodiment of the present invention, the stress incorporating film 360 is also formed directly beneath the bottom surface 318 of semiconductor body 308 including beneath the channel region 350 of the semiconductor body 308 as shown in Figure 3A and Figure 3B. The stress incorporating film can be formed beneath the semiconductor body or bodies by first removing a portion of the barried oxide or insulator 306 beneath the semiconductor body and then back filling the region with a stress incorporating film. By including a stress incorporating film directly beneath the bottom surface of the channel region 350 of semiconductor bodies 308, the stress material 360

completely surrounds the channel and provides stress from all side of the channel and not just the top.

[0027] In an embodiment of the present invention, the film 360 has a compressive stress so that the semiconductor body and especially the channel region of the semiconductor body is under a tensile stress. A channel region width a tensile stress improves the mobility of electrons and therefore is ideal for use in a NMOS device where the carriers are electrons. In an embodiment of the present invention, the stress incorporating film 360 is a film having suitable compressive stress to produce a tensile stress between 0.5-5.0 GPa and ideally about 1 GPa in the channel region of the semiconductor body. In an embodiment of the present invention, the stress incorporating film 360 has a thickness between 10-200 nanometers. In an embodiment of the present invention, the stress film 360 improves carrier mobility by 20-80 percent.

[0028] In an embodiment of the present invention, the film 360 has a tensile stress so that the semiconductor body 308 and especially the channel region 350 of the semiconductor body is under a compressive stress. A channel region under a compressive stress improves the mobility of holes and therefore is ideal for use in a PMOS device where the carriers are holes. In an embodiment of the present invention, the film 360 is a film having a suitable tensile stress to produce a compressive stress between 0.5-5.0 GPa in the channel region of the silicon body 308. In an embodiment of the present invention, the thin film 360 is a silicon nitride film having a tensile stress.

[0029] In an embodiment of the present invention, a thin oxide or passivating film 319 is formed on the underside 318 of the semiconductor bodies in order to help reduce parasitic leakage effects. In an embodiment of the present invention, the passivating film 319 includes SiO_2 and can be formed to a thickness greater than about 1 nanometer.

[0030] Because the channel region 350 is surrounded on three sides by gate electrode 324 and gate dielectric 322, transistor 300 can be operated in a fully depleted manner wherein when transistor 300 is turned "on" the channel region 350 fully depletes thereby providing the advantageous electrical characteristics and performance of a fully depleted transistor. That is, when transistor 300 is turned "ON" a depletion region is formed in channel region 350 along with an inversion layer at the surfaces of region 350 (i.e., an inversion layer is formed on the side surfaces and top surface of the semiconductor body). The inversion layer has the same conductivity type as the source and drain regions and forms a conductive channel between the source and drain regions to allow current to flow therebetween. The depletion region depletes free carriers from beneath the inversion layer. The depletion region extends to the bottom of channel region 350, thus the transistor can be said to be a "fully depleted" transistor. Fully depleted transistors have improved electrical performance characteristics over non-fully depleted or partially depleted transistors. For example, operating transistor 300 in a fully depleted manner, gives transistor 300 an ideal or very steep subthreshold slope. The tri-gate transistor can be fabricated with very steep sub-threshold slope of less than 80 mV/decade, and ideally about 60 mV/decade even when fabricated with semiconductor body thicknesses of less than 30 nm. Additionally, operating transistor 300 in the fully depleted manner, transistor 300 has an improved drain induced barrier (DIBL) low in effect which provides for better "OFF" state leakage which results in lower leakage and thereby lower power consumption. In an embodiment of the present invention the tri-gate transistor 300 has a DIBL effect of less than 100mV/V and ideally less than 40 mV/V.

[0031] Figure 6 is an illustration of two plots 602 and 604 which set forth the body height and body width which will produce either fully depleted (F.D) or partially depleted (P.D) tri-gate transistors having gate length (Lg) of 30 nm (602) and 20

nm (604) respectively. In an embodiment of the present invention, the body height, body width and gate length are chosen to have dimensions in which a fully depleted transistor will be formed. In other embodiments, the tri-gate transistor has a body height, body width and gate length such that a partially depleted transistor is formed.

[0032] The tri-gate transistor of the present invention can be said to be a non-planar transistor because the inversion layer of the channel region 350 is formed in both the horizontal and vertical directions in semiconductor body 308. The semiconductor device of the present invention can also be considered a non-planar device because the electric field from the gate electrode 324 is applied from both horizontal (g2) and vertical sides (g1 and g3).

[0033] In an embodiment of the present invention tri-gate transistor 300 can include other films or features, such as a silicon or other semiconductor film 410, sidewall spacer 420 and silicide 430 formed prior to forming the stress incorporating film 360 as shown in Figure 4. For example, in an embodiment of the present invention a semiconductor film 410 is formed on the source region 330 and on the drain region 332 of semiconductor body 308 to form "raised" source and drain regions. Semiconductor film 410 can be a silicon film or a silicon alloy such as silicon germanium (Si_xGe_y). In an embodiment of the present invention the semiconductor film 410 is a single crystalline silicon film formed of the same conductivity type as the source region 330 and drain region 332. In an embodiment of the present invention the semiconductor film can be a silicon alloy such as silicon germanium wherein silicon comprises approximately 1 to 99 atomic percent of the alloy. The semiconductor film 410 need not necessarily be a single crystalline semiconductor film and in an embodiment can be a polycrystalline film. Semiconductor film 410 can be electrically isolated from a gate electrode 324 by a pair of dielectric sidewall spacers 420 such as silicon nitride or silicon oxide or composites thereof. Sidewall spacers 420 run along the

laterally opposite sidewalls 326 and 328 of gate electrode 324 as shown in Figure 4 thereby isolating the semiconductor film 410 from gate electrode 324 as shown in Figure 4. An embodiment of the present invention sidewalls spacers 420 have a thickness of between 20-200Å. By adding a silicon or semiconductor film to the source and drain regions 330 and 332 of the semiconductor body and forming "raised" source and drain regions, the thickness of the source and drain regions is increased thereby reducing the source/drain contact resistance to transistor 300 and improving its electrical characteristics and performance.

[0034] In an embodiment of the present invention a silicide film 430, such as, but not limited to, titanium silicide, nickel silicide, and cobalt silicide is formed on the source region 330 and drain region 332. In an embodiment of the present invention silicide film 430 is formed on a silicon film 410 of silicon body 308 as shown in Figure 4. Silicide film 430 however can also be formed directly onto the top surface 316 of silicon body 308. For example, silicide film 430 can be formed on silicon body 308 by first forming a silicon film such as an undoped silicon film and a silicon body and then completely consuming the silicon film during the silicide process. Dielectric spacers 420 enables silicide film 430 to be formed on semiconductor body 308 or silicon film 410 in a self-aligned process (i.e., a salicide process).

[0035] Additionally, in the embodiment of the present invention a semiconductor or silicon film 440 can also be formed on the top of gate electrode 324 as can a silicide film 450 on the top surface gate electrode 325 as can be a silicide film 450. Silicide film 450 and silicon film 440 are typically formed at the same time as silicide film 430 and silicon film 420 on silicon body 308. The formation of a silicon film 440 on silicide film 450 on the gate electrode reduces the contact resistance to the gate thereby improving the electrical performance of transistor 300.

[0036] A method of fabricating a tri-gate transistor in accordance with embodiments of the present invention is illustrated in Figures 5A-5E. The

fabrication of a tri-gate transistor begins with substrate 502. A silicon or semiconductor film 508 is formed on substrate 502 as shown in Figure 5A. In an embodiment of the present invention, the substrate 502 is an insulating substrate, such as shown in Figure 5A. In an embodiment of the present invention, insulating substrate 502 includes a lower monocrystalline silicon substrate 504 and a top insulating layer 506, such as a silicon dioxide film or silicon nitride film. Insulating layer 506 isolates semiconductor film 508 from substrate 504, and in embodiment is formed to a thickness between 200-2000Å. Insulating layer 506 is sometimes referred to as a "buried oxide" layer. When a silicon or semiconductor film 508 is formed on an insulating substrate 502, a silicon or semiconductor on insulating (SOI) substrate 500 is created. In other embodiments of the present invention, the substrate 502 can be a semiconductor substrate, such as but not limited to a silicon monocrystalline substrate and a gallium arsenide substrate.

[0037] Although semiconductor film 508 is ideally a silicon film, in other embodiments it can be other types of semiconductor films in which carrier mobility can be enhanced when under stress, such as but not limited to a silicon germanium alloy (Si_xGe_y) with less than 25% Ge, and III-V materials such as, gallium arsenide (GaAs), InSb, GaP and GaSb. In an embodiment of the present invention, semiconductor film 508 is an intrinsic (i.e., undoped) silicon film. In other embodiments, semiconductor film 508 is doped to a p type or n type conductivity with a concentration level between $1x10^{16}$-$1x10^{19}$ atoms/cm^3. Semiconductor film 508 can be insitu doped (i.e., doped while it is deposited) or doped after it is formed on substrate 502 by for example ion-implantation. Doping after formation enables both PMOS and NMOS tri-gate devices to be fabricated easily on the same insulating substrate. The doping level of the semiconductor body at this point determines the doping level of the channel region of the device.

[0038] Semiconductor film 508 is formed to a thickness which is approximately equal to the height desired for the subsequently formed semiconductor body or

bodies of the fabricated tri-gate transistor. In an embodiment of the present invention, semiconductor film 508 has a thickness or height 509 of less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, semiconductor film 508 is formed to the thickness approximately equal to the gate "length" desired of the fabricated tri-gate transistor. In an embodiment of the present invention, semiconductor film 508 is formed thicker than desired gate length of the device. In an embodiment of the present invention, semiconductor film 508 is formed to a thickness which will enable the fabricated tri-gate transistor to be operated in a fully depleted manner for its designed gate length (Lg).

Semiconductor film 508 can be formed on insulating substrate 502 in any well-known method. In one method of forming a silicon on insulator substrate, known as the SIMOX technique, oxygen atoms are implanted at a high dose into a single crystalline silicon substrate and then anneal to form the buried oxide 506 within the substrate. The portion of the single crystalline silicon substrate above the buried oxide becomes the silicon film 508. Another technique currently used to form SOI substrates is an epitaxial silicon film transfer technique which is generally referred to as bonded SOI. In this technique a first silicon wafer has a thin oxide grown on its surface that will later serve as the buried oxide 506 in the SOI structure. Next, a high dose hydrogen implant is made into the first silicon wafer to form a high stress region below the silicon surface of the first wafer. This first wafer is then flipped over and bonded to the surface of a second silicon wafer. The first wafer is then cleaved along the high stress plain created by the hydrogen implant. This results in a SOI structure with a thin silicon layer on top, the buried oxide underneath all on top of the single crystalline silicon substrate. Well-known smoothing techniques, such as HC smoothing or chemical mechanical polishing (CMP) can be used to smooth the top surface of semiconductor film 508 to its desired thickness.

[0039] At this time, if desired, isolation regions (not shown) can be formed into SOI substrate 502 in order to isolate the various transistors to be formed therein from one another. Isolation regions can be formed by etching away portions of the substrate film 508 surrounding a tri-gate transistor, by for example well-known photolithographic and etching techniques, and then back filling the etched regions with an insulating film, such as SiO_2.

[0040] Next, standard photolithography and etching techniques are used to define semiconductor bodies or fins 520 in the semiconductor film 508 for the tri-gate transister as shown in Figure 5B. In an embodiment of the present invention, the fins or bodies 520 are patterned to have a width 518 which is equal to or greater than the width desired of the gate length (Lg) of the fabricated transistor. In this way, the most stringent photolithography constraints used to fabricate the transistor are associated with the gate electrode patterning and not the semiconductor body or fin definition. In an embodiment of the present invention, the semiconductor bodies or fins will have a width 518 less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers. In an embodiment of the present invention, the semiconductor bodies or fins have a width 518 approximately equal to the silicon body height 509. In an embodiment of the present invention, the fins or bodies 520 have a width 518 which is between ½ the semiconductor body height 509 and two times the semiconductor body height 509.

[0041] Additionally, as shown in Figure 5B, the photolithography and etching step can also be used to form source landing pads 522 and drain landing pads 524 from the semiconductor film. The landing pads can be used to connect together the various source regions and to connect together the various drain regions of the fabricated transistor.

[0042] The semicoductor film 508 can be patterned into fins and landing pads utilizing well known photolithography and etching techniques which generally

include the formation of a photoresist mask by masking, exposing, and developing a blanket deposited photoresist film as is well known in the art, and then etching semiconductor film in alignment with the photoresist mask to form one or more silicon bodies or fins 520 and source and drain landing pads 522 and 524 respectively. Semiconductor film 508 is etched until the underlying buried oxide layer 506 is exposed. Well-known semiconductor etching techniques, such as anisotropic plasma etching or reactive ion etching can be used to etch semiconductor film 508 in alignment with the photoresist mask. After semiconductor film 508 is etched to form semiconductor bodies or fins 520 (and source/drain landing pads 522 and 524, if desired) the photoresist mask is removed by well-known techniques, such as by chemical stripping and O2 ashing, to produce the substrate shown in Figure 5B.

[0043] Next, a gate dielectric layer 526 is formed on and around each semiconductor body 520. That is, a gate dielectric layer 526 is formed on the top surface 527 of each of the semiconductor bodies 520 as well as on the laterally opposite sidewalls 528 and 529 of each of the semiconductor bodies 520. The gate dielectric can be a deposited dielectric or a grown dielectric. In an embodiment of the present invention, the gate dielectric layer 526 is a silicon dioxide dielectric film grown with a dry/wet oxidation process. In an embodiment of the present invention, the silicon oxide film is grown to a thickness of between 5-15Å. In an embodiment of the present invention, the gate dielectric film 526 is a deposited dielectric, such as but not limited to a high dielectric constant film, such as metal oxide dielectric, such as tantalum pentaoxide (Ta_2O_5), titanium oxide (TiO_2), hafnium oxide (HfO_2), $HfSiO_xN_y$, zirconium oxide (ZrO_2) and lanthanum oxide LaO_2) or other high-K dielectrics, such as PZT and BST. A high dielectric constant film can be formed by any well-known technique, such as by chemical vapor deposition (CVD).

[0044] Next, as also shown in Figure 5C, a gate electrode 530 is formed. The gate electrode 530 is formed on the gate dielectric layer 526 formed on the top surface 527 of each of the semiconductor bodies 520 and is formed on or adjacent to the gate dielectric 526 formed on or adjacent to the sidewalls 528 and 529 of each of the semiconductor bodies as shown in Figure 5E. The gate electrode 530 has a top surface 532 opposite of bottom surface formed on the insulating substrate 502 and has a pair of laterally opposite sidewalls 534 and 536. The distance between the laterally opposite sidewalls 534 and 536 define the gate length (Lg) 538 of the tri-gate transistor. Gate electrode 530 can be formed by blanket depositing a suitable gate electrode material over the substrate and then patterning the material into an electrode 530. The gate electrode can be formed to a thickness 533 between 200-3000Å. In an embodiment the gate electrode has a thickness or height 533 of at least three times the height 509 of semiconductor bodies 520. The gate electrode material is then patterned with well-known photolithography and etching techniques to form gate electrode 530 from the gate electrode material. In embodiment of the present invention, the gate electrode material comprises polycrystalline silicon. In another embodiment of the present invention, the gate electrode material comprises a polycrystalline silicon germanium alloy. In yet other embodiment of the present invention, the gate electrode material can comprise a metal film, such as tungsten, tantalum, and their nitrides. Gate electrode 530 can be formed by well-known techniques, such as by blanket depositing a gate electrode material over the substrate of Figure 5B and then patterning the gate electrode material with well-known photolithography and etching techniques. In an embodiment of the present invention, the photolithography process used to define gate electrode 530 utilizes the minimum or smallest dimension lithography process used to fabricate the tri-gate transistor. (That is, in an embodiment of the present invention, the gate length (Lg) 538 of gate electrode 530 has a minimum feature dimension of the

transistor defined by photolithography.) In an embodiment of the present invention, the gate length 538 is less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers.

[0045] Next, source and drain regions for the transistor are formed in semiconductor body 520 on opposite sides of gate electrode 530. In an embodiment of the present invention, the source and drain regions include tip or source/drain extension regions. Source and drain extension regions 540 and 542, respectively, can be formed by placing dopants 544 into semiconductor bodies 520 on both sides 532, 534 of gate electrode 530 in order to form tip regions 540 and 542 as shown in Figure 5D. For a PMOS tri-gate transistor, the semiconductor fins or bodies 520 are doped to a p type conductivity and to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. For a NMOS tri-gate transistor, the semiconductor fins or bodies 520 is doped with n type conductivity ions to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. In an embodiment of the present invention, the silicon films are doped by ion-implantation. In an embodiment of the present invention, the ion-implantation occurs in a vertical direction (i.e., a direction perpendicular to substrate 502). When gate electrode 530 is a polysilicon gate electrode, it can be doped during the ion-implantation process. Gate electrode 530 acts as a mask to prevent the ion-implantation step from doping the channel region(s) 548 of the tri-gate transistor. The channel region 548 is the portion of the silicon body 520 located beneath or surrounded by the gate electrode 530. If gate electrode 530 is a metal electrode, a dielectric hard mask maybe used to block the doping during the ion-implantation process. In other embodiments, other methods, such as solid source diffusion, may be used to dope the semiconductor body to form source and drain extensions.

[0046] In embodiments of the present invention, "halo" regions can be formed in silicon body prior to the formation of a source/drain regions or source/drain extension regions. Halo regions are doped regions formed in the channel region

548 of the device and are of the same conductivity but of a slightly higher concentration than the doping of the channel region of the device. Halo regions can be formed by ion-implantating dopants beneath the gate electrode by utilizing large angled ion-implantation techniques.

[0047] Next, if desired, the substrate shown in Figure 5C can be further processed to form additional features, such as heavily doped source/drain contact regions, deposited silicon on the source and drain regions to form raised source and drain regions, as well as the gate electrode, and the formation of silicide on the source/drain contact regions as well as on the gate electrode.

[0048] Next, as shown in Figure 5D, the buried oxide layer 506 located underneath and adjacent to the semiconductor fins or bodies is removed to form an air gap 560 in the buried oxide layer. The buried oxide layer can be removed by using a selective etch which preferencely etches the buried insulating film without substantially etching away the semiconductor body. When the semiconductor bodies are silicon and the buried insulating layer 506 is a silicon oxide, the buried silicon oxide layer can be selectively etched away with a buffered HF etchant. It is to be appreciated that any suitable wet or dry etch technique which can selectively etch away the buried insulating layer without etching away the semiconductor body may be utilized to form air gaps 560. An etchant with a selectivity of greater than 10 is desirable.

[0049] The buried insulator etch can be performed on the wafer with or without a patterning layer depending upon the layout of the device. Typically a patterned photoresist mask will be utilized which exposes the transistors which are to receive the subsequent stress film and covers those transistors which are not to include a stress film.

[0050] In an embodiment of the present invention, after the removal of the buried insulating film from beneath the semiconductor fins or bodies, a short oxidation or passivation step can be performed to passivate the bottom of the exposed fins in

order to reduce parasitic leakeage effects. Any suitable oxidation or passivation process can be used to form the passivating dielectric. In an embodiment of the present invention, the bottom of the fins are passivated by SiO_2 to form a passivating oxide film having a thickness greater than about 1 nanometer.

[0051] After the underlying insulating film 506 is removed and passivation or oxidation complete, a filling step of the stress incorporation film 560 can begin. The stress incorporation film 560 must be an insulating film in order to prevent shorts from the source to the drain. The purpose of the stress incorporation film is to provide stress in the channel region of the device. The type of stress in the stress incorporation film depends upon the type of device being fabricated. For a NMOS device where the carriers are electrons, the channel regions need to be under tensile stress to increase mobility of electrons. In order to place the channel region under tensile stress, the stress incorporation film 560 needs to be a compressive film. Additionally, the process used to form the stress incorporation film 560 should be a conformal process, such as a vapor phase deposition, which can blanket deposit the film equally on vertical and horizontal surfaces and be able to fill underneath the semiconductor bodies. It is desirable that the stress incorporation film be able to completely fill the regions underneath the fins or bodies of the device. This can be facilitated by making narrower fins or making the underlying insulating film layer 506 thicker in order to improve the aspect ratio of the fill under the channel regions. In an embodiment of the present invention, the stress incorporation film is a compressive silicon nitride film. In an embodiment of the present invention, an NMOS device is fabricated with a compressive silicon nitride film formed by chemical vapor deposition (CVD) utilizing a reactant gas mixture comprising dichloro-silane (DCS) and ammonia (NH_3). BTBAS can also be used in place of DCS. Such a process will blanket deposit a silicon nitride film over the substrate with equal deposition on horizontal

and vertical surfaces and enable the filling of the air gap beneath the silicon bodies.

[0052] For a PMOS device where the carriers are holes, the channel regions needs to be in compression to increase the mobility of the holes. In order to place the channel in compression, the stress incorporation film needs to be a tensile film. In an embodiment of the present invention, the stress incorporation film is a tensile silicon nitride film.

[0053] In an embodiment of the present invention, the stress incorporation film is formed to a thickness sufficient to completely fill the air gap regions beneath the semiconductor bodies and channel region and completely surround the semiconductor body and gate electrode as shown in Figure 5E. The stress incorporation film completely surrounds the device and provides stress over a large area resulting in the desired stress in the channel to improve mobility. Additionally, in embodiments of the present invention, the film stress properties are modulated during deposition in order to optimize the film for device performance.

[0054] After deposition is completed, a masking and etch step can be used to remove the stress incorporation film from area where it is not desired, and processing continued in a normal manner to form "back end" features, such as metal interconnects and interlayer dielectrics to electrically couple the individual transistors together into a functional circuit.

[0055] Thus, a novel non-planar device with a stress incorporation film and its method of fabrication have been described.

IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate;

a gate dielectric formed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a film formed adjacent to said semiconductor body wherein said film produces a stress in said semiconductor body.

2. The semiconductor device of claim 1 wherein said film produces a compressive stress in said semiconductor body.

3. The semiconductor device of claim 1 wherein said film produces a tinsel stress in said semiconductor body.

4. The semiconductor device of claim 1 wherein said film has tinsel stress.

5. The semiconductor device of claim 1 wherein said film has a compressive stress.

6. The semiconductor device of claim 5 wherein said compressive film comprises silicon nitride.

7. The semiconductor device of claim 1 wherein said semiconductor body is a single crystalline silicon film.

8. The semiconductor device of claim 1 wherein said semiconductor is selected from the group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

9. A tri-gate transistor comprising:

a single crystalline silicon body formed on insulating substrate, said silicon body having a top surface opposite a bottom surface and a first and second laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body and on said first and second laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric and on said top surface of said silicon body and adjacent to said gate dielectric on said first and second laterally opposite sidewalls of said silicon body;

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode; and

a stress induced film formed around said silicon body and said gate electrode, said film providing stress in the channel region of said device.

10. The method of claim 9 wherein said thin film has a compressive stress and places a tinsel stress in said channel region.

11. The semiconductor device of claim 10 wherein said thin film comprises a silicon nitride film.

12. The semiconductor device of claim 9 wherein said thin film has tinsel stress and incorporates a compressive stress into said channel region of said semiconductor body.

13. The tri-gate transistor of claim 10 wherein said semiconductor body channel region is doped to a p type conductivity with a concentration level between $1x10^{16} - 1x10^{19}$ atoms/cm^3.

14. The tri-gate device of claim 12 wherein said channel region of said semiconductor body is doped to a n type conductivity with a concentration level between $1x10^{16} - 1x10^{19}$ atoms/cm^3.

15. The tri-gate transistor of claim 9 wherein said thin film completely surrounds said semiconductor body and said gate electrode.

16. The method of claim 9 wherein a thin grown oxide layer is formed between the bottom of said semiconductor body and said thin film.

17. A method of forming a semiconductor device comprising:

forming a semiconductor body having a top surface and laterally opposite sidewalls on a insulating substrate;

forming a gate dielectric on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

forming a gate electrode on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

forming a thin film adjacent to said semiconductor body wherein said thin film produces a stress in said semiconductor body.

18. The method of claim 17 wherein said thin film produces a compressive stress in said semiconductor body.

19. The method of claim 17 wherein said thin film produces a tinsel stress in said semiconductor body.

20. The method of claim 17 wherein said thin film has a tinsel stress.

21. The method of claim 17 wherein said thin film has a compressive stress.

22. The method of claim 17 wherein said semiconductor body comprises a single crystalline silicon film.

23. The method of claim 17 wherein said semiconductor body is selected from the group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb, and carbon nanotubes.

24. A method of forming nonplanar transistor comprising:

patterning a monocrystalline silicon film formed on an insulating substrate into a silicon body having a top surface opposite a bottom surface formed on said insulating film, and a first and second laterally opposite sidewalls;

forming a gate dielectric layer on said top surface of said silicon body and on said sidewalls of said silicon body;

depositing a gate material over said silicon body and over said insulating substrate;

patterning said gate material to form a gate electrode on said gate dielectric layer on said top surface of said silicon body in adjacent to said gate dielectric on said sidewalls of said silicon body, said gate electrode having laterally opposite

sidewalls which run perpendicular to said laterally opposite sidewalls of said silicon body;

forming a pair of source/drains regions in said silicon body on opposite sides of said laterally opposite sidewalls of said gate electrode, wherein the region between said source/drain regions in said silicon body forms a channel region;

removing a portion of said insulating substrate from underneath a portion of channel region of said silicon body and beneath a portion of said source and drain regions of said silicon body; and

forming a film having a stress therein beneath said exposed portion of said silicon body beneath said gate electrode and beneath said exposed portion of said source and drain regions beneath said gate electrode.

25. The method of claim 24 wherein said thin film has compressive stress which produces a tinsel stress in said channel region.

26. The method of claim 24 wherein said thin film has a tinsel stress which produces a compressive stress in said channel region of said semiconductor body.

27. The method of claim 24 further comprising forming said thin film adjacent to said laterally opposite sidewalls of said silicon body and said laterally opposite sidewalls of said gate electrode.

28. The method of claim 24 wherein said formation of said thin film is continued until said silicon body and said gate electrode are completely surrounded by said thin film.

29. The method of claim 24 further comprising oxidizing said bottom portion of said semiconductor body after exposing said semiconductor body and prior to forming said thin film.