Diode-Based Devices and Methods for Making the Same

TECHNICAL FIELD

[0003] This patent application relates to semiconductor diodes made from compound semiconductors or other lattice mismatched semiconductors on silicon wafers, as well as methods of fabricating such semiconductor diodes, and more particularly, for photonic applications such as light emitting diodes (LEDs), lasers, photovoltaics, and other optoelectronic uses.

BACKGROUND

[0004] This section provides background information and introduces information related to various aspects of the disclosures that are described and/or claimed below. These background statements are not admissions of prior art.

[0005] The majority of chip manufacturing takes advantage of silicon processing on high-quality, large-area, low-cost silicon wafers. Commercial manufacturers of devices made from compound semiconductors such as gallium arsenide and indium phosphide generally have been unable to take advantage of silicon wafers. They typically build light emitting diodes (LEDs), multi junction solar cells, and other compound semiconductor devices on small, expensive wafers made of materials such as sapphire, germanium, gallium arsenide, or silicon carbide.

[0006] The challenge of making compound semiconductor devices on inexpensive substrates has widespread economic implications. Compound semiconductors are an important component of our communications infrastructure because they can emit and detect light. They are the materials in the lasers that transmit signals through optical fibers, the sensors that receive those signals, the amplifiers in cellular telephones, the amplifiers in cell phone base stations, and the circuits that transmit and receive microwave signals.

[0007] Light emitting diodes typically consist of gallium nitride films deposited onto sapphire or silicon carbide wafers. These exotic substrates contribute to the high cost of LEDs. A sapphire wafer 4 inches in diameter typically costs around $130, and a 2-inch silicon carbide wafer can cost about $2000. By contrast, an 8-inch silicon wafer, which provides four times as much

surface area as a 4-inch wafer and 16 times as much surface area as a 2-inch wafer, typically costs less than $100.

[0008] High-efficiency multi junction solar cells typically contain layers of germanium, gallium arsenide, and indium gallium phosphide deposited onto germanium wafers. As is the case with wafers for LEDs, germanium wafers similarly are smaller and significantly more expensive than silicon wafers.

[0009] The ability to create compound semiconductor devices on silicon wafers facilitates market growth in several key industries.

[0010] Two key technical barriers have prevented the fabrication of compound semiconductor devices on silicon wafers: the mismatch of lattice constants and the mismatch of thermal expansion coefficients.

[0011] *Lattice Mismatch:* In a crystal, the atoms sit in a regular periodic array known as a lattice. The distance between the atoms, known as the "lattice constant," is typically a few ångstroms (1 ångstrom = 10^{-10} meter). Silicon has a smaller lattice constant than many compound semiconductors. When compound semiconductors grow on silicon, crystalline imperfections known as *misfit dislocations* appear at the interface. The misfit dislocations create other crystalline defects known as *threading dislocations,* which propagate upward from the interface. Threading dislocations diminish the performance and the reliability of compound semiconductor devices such as lasers, solar cells, light-emitting diodes, etc.

[0012] *Thermal Contraction Mismatch:* Compound semiconductors typically grow at high temperatures, which can exceed 1000°C. When the wafer cools, the compound semiconductor

film may contract more than the silicon wafer. As a result, the wafer may bow in a concave manner, stressing and ultimately cracking the film.

[0013] Until recently, the most promising previous efforts to grow high-quality compound semiconductors onto silicon substrates have relied on three approaches: graded buffer layers, wafer bonding, or selective growth on mesas. None of these approaches has achieved commercial success.

[0014] In *graded buffer layers,* the composition of the material changes gradually from substantially pure silicon to a pure compound semiconductor. Since the lattice constant also changes gradually, crystalline defects are less likely to form at the interface. Unfortunately, the graded buffer layers have to be relatively thick (about ten microns for a 4% lattice mismatch). The thick buffer layer increases both the costs and the likelihood of cracking.

[0015] *Wafer bonding* involves growing devices on expensive substrates, then lifting off the devices and bonding them to a silicon wafer. This approach rules out modern silicon processing as a route to cost reduction. Furthermore, bonding typically requires temperatures above 300°C. When the materials cool, the compound semiconductors may crack because they contract more than the silicon wafer.

[0016] *Selective growth on a mesa* exploits the mobility of some dislocations. The strategy is to deposit compound semiconductors in small regions (10 to 100 microns in length), thereby providing a short path where mobile dislocations can glide to the edge of the region and remove themselves from the device. However, structures created by this technique typically have a high density of threading dislocations (more than 100 million per square centimeter). This technique cannot remove immobile dislocations, which predominate when the lattice mismatch exceeds 2%.

[0017] Aspect Ratio Trapping (J.S. Park et al., APL 90, 052113 (2007), hereby incorporated by reference in its entirety) is a recently developed technology that makes it possible to deposit high quality compound semiconductors, germanium or other lattice mismatched materials on silicon wafers. Figure 1 illustrates the principle of Aspect Ratio Trapping (ART). A thin film of dielectric material 20 such as silicon dioxide (SiO_2) or silicon nitride (SiN_x) is deposited onto a silicon wafer 10. Those of skill in the art can select a variety of dielectric materials such as SiO_xN_y, and silicates or oxides of material such as Hf and Zr, such as HfO.

[0018] A trench is etched in the dielectric material, and then deposit a non-lattice-matched semiconductor 30 such as germanium or a compound semiconductor in the trench. The threading dislocations 40, shown as dotted lines, propagate upward, typically at approximately a 45 degree angle from the interface, then intersect the sidewalls of the trench, where they terminate. Threading dislocations 40 cannot propagate down the length of the trench because crystal facets guide them to the sidewalls. Reference is made to the region in the trench where the sidewalls trap threading dislocations as the "trapping region" 50. The upper region of the non-lattice-matched semiconductor 30, above the trapping region 50, is a relatively defect-free region 60.

[0019] ART addresses the issue of cracking caused from mismatch of thermal expansion coefficients for these reasons: (1) the stresses are small because the epitaxial layers are thin; (2) the material can elastically accommodate the stresses arising from thermal expansion mismatch because dimensions of the ART openings are small; and (3) the SiO_2 pedestals, which are more compliant than the semiconductor materials, may deform to accommodate the stress.

SUMMARY OF THE DISCLOSURE

[0020] In accordance with an embodiment, a diode comprises a substrate, a dielectric material including an opening that exposes a portion of the substrate, the opening having an aspect ratio of at least 1, a bottom diode material including a lower region disposed at least partly in the opening and an upper region extending above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate, a top diode material proximate the upper region of the bottom diode material, and an active diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface of the substrate.

[0021] In accordance with another embodiment, a diode comprises a substrate, a bottom diode material that is lattice mismatched to the substrate, the bottom diode material extending above a top surface of the substrate and including a bottom diode section having a width across the top surface and a height above the top surface, the height being greater than the width, a top diode material proximate the bottom diode material, and an active light emitting diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface.

[0022] A further embodiment is a method of making a diode. The method comprises depositing a layer of a dielectric material on a substrate, patterning an opening in the dielectric material to expose a portion of the substrate, the opening having an aspect ratio of at least 1, forming a bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in and above the opening, forming an active diode region adjacent the bottom diode region, and forming a top diode region adjacent the active diode region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] For a more complete understanding of embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0024] Figure 1 illustrates the principle of Aspect Ratio Trapping (ART);

[0025] Figure 2 shows the generic structure of semiconductor diodes according to embodiments;

[0026] Figure 3 is a first embodiment of a diode configured in the shape of a fin;

[0027] Figures 4 and 5 are exemplary stages in the formation of the embodiment of Figure 3;

[0028] Figure 6 is an alternate embodiment of the embodiment of Figure 3;

[0029] Figure 7 summarizes a first method according to an embodiment for forming the embodiment of Figure 3;

[0030] Figure 8 summarizes a second method according to an embodiment for forming the embodiment of Figure 3;

[0031] Figures 9 and 10 show alternate steps for fabricating the embodiment of Figure 3;

[0032] Figure 11 summarizes a third method according to an embodiment for forming the embodiment of Figure 3;

[0033] Figures 12 through 15 show exemplary stages for forming an embodiment illustrated in Figure 16;

[0034] Figure 16 is an embodiment of a diode configured in the shape of a column;

[0035] Figure 17 summarizes a first method according to an embodiment for forming the embodiment in Figure 16;

[0036] Figures 18 and 19 illustrate steps in an alternate method for forming the embodiment in Figure 16;

[0037] Figure 20 summarizes the alternate method according to an embodiment for forming the embodiment in Figure 16;

[0038] Figure 21 shows a variation of the embodiment of Figure 16 in which an array of column-shaped diodes with circular cross sections is arranged in a hexagonal array according to another embodiment;

[0039] Figure 22 shows a top view of the embodiment in Figure 21;

[0040] Figures 23 and 24 illustrate exemplary stages for forming an embodiment illustrated in Figure 25;

[0041] Figure 25 is an embodiment of a diode in which the dielectric layer is transmissive rather than reflective;

[0042] Figure 26 summarizes a method according to an embodiment for forming the embodiment in Figure 25;

[0043] Figure 27 illustrates steps for forming another embodiment illustrated in Figure 28;

[0044] Figure 28 is an embodiment of a diode in which the silicon substrate has been removed;

[0045] Figure 29 summarizes a method for forming the embodiment in Figure 28;

[0046] Figures 30 and 31 show steps for forming an embodiment in Figure 32;

[0047] Figure 32 is an embodiment of a diode in which the top electrical contact also serves as a reflector;

[0048] Figure 33 summarizes a method according to an embodiment for forming the embodiment in Figure 32;

[0049] Figure 34 shows steps for forming an embodiment illustrated in Figure 35;

[0050] Figure 35 is an embodiment of a diode which takes advantages of the fact that gallium nitride and other III-nitride semiconductor materials naturally grow in the shape of a six-sided pyramid when they grow out of a hole or a trench in a dielectric layer;

[0051] Figure 36 summarizes a method according to an embodiment for forming the embodiment in Figure 35;

[0052] Figure 37 illustrate steps for forming the embodiment in Figure 38;

[0053] Figure 38 is an embodiment of a variation of the embodiment in Figure 35 in which the silicon substrate has been removed; and

[0054] Figure 39 summarizes a method according to an embodiment for forming the embodiment in Figure 38.

DETAILED DESCRIPTION

[0055] The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0056] The exemplary diode structures are generally discussed in the context of a single diode, although semiconductor engineers and others skilled in the art will understand that most applications require multiple diodes, typically integrated on a single chip.

[0057] In general, semiconductor diodes disclosed in this document have the generic structure illustrated in Figure 2. The structure comprises a substrate 101, a bottom diode region 102, an active diode region 103, a top diode region 104, an electrical contact on the top of the device 105, and an electrical contact on the bottom of the device 106. Each region 102, 103, and 104 can contain multiple layers.

[0058] The bottom diode region 102 and the top diode region 104 have opposite doping types. For example, if the bottom diode region 102 is predominantly n-type doped (with an electron *donor* such phosphorous, arsenic, or antimony), then the top diode region 104 will be predominantly p-type doped (with an electron *acceptor* such as boron or aluminum), and vice versa. Heavy doping in both the bottom diode region 102 and the top diode region 104 provides a low-resistance pathway for current to enter and leave the device. Typical doping levels of the top and bottom regions would be in the range of 10^{17}-10^{20} cm^{-3}. Typical doping level of the active region would be below 10^{17} cm^{-3}. Note that the use of "top" and "bottom" for designating

regions is a matter of convenience and in some frames of reference a top region can be located above a bottom region. For example, consider a diode formed above a substrate with its top region formed above its bottom region. If the diode is flip-chip bonded to a handle wafer and then the substrate is removed, the frame of reference for viewing the diode typically is flipped. In this case the top region will be viewed as being below the bottom region.

[0059] The substrate 101 is typically a silicon wafer, although in different embodiments a variety of other substrates including sapphire and silicon carbide are suitable. At least some portion of the substrate 101 will have the same predominant doping type (either n or p) as the bottom diode region 102. As a result, it will be possible to make good electrical contact between the bottom diode region 102 and the substrate 101.

[0060] The detailed structure of the active diode region 103 may depend upon numerous factors, including the intended application. In one form, the active diode region 103 is formed by the junction of the top diode region 104 and the bottom diode region 104. In this case, it can be desirable to vary the doping of the top and bottom regions near the junction. In an LED, the active diode region 103 may contain many layers that include both doped layers and thin undoped quantum wells where electrons and holes can recombine and generate photons. In another example of a solar cell, the active diode region 103 may consist of a single layer of moderately n-doped or moderately p-doped semiconductor material to absorb incident photons and generate an electron-hole pair.

[0061] The materials used to form the diode regions are well known to those of skill in the art. Typical examples of useful semiconductor materials are: Group IV materials, such as Si, C, or Ge, or alloys of these such as SiC or SiGe; Group II-VI compounds (including binary, ternary, and quaternary forms), e.g., compounds formed from Group II materials such as Zn, Mg, Be or Cd

and Group VI materials such as Te, Se or S, such as ZnSe, ZnSTe, or ZnMgSTe; and Group III-V compounds (including binary, ternary, and quaternary forms), e.g., compounds formed from Group III materials such as In, Al, or Ga and group V materials such as As, P, Sb or N, such as InP, GaAs, GaN, InAlAs, AlGaN, InAlGaAs, etc. Examples of III-N compounds include aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), and their ternary and quaternary compounds. Thus, the semiconductor material may include at least one of a group IV element or compound, a III-V or III-N compound, or a II-VI compound. Those of skill in the art understand how to select and process these materials based desired properties such as bandgaps, lattice constants, doping levels, etc.

[0062] Figure 3 shows a semiconductor diode according to a first exemplary embodiment. Figure 4 shows an example physical foundation for Figure 3, including a substrate 155, such as a silicon wafer, in which for many photonic applications such as LEDs or solar cells the surface often may have a (111) crystal orientation, although in other embodiments other orientations such as (100) are selected. The substrate 155 can be either n-doped or p-doped, depending on the configuration of the diode-based device. Other suitable substrates may include sapphire and silicon carbide.

[0063] To prepare the diode of Figure 3, a first step is to deposit a layer of dielectric material 160, such as SiO_2 or silicon nitride onto the silicon substrate 155 by chemical vapor deposition (CVD) or another deposition technique. In devices where reflection of light from the dielectric layer may create a problem, silicon nitride is generally preferable because its index of refraction is closer to that of common semiconductor materials. The thickness of the dielectric film is typically 200 to 400 nm, but it can be thicker or thinner.

[0064] A trench or trenches 165 are patterned with substantially vertical sidewalls in the layer of dielectric material 160, thereby exposing a portion of the surface of the silicon substrate 155, as shown in Figure 4. The number of trenches may be 1 or more than 1, such as 2, 3, 4, 5, 6, or even more depending upon the desired application. It is possible to pattern a trench by conventional photolithography or reactive ion etch techniques. As would be recognized by one skilled in the art based on the disclosure herein, the trench could be another shaped opening such as a hole, recess, or ring, for example. The width of the trench 165 is preferably equal to or less than the thickness of the dielectric material. This condition emerges from the requirements of Aspect Ratio Trapping: the ratio of the height of the trench 165 to the width of the trench 165 is preferably greater than or equal to 1 in order to trap substantially all threading dislocations. This technique is disclosed in earlier commonly assigned patent applications (e.g., U.S. Patent Application Serial No. 11/436,198, filed on May 17, 2006, entitled "LATTICE-MISMATCHED SEMICONDUCTOR STRUCTURES WITH REDUCED DISLOACTION DEFECT DENSITIES AND RELATED METHODS FOR DEVICE FABRICATION;" U.S. Patent Application Serial No. 12/180,254, filed on June 25, 2008, entitled "LATTICE-MISMATCHED SEMICONDUCTOR STRUCTURES WITH REDUCED DISLOCATION DEFECT DENSITIES AND RELATED METHODS FOR DEVICE FABRICATION;" ;" U.S. Patent Application Serial No. 11/436,062, filed on May 17, 2006, entitled "LATTICE-MISMATCHED SEMICONDUCTOR STRUCTURES WITH REDUCED DISLOCATION DEFECT DENSITIES AND RELATED METHODS FOR DEVICE FABRICATION;" U.S. Provisional Application Serial No. 60/842,771, filed on September 7, 2006, entitled "DEFECT REDUCTION OF SELECTIVE Ge EPITAXY IN TRENCHES ON Si(001) SUBSTRATES USING ASPECT RATIO TRAPPING;" U.S. Patent Application Serial No. 11/852,078, filed on September 7, 2007,

entitled "DEFECT REDUCTION USING ASPECT RATIO TRAPPING," which are all hereby incorporated in their entirety by reference) and in peer-reviewed journal articles (Park et al., APL 90, 052113 [2007], which is hereby incorporated in its entirety by reference).

[0065] In some cases, it may be advantageous to clean the surface of the silicon substrate 155 at the bottom of the trenches 165 by standard techniques to prepare for epitaxial growth of the bottom diode region. *See, e.g.*, (Park et al., APL 90, 052113 [2007]).

[0066] Another step is to grow the bottom diode region 170, thereby creating the structure shown in Figure 5. The material for the bottom diode region 170 depends on the device. For a solar cell, the bottom diode region 170 can be, for example, indium gallium phosphide (InGaP). For a LED, the bottom diode region 170 can be, for example, GaN, AlN, InN, or binary, ternary, or quaternary compounds comprised of these. The bottom diode region 170 can also be made from many other semiconductor materials including compound semiconductor materials such as binary, ternary, and quaternary combinations of at least one group III element chosen from Ga, In, or Al, plus at least one group V element chosen from As, P, or Sb , which have useful properties for devices such as LEDs, lasers and resonant tunneling diodes.

[0067] It is possible to dope the bottom diode region 170 *in situ* during epitaxial growth or to dope it *ex situ* by ion implantation. (As a general matter, it is generally preferable to dope the bottom diode regions, active diode regions, and top diode regions mentioned in this disclosure, and it is possible to dope them either *in situ* during epitaxial growth or *ex situ* by ion implantation.)

[0068] In Figure 5, the bottom diode region 170 has the configuration of a free-standing fin. Jinichiro Noborisaka and his colleagues at Hokkaido University have described methods of growing free-standing vertical structures such as nanowires by metal-organic vapor phase epitaxy (Noborisaka *et al.*, Appl. Phys. Lett. 86, 213102 [2005]; Noborisaka *et al.*, Appl. Phys. Lett. 87,

093109 [2005]), which are hereby incorporated by reference in their entirety. The Hokkaido group identified growth conditions in which the crystal phases which accumulate on the top of the structure grow much faster than the crystal phases which accumulate on its sides. In other words, these growth conditions favor growth perpendicular to the plane of the substrate while suppressing growth parallel to the plane of the substrate. To establish these growth conditions, the Hokkaido group adjusted variables such as the partial pressure of the gas precursors, the ratio of elements in the gas precursors, and the temperature of the substrate. These methods may be applied to grow the bottom diode region 170 in the form of a free-standing fin as shown in Figure 5. Preferably, the dielectric sidewalls of the trenches will have a {110} crystal orientation so that the subsequent epitaxial fin has {110} sidewalls, which are stable and grow slowly or not at all under the growth conditions described by Noborisaka et al.

[0069] The lower region of the fin, which is surrounded by the vertical sidewalls of the dielectric material 160, may be called the "trapping region" 175 because it traps dislocations including the threading dislocations 180. Threading dislocations originate at the interface between the fin-shaped bottom diode region 170 and the substrate 155, and they propagate upward at angles of approximately 45 degrees. Figure 5 shows the threading dislocations 180 as dashed lines. The portion of the bottom diode region 170 which lies above the trapping region 175 remains relatively free of defects. This low-defect region enables us to create high-quality compound semiconductor devices on high-quality, large-area, low-cost silicon wafers. For some materials, such as GaN, InN, AlN, or ternary or quarternary combinations of these, a dislocation density of e.g. less than or equal to $10^8/cm^2$ is low enough to be useful for device applications. For some other materials, such as GaAs and InP, a somewhat lower dislocation density is typically required to be useful for devices, e.g. less than or equal to $10^6/cm^2$.

[0070] Figure 6 shows a step to grow the active diode region 185. The detailed structure of the active diode region 185 depends on the device; for example, it can include multiple quantum wells or a single layer of moderately doped semiconductor. Before growing the active device region 185, the growth conditions may be adjusted so that the crystal phases which accumulate on the sides of the bottom diode region 170 grow at approximately the same rate as the phases which accumulate on the top of the bottom diode region 170. As a result, the active diode region 185 can grow conformally around the outside of the bottom diode region 170. Noborisaka and his colleagues have described the growth conditions (Noborisaka *et al.,* Appl. Phys. Lett. 87, 093109 [2005]).

[0071] In this embodiment and other embodiments, it is preferred that the active diode region 185 and the top diode region 190 have approximately the same lattice constants as the bottom diode region, although the lattice constants do not have to be approximately the same. As a result of having approximately the same lattice constants, few if any defects will form at the interfaces between the diode regions.

[0072] As is further shown in Figure 6, the top diode region 190 is grown. The semiconductor material for the top diode region depends on the device. The doping of the top diode region 190 will be the opposite of the doping of the bottom diode region 170; if one is p-type, the other will be n-type, and vice versa.

[0073] In Figure 6, the width of the top diode regions 190 is limited so that an opening remains between adjacent fins. This architecture is appropriate for a solar cell, where it is important to reduce or minimize the probability that the top diode region 190 will absorb the incoming light. Electron-hole pairs created in the top diode region 190 will not generate any useful electricity if they recombine before they reach the active diode region 185. The amount of

material in the top diode region 190 may be reduced or minimized by leaving free space between the fins and by making the top diode region 190 as thin as possible. In this case, the top diode region could have a thickness in the range, e.g., of 10-500 nm.

[0074] When engineering a solar cell from the architecture shown in Figure 6, efficiency can be increased by keeping the distance between adjacent active diode regions 185 smaller than the wavelength of the incident light. This strategy may prevent the incident light from entering the free space between the active regions 185 and reaching the silicon substrate 155, which can reduce the efficiency of the solar cell.

[0075] Figure 3 shows an alternate approach, in which the top diode region 195 is further grown so that it fills the entire volume between adjacent fins. With this architecture, crystalline defects known as coalescence defects can form at the intersection 197 of the growth fronts, represented by the dotted line in Figure 3. Since these defects reside far from the active region of the diode, any impairment of device performance may be reduced or minimized. When continuing to grow the top diode region 195, it can be useful to select growth conditions which favor growth parallel to the plane of the silicon substrate 155 and suppress growth perpendicular to the plane of the silicon substrate 155.

[0076] Figure 3 also shows the structure after fabricating the top electrical contact 200 and the bottom electrical contact 203 by standard techniques. Those skilled in the art understand there are many suitable materials for the electrical contacts, such as a strip of conductive metal such as copper, silver, or aluminum, or a layer of relatively transparent conductive oxide such as indium tin oxide. For LEDs, the bottom electrical contact 203 is preferably a highly reflective conductive material such as silver, which can reflect the internally created light so it will exit the LED from another surface. Those skilled in the art understand there are many ways to couple the

bottom electrical contact 203 to the bottom diode region 170 though the substrate 155 such as forming contact vias to make such an electrical connection. A single bottom electrical contact 203 may serve multiple diode elements.

[0077] One feature of the architecture shown in Figure 3, in which the top diode region 195 fills up the entire volume between adjacent fins, is that a single top diode region 195 makes physical contact (and therefore electrical contact) with active diode regions 185 in multiple other diodes. This architecture is particularly advantageous for LEDs because it can reduce or minimize the area of the top electrical contacts 200, which can block emission of the light generated within the active diode region 185. With a common top diode region 195, each diode element may not need its own top electrical contact 200; a single top electrical contact 200 can serve multiple diode elements.

[0078] The additional semiconductor material in the common top diode region 195 of Figure 3, compared with Figure 6, does not impair the performance of an LED. The top diode region 195 generally will not absorb a significant number of or any emitted photons, provided that the bandgap of the semiconductor material in the top diode region is wider than the bandgap of the semiconductor material in the active diode region.

[0079] The structures shown in both Figures 3 and 6 may offer various performance advantages compared with conventional LEDs. For example, the preferred material for fabricating a blue LED on a substrate, such as a single crystal silicon substrate, is gallium nitride. Gallium nitride, which has a wurtzite crystal structure, naturally grows with its c-plane parallel to the silicon substrate 155 and with its m-planes and a-planes normal to the silicon substrate 155. In conventional LEDs, one factor limiting internal quantum efficiency is that the polar c-plane of gallium nitride faces the semiconductor diode. The structures shown in Figures 3 and 6 may

deliver higher internal quantum efficiency because non-polar m-planes or a-planes of gallium nitride face the diode. In one preferred LED structure, the bottom diode region 170, active diode region 185, and top diode region 195 are made from gallium nitride and indium gallium nitride, m-plane or a-plane crystal surfaces of gallium nitride form the interface between the bottom diode region 170 and the active diode region 185, and m-plane or a-plane crystal surfaces of gallium nitride form the interface between the active diode 185 region and the top diode region 195.

[0080] Further, structures shown in both Figures 3 and 6 can also be used for LEDs based on cubic materials such as GaAs and AlGaAs.

[0081] The following are examples of process parameters to form the bottom, active, and top diode regions according to embodiments in this disclosure. First, a substrate and a patterned dielectric layer as known in the art are provided. Process parameters for bottom, active, and top diode regions, of a GaAs and AlGaAs-based LED, according to the first embodiment are as follows.

[0082] In this example, the bottom diode region can be a pillar or fin (central pillar or fin) of GaAs having height dimensions greater than width or radial dimensions (e.g., 1 micron in height and 100 nm in width). Growth conditions (e.g., CVD) include i) pressure: 0.1 atm ii) precursors: TMG (Trimethylgallium) and 20% AsH_3 (Arsine), diluted in H_2, iii) temperature: 750C and iv) dopant: n-type. To make the bottom diode region N-type, one dopant is silicon. To highly enhance vertical growth, the partial pressure of AsH_3 may be relatively low for this step, compared to what would normally be used for GaAs growth as understood by those well versed in the art. For example, the partial pressure of AsH_3 could be 5-10X lower than normal. Because this is a reactor-dependent value, no absolute value is given here.

[0083] Further in this example, the active diode region can include a plurality of layers being a first confinement layer, a quantum well layer and a second confinement layer at the bottom diode layer.

[0084] Growth conditions for an AlGaAs layer for carrier confinement (e.g., 15 nm thick) include i) pressure: 0.1 atm, ii) precursors: TMG, TMA (Trimethylaluminium), and 20% arsine, diluted in H_2, iii) temperature: 850C and iv) dopant: N-type dopant is silicon.

[0085] Growth conditions for a GaAs quantum well layer for emission (e.g.,10 nm thick) include i) pressure: 0.1 atm, ii) precursors: TMG and 20% arsine, diluted in H_2, iii) temperature: 720C and iv) dopant: no doping.

[0086] Growth conditions for an AlGaAs layer for carrier confinement (e.g., 15 nm thick) include i) pressure: 0.1 atm, ii) precursors: TMG, TMA (Trimethylaluminium), and 20% arsine, diluted in H_2, iii) temperature: 850C and iv) dopant: P-type dopant with zinc.

[0087] Continuing in this example, the top diode region is at or on the active diode layer (e.g., 0.5 micron thick). Growth conditions for a layer of GaAs include i) pressure: 0.1 atm, ii) precursors: TMG and 20% arsine, diluted in H_2, iii) temperature: 720C and iv) dopant: P-type dopant is zinc.

[0088] The embodiment shown in Figure 3 can comprise a semiconductor diode made from compound semiconductors or other lattice mismatched materials on a silicon substrate and may comprise a silicon substrate 155; a layer of dielectric material 160 covering the silicon substrate 155, the layer of dielectric material 160 containing a trench 165, which exposes the surface of the silicon substrate 155, the trench having substantially vertical sidewalls, and the ratio of the height of the trench to the width of the trench being greater to or equal to 1; a bottom diode region 170

of semiconductor material filling the trench and extending upward in the shape of a fin; a trapping region 175 in the lowest segment of the bottom diode region 170 wherein threading dislocations 180 intersect the sidewalls of the dielectric material 160 and terminate (e.g., at a reduced defect area); an active diode region 185 of semiconductor material grown conformally around the bottom diode region 170; a top diode region 195 of semiconductor material grown conformally around the active diode region; a top electrical contact 200; and a bottom electrical contact 203.

[0089] Figure 7 summarizes a method of fabricating the semiconductor diode shown in Figure 3 - specifically, a method of fabricating a diode made from compound semiconductors or other lattice mismatched materials on a silicon substrate comprising the following steps. Step 900 includes depositing a layer of dielectric material, such as dielectric material 160, onto the surface of a silicon substrate, such as silicon substrate 155. Step 905 includes patterning a trench in the layer of dielectric material, such as trench 165 in dielectric material 160, to expose the surface of the silicon substrate, the trench having substantially vertical sidewalls, and the ratio of the height to the width of the trench being greater than or equal to 1. Step 910 includes selecting growth conditions which favor growth perpendicular to the plane of the silicon substrate and suppress growth parallel to the plane of the silicon substrate. Step 915 includes growing a semiconductor material to form a bottom diode region, such as bottom diode region 170, which fills the trench and extends upward in the shape of a fin. Step 920 includes selecting growth conditions so that the semiconductor material for the active diode region, such as active diode region 185, will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region. Step 925 includes growing a semiconductor material conformally around the top of the bottom diode region and the sides of the bottom diode region to

create an active diode region, such as active diode region 185. Step 930 includes growing a semiconductor material conformally around the top of the active diode region and the sides of the active diode region to create a top diode region, such as top diode region 195. Step 935 includes fabricating a top electrical contact, such as top electrical contact 200, on the surface of the top diode region. Step 940 includes fabricating a bottom electrical contact, such as bottom electrical contact 203, on the bottom of the silicon substrate.

[0090] In another embodiment shown in Figure 8, step 950 includes continuing to grow the top diode region so that the top diode regions from adjacent diodes merge, thereby creating a single top diode region which connects together multiple diodes.

[0091] In a further alternative embodiment, a method takes into consideration the fact that the technique for growing free-standing vertical structures as described by Noborisaka and his colleagues may not work under all conditions. For example, it will not generally be possible to grow free-standing vertical structures if the silicon substrate has a (100) crystal surface.

[0092] This method begins with an appropriately doped silicon substrate 155, as shown in Figure 9. A first layer of dielectric material 210 is grown on the surface of the silicon substrate 155. In some embodiments, the preferred material for the first dielectric layer 210 is silicon nitride. This first dielectric layer 210 should be thick enough to trap defects after creating trenches in it; e.g., the thickness of the first dielectric layer 210 should be equal to or greater than the width of the trenches.

[0093] A second dielectric layer 215 is grown on top of the first dielectric layer 210. In some embodiments, the preferred material for this second dielectric layer is silicon dioxide (SiO_2).

[0094] Trenches 220 are patterned with substantially vertical sidewalls through both dielectric layers 210 and 215, exposing a portion of the surface of the silicon substrate 155. An optional step is to clean the surface of the silicon substrate 155 at the bottom of the trenches 220, such as by the cleaning method described above.

[0095] The bottom diode region 170 is grown by filling the trenches with a semiconductor material, as shown in Figure 10. Because there is a lattice mismatch between silicon the bottom diode region semiconductor material, misfit dislocations may form at the interface between the silicon substrate 155 and the bottom diode region 170. Threading dislocations 180 may propagate upward at an angle, intersect the sidewalls of the first dielectric layer 210, and terminate within the trapping region 175. The segment of the bottom diode region 170 above the trapping region 175 may be relatively free of defects and suitable for high-performance devices. In this way, compound semiconductor devices on silicon substrates can be created.

[0096] The second dielectric layer 215 is removed with a process such as a wet etch with hydrofluoric acid and water. This process will selectively remove the second (SiO_2) dielectric layer 215 without attacking either the first (SiN_x) dielectric layer 210 or any of the semiconductor materials that may comprise the bottom diode region 225. The resultant structure appears in Figure 5. Thus, this method describes a different way to fabricate the bottom diode region configured in the shape of a fin.

[0097] This method continues as described above and illustrated in Figures 3 and 6: deposit the active diode region 185, the top diode region 190, and the top and bottom electrical contacts 200 and 203.

[0098] Figure 11 summarizes this alternative method that is depicted, at least partially by Figures 9 and 10, which comprises the following steps. Step 1000 includes depositing a first

layer of dielectric material, such as first dielectric layer 210, onto the surface of a silicon substrate, such as silicon substrate 155. Step 1005 includes depositing a second layer of dielectric material, such as second dielectric layer 215, onto the surface of the first layer of dielectric material, the second layer of dielectric material having different characteristics than the first layer of dielectric material. Step 1010 includes patterning a trench, such as trench 220, through both the first layer of dielectric material and the second layer of dielectric material to expose the surface of the silicon substrate, the trench having substantially, vertical sidewalls, the ratio of the height of the trench to the width of the trench being equal to or greater than 1 (e.g., in the first layer of dielectric material). Step 1015 includes growing a semiconductor material into the trench to form a bottom diode region, such as bottom diode region 170. Step 1020 includes selectively removing the remaining portions of the second layer of dielectric material. Step 1025 includes growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region, such as active diode region 185. Step 1030 includes growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 195. Step 1035 includes fabricating a top electrical contact, such as top electrical contact 200, on the surface of the top diode region. Step 1040 includes fabricating a bottom electrical contact, such as bottom electrical contact 203 on the bottom of the silicon substrate.

[0099] Figure 12 shows another embodiment in which the semiconductor diode is configured as a column, rather than as a fin. A layer of dielectric material 160, such as SiO_2 or SiN_x, is grown onto the surface of an appropriately doped silicon substrate 155.

[0100] A hole 250 is patterned with substantially vertical sidewalls in the dielectric material 160 by standard photolithographic or etch techniques. To enable the hole 250 to trap substantially

all threading dislocations, the ratio of the depth of the hole 250 to the diameter of the hole 250 is preferably equal to or greater than 1. The hole exposes the surface of the silicon substrate 155.

[0101] Growth conditions (such as the pressure and the composition of the precursor gases and the temperature of the substrate) are selected that favor growth perpendicular to the plane of the silicon substrate 155 and suppress growth parallel to the plane of the silicon substrate 155, as described in the Noborisaka paper cited above. An appropriately doped semiconductor material is grown that fills the holes and forms free-standing columns above the holes to create the bottom diode region 260, as shown in Figure 13.

[0102] Again, because there is a lattice mismatch between silicon the semiconductor diode material, misfit dislocations may occur at the interface between the bottom diode region 260 and the silicon substrate 155. Threading dislocations may propagate upward from the interface and intersect the curved sidewalls of hole in the dielectric layer 160 and terminate. The trapping region in which the threading dislocations originate and terminate may remain substantially within the hole 250 in the dielectric layer and therefore may not be visible in Figure 13. The entire portion of the bottom diode region 260 visible in Figure 13 exists above the trapping region. This upper portion of the bottom diode region 260 may be relatively free of crystalline defects and suitable for creating high-performance devices.

[0103] (For the special case in which the bottom diode region 260 is a column with very small diameter, well below 100 manometers, the semiconductor material in the bottom diode region 260 can undergo complete elastic relaxation without the formation of any lattice mismatch defects. In this case, there may be no threading dislocations for the sidewalls of the dielectric layer to trap, and the diode may not contain a "trapping region.")

[0104] The growth conditions are adjusted so that the material or materials for the active diode region 265 will grow at approximately equal rates on the top and on the sides of the bottom diode region 260. Semiconductor material is conformally grown on the top and the sides of the bottom diode region 260 to create the active diode region 265 shown in Figure 14.

[0105] Semiconductor material is conformally grown on the top and sides of the active diode region 265 to create the top diode region 270, as shown in Figure 15. It may be possible to grow either a discontinuous top diode region 270, so that the semiconductor diodes have the configuration of free-standing columns as shown in Figure 15, or a continuous top diode region 275 as shown in Figure 16.

[0106] The top electrical contact 280 is grown on the exposed surface of the top diode region 275, and the bottom electrical contact 285 is grown below the silicon substrate 155, as shown in Figure 16.

[0107] The diode shown in Figure 16 can comprise a silicon substrate 155; a dielectric layer 160 containing a hole 250 which exposes the surface of the silicon substrate, the hole 250 having substantially vertical sidewalls, the ratio of the depth of the hole 250 to the diameter of the hole 250 being greater than 1; a bottom diode region 260 of semiconductor material filling the hole and extending upward in the shape of a column; a trapping region in the lowest segment of the bottom diode region 260 wherein threading dislocations intersect the curved sidewalls of the hole 250 in the dielectric material 160 and terminate; an active diode region 265 of semiconductor material grown conformally around the bottom diode region 260; a top diode region 275 grown conformally around the active diode region 265; a top electrical contact 280; and a bottom electrical contact 285.

[0108] The following methods are two exemplary methods of fabricating the embodiment shown in Figure 16.

[0109] Figure 17 summarizes one method, which comprises the following steps. Step 1100 includes depositing a layer of dielectric material, such as dielectric material 160 onto the surface of a silicon substrate, such as silicon substrate 155. Step 1105 includes patterning a hole, such as hole 250, in the layer of dielectric material to expose the surface of the silicon substrate, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole being greater than or equal to one. Step 1110 includes selecting growth conditions which favor growth perpendicular to the plane of the silicon substrate and suppress growth parallel to the plane of the silicon substrate. Step 1115 includes growing a semiconductor material to form a bottom diode region, such as bottom diode region 260, which fills the hole and extends upwards in the shape of a column. Step 1120 includes selecting growth conditions so that the semiconductor material for the active diode region, such as active diode region 265, will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region. Step 1125 includes growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region. Step 1130 includes growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 275. Step 1135 includes fabricating a top electrical contact, such as top electrical contact 280, on the surface of the top diode region. Step 1140 includes fabricating a bottom electrical contact, such as bottom electrical contact 285, on the bottom of the silicon substrate.

[0110] Another method does not depend on the ability to grow a free-standing bottom diode region in the shape of a column. It begins with an appropriately doped silicon substrate 155, as

shown in Figure 18. A first dielectric layer 210, such as SiNx, is grown on the surface of the silicon substrate 155.

[0111] A second dielectric layer 215 is grown on top of the first dielectric layer 210. In some embodiments, the preferred material for this second dielectric layer 215 is silicon dioxide SiO2.

[0112] A hole 300 is patterned with substantially vertical sidewalls through both dielectric layers 210 and 215, exposing the surface of the silicon substrate 155. It is possible to pattern the hole 300 by various techniques such as standard photolithography or reactive ion etch processes.

[0113] The thickness of the first dielectric layer 210 may be greater than or equal to than the diameter of the hole 300. Under these conditions, the curved sidewalls of the first dielectric layer 210 may trap substantially all of the threading dislocations.

[0114] The surface of the silicon substrate 155 at the bottom of the hole 300 may be cleaned by the cleaning method referred to earlier.

[0115] The bottom diode region 260 is grown by filling the hole 300 with a semiconductor material, as shown in Figure 19.

[0116] Misfit dislocations may form at the interface between the silicon substrate 155 and the bottom diode region 260. Threading dislocations may propagate upward and intersect the sidewalls of the first dielectric layer 210, and may terminate within trapping regions, which reside at the bottom of the filled holes 300 and therefore are not visible in Figure 19. The segment of the bottom diode region 310 above the trapping region may be relatively free of defects and therefore suitable for high-performance devices.

[0117] The remaining portions of the second dielectric layer 215 (e.g., the SiO2 layer) are removed by means of a wet etch with hydrofluoric acid and water. This process may selectively remove the second (e.g., SiO2) dielectric layer 215 without attacking either the first (e.g., SiNx) dielectric layer 210 or any of the semiconductor materials that may comprise the bottom diode region 260.

[0118] The resultant structure appears in Figure 13. The process then continues as described in the method described above with respect to Figures 14 through 16: deposit the active diode region 265 as shown in Figure 14, the top diode region 270 or 275 as shown in Figure 15 or Figure 16, and the top electrical contacts 280 and bottom electrical contacts 285 as shown in Figure 16.

[0119] Figure 20 summarizes the above described method, which comprises the following steps. Step 1200 includes depositing a first layer of dielectric material, such as first dielectric layer 210, onto the surface of a silicon substrate, such as silicon substrate 155. Step 1205 includes depositing a second layer of dielectric material, such as second dielectric layer 215, onto the surface of the first dielectric layer. Step 1210 includes patterning a hole, such as hole 300, in both the first layer of dielectric material and the second layer of dielectric material to expose the surface of the silicon substrate, the hole having substantially vertical sidewalls, the ratio of the depth of the hole to the diameter of the hole (300) being greater than or equal to 1. Step 1215 includes growing a semiconductor material into the hole to form a bottom diode region, such as bottom diode region 260. Step 1220 includes selectively removing the remaining portions of the second layer of dielectric material. Step 1225 includes growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region, such as active diode region 265. Step 1230 includes growing a semiconductor material

conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 270 or 275. Step 1235 includes fabricating a top electrical contact, such as top electrical contact 280, on the surface of the top diode region. Step 1240 includes fabricating a bottom electrical contact, such as bottom electrical contact 285, on the bottom of the silicon substrate.

[0120] Some semiconductor materials demonstrate unique behavior when deposited into the round holes 250 and subsequently grow free-standing bottom diode regions 260. Specifically, the free-standing columns can grow out of the round holes to form hexagonal columns; e.g., the columns (element 260 in Figure 13, element 265 in Figure 14, and element 270 in Figure 15) have hexagonal cross sections rather than round cross-sections. Reference is made to a semiconductor diode like in Figures 12 through 16, except with columns that have hexagonal cross sections, as discussed.

[0121] The hexagonal columns may be advantageously used to increase the packing density of the semiconductor diodes by configuring them in a hexagonal array rather than a square array. Figure 21 shows several semiconductor diodes, of which only the top diode regions 270 are visible, arranged in a hexagonal array rather than a square array. (Note that in Figure 21, the columns have a circular cross section rather than a hexagonal cross section). A hexagonal array of holes 250 is created in the dielectric material 160 rather than a square array.

[0122] Figure 22, a top view of the hexagonal array, shows the dense packing of semiconductor diodes which a hexagonal array allows. The hexagonal features in Figure 22 are the tops of the top diode regions 270 with hexagonal cross sections. The regions between the hexagonal features are the exposed portions of the dielectric material 160. Another embodiment

comprises a plurality of diodes such as those described in above, arranged in a hexagonal array with other diodes that also have hexagonal cross sections in order to achieve dense packing.

[0123] The diode structure shown in Figure 3 is suitable for LEDs and other photonic devices. However, in multi-junction solar cells, reflection of light from the dielectric layer 160 may reduce conversion efficiency. Suppose, for example, the silicon substrate 155 contains a p-n junction intended to capture relatively low-energy photons. These relatively low-energy photons would strike the top of the structure, transmit through the top diode region 195 and (depending on their path) perhaps also transmit through the active diode region 185 and the bottom diode region 170, then strike the dielectric layer 160. Some percentage of these photons would reflect from the dielectric layer 160, transmit through the other layers 170, 185, and 195, and exit through the top surface of the device. The solar cell would not absorb them, and they would be lost to the process.

[0124] Figure 25 illustrates one exemplary device architecture. This structure can provide a dielectric layer with a reduced thickness (e.g., less than 20 nanometers)—thin enough to transmit the photons rather than reflecting them. To build this structure, the silicon substrate 155 shown in Figure 23 is provided. If a multi junction solar cell in which the silicon layer contains one of the junctions were being built, the silicon substrate 155 would be doped appropriately. A dielectric layer 350 is grown on the silicon substrate 155 thin enough (less than 20 nanometers) to transmit substantially all of the incident light. Trenches 355 are patterned in the dielectric layer.

[0125] The deposition conditions are adjusted in the reactor to favor vertical growth and to suppress horizontal growth, as described above. The bottom diode region 365 is grown in the shape of a free-standing fin, as shown in Figure 24.

[0126] The deposition conditions are adjusted in the reactor so that vertical growth and horizontal growth occur at approximately the same rates. A semiconductor material is conformally grown around the top and sides of the bottom diode region 365 to create the active diode region 380, as shown in Figure 25.

[0127] Since the dielectric layer is so thin, the aspect ratio of the trenches (the ratio of height to width) 355 is less than 1. As a result, the sidewalls of the dielectric layer 350 may not be able to trap substantially all of the threading dislocations 375. The threading dislocations 375 may continue to propagate into the active diode region 380. Note that electron-hole pairs can recombine when they contact the threading dislocations 375 and reduce the efficiency of the solar cell. However, the structure mitigates this effect because the photons will pass through what a primary light absorption region 390, which resides in the upper portion of the diode, before they can reach the threading dislocations 375. The primary light absorption region 390 may absorb most of the photons because it is relatively large compared with the region occupied by the threading dislocations 375. Recombination of electron-hole pairs at the threading dislocations 375 may therefore be a secondary effect and not significantly reduce solar cell efficiency.

[0128] A semiconductor material is conformally grown around the top and sides of the active diode region 380 to create the top diode region 395. Again, coalescence defects 400 may appear in the top diode region 395 where the growth fronts from adjacent fins merge.

[0129] A top electrical contact 410 is grown onto the top surface of the top diode region 395 and a bottom electrical contact 415 is grown onto the bottom of the silicon substrate 155. In a solar cell, the influence of the coalescence defects 400 can be mitigated by covering them with the top electrical contact 410.

[0130] The embodiment shown in Figure 25 is a diode made from compound semiconductors or other lattice mismatched semiconductors on a silicon substrate and can comprise a silicon substrate 155; a layer of dielectric material 350 covering the silicon substrate, the layer of dielectric material containing a trench 355 exposing the surface of the silicon substrate 155, the layer of dielectric material 350 having a thickness of less than 20 nanometers; a bottom diode region 365 of semiconductor material filling the trench 355 and extending upward in the shape of a fin; an active diode region 380 of semiconductor material grown conformally around the bottom diode region 365; a top diode region 395 of semiconductor material grown conformally around the active diode region 380; a top electrical contact 410; and a bottom electrical contact 415.

[0131] Figure 26 illustrates a method of fabricating the embodiment depicted in Figure 5. The method comprises the following steps. Step 1300 includes depositing a layer of dielectric material, such as dielectric material 350, with thickness less than or equal to 20 nanometers onto the surface of a silicon substrate, such as silicon substrate 155. Step 1305 includes patterning a trench, such as trench 355, in the layer of dielectric material to expose the surface of the silicon substrate, the trench having substantially vertical sidewalls. Step 1310 includes selecting growth conditions which favor growth perpendicular to the plane of the silicon substrate and suppress growth parallel to the plane of the silicon substrate. Step 1315 includes growing a semiconductor material to form a bottom diode region, such as bottom diode region 365, which fills the trench and extends upward in the shape of a fin. Step 1320 includes selecting growth conditions so that the semiconductor material for the active diode region, such as active diode region 380, will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region. Step 1325 includes growing a semiconductor material

conformally around the top and sides of the bottom diode region to create an active diode region. Step 1330 includes growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 395. Step 1335 includes fabricating a top electrical contact, such as top electrical contact 410, on the surface of the top diode region. Step 1340 includes fabricating a bottom electrical contact, such as bottom electrical contact 415, on the bottom of the silicon substrate.

[0132] In some applications, the presence of the silicon substrate can degrade the performance of the device. For example, for light-emitting diodes emitting in certain wavelength ranges, the silicon may absorb the light. An exemplary device architecture that can remove the silicon substrate is shown in Figure 28. Steps in the process of making such a device are the steps that lead up to fabrication of the structure in Figure 3 as shown in Figure 27, which is simply the structure in Figure 3 inverted, before application of the electrical contacts 200 and 203.

[0133] A "handle" substrate or surface 430 is bonded to the top diode region 195, as shown in Figure 28. The handle substrate 430 could be part of an LED packaging fixture. It may be necessary to planarize the surface of the top diode region 190, 195 by some suitable technique such as, for example, chemical mechanical planarization in order to bond the handle substrate 430 to it securely.

[0134] The handle substrate 430 may be electrically conductive, or it may contain conductor elements which will serve as contacts for the top diode region 195. Bonding methods are well known in the art, including methods used in flip-chip bonding where the "top" portion of an LED is bonded to a surface that is part of an LED package.

[0135] The initial silicon substrate 155 is removed by one or more methods such as grinding, etching with a chemical such as tetramethyl ammonium hydroxide, or laser ablation, all of which are well known to those skilled in the art.

[0136] As shown in Figure 28, top electrical contacts 435 and bottom electrical contacts 440 are added by standard techniques. As explained above, the bottom electrical contacts 440 may also reside within the handle substrate 430.

[0137] It may be useful to select reflective materials for the contacts 435 and 440 in order to induce light to exit the LED in the most favorable direction.

[0138] The embodiment shown in Figure 28 is a diode made from compound semiconductors or other lattice mismatched semiconductor materials and can comprise a layer of dielectric material 160 containing a trench 165, the trench having substantially vertical sidewalls, and the ratio of the height of the trench to the width of the trench being greater to or equal to 1; a fin-shaped bottom diode region 170 of semiconductor material filling the trench; a trapping region 175 within the bottom diode region 170 wherein threading dislocations 180 intersect the sidewalls of the trench 160 and terminate; an active diode region 185 of semiconductor material grown conformally around the bottom diode region 170; a top diode region 195 of semiconductor material grown conformally around the active diode region; a handle substrate 430; a top electrical contact 435; and a bottom electrical contact 440.

[0139] Figure 29 illustrates a method of fabricating the embodiment of Figure 28. The method comprises the following steps. Step 1400 includes depositing a layer of dielectric material, such as dielectric material 160, onto the surface of a silicon substrate, such as silicon substrate 155. Step 1405 includes patterning a trench, such as trench 165, in the layer of dielectric material to expose the surface of the silicon, the trench having substantially vertical

sidewalls, and the ratio of the height of the trench to the width of the trench being greater than or equal to 1. Step 1410 includes selecting growth conditions which favor growth perpendicular to the plane of the silicon substrate and suppress growth parallel to the plane of the silicon substrate. Step 1415 includes growing a semiconductor material to form a bottom diode region, such as bottom diode region 170, which fills the trench and extends upward in the shape of a fin. Step 1420 includes selecting growth conditions so that the semiconductor material for the active diode region, such as active diode region 185, will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region. Step 1425 includes growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region. Step 1430 includes growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 190. Step 1435 includes bonding a handle substrate, such as handle substrate 430, to the surface of the top diode region. Step 1440 includes removing the silicon substrate by a chemical or mechanical process. Step 1445 includes fabricating a top electrical contact, such as top electrical contact 435, on the exposed surface of the dielectric layer. Step 1450 includes fabricating a bottom electrical contact, such as bottom electrical contact 440, on the exposed surface of the handle substrate.

[0140] One example of an alternate method of creating the embodiment of Figure 28 is to create the fin-shaped structure shown in Figure 9 by the process described in Figure 11 rather than the process described in Figure 7.

[0141] An alternative way to reduce or minimize absorption of light by the silicon substrate is to incorporate a reflector above the silicon substrate. The embodiment shown in Figure 32

illustrates one way to do this using a diode with a reflector that also serves as the top electrical contact.

[0142] To build this structure, a substrate 500 made from a material such as (111)-surface silicon, doped either p-type or n-type, depending on the configuration of the diode device, is provided, as shown in Figure 30. A first layer of dielectric material 510, such as silicon nitride, a layer of a refractory metal 520, such as tungsten, and a second layer of dielectric material 530 are deposited or grown. A refractory layer/material or refractory metal 520, such as tungsten, is chosen because this layer 520 may withstand the growth temperature of the subsequent layers without melting.

[0143] A trench is patterned in the structure by photolithography and/or reactive ion etch.

[0144] Dielectric spacers 550 are created on the sidewalls of the trench by conventional methods. In the spacer process, all exposed surfaces (sidewalls of the second layer of dielectric material 530, the refractory metal 520, and the first layer of dielectric material 510, and the exposed surface of the silicon substrate 500 at the bottom of the trench) are conformally coated with a layer of dielectric material, such as SiO2. The dielectric material is subjected to a brief anisotropic reactive ion etch, which selectively removes all the SiO2 coating horizontal surfaces but leaves intact the SiO2 coating vertical surfaces. This process yields dielectric spacers 550. It leaves no metal exposed.

[0145] Optionally, the exposed surface of the silicon substrate 500 at the bottom of the trench may be cleaned by methods described above.

[0146] Growth conditions which favor growth perpendicular to the plane of the silicon substrate 500 and suppress growth parallel to the plane of the silicon substrate 500 are selected,

as described in the paper by Noborisaka and his colleagues cited above. A semiconductor material is grown to form a free-standing bottom diode region 570 which fills the trench and extends upward in the shape of a fin. The growth of the semiconductor material may be performed using MOCVD. The process window (e.g., the conditions of temperature and pressure) for this growth step may be narrow because the semiconductor material for the bottom diode region cannot be allowed to nucleate on either the dielectric spacers 550 or the second dielectric layer 530.

[0147] Threading dislocations 560 may propagate upward, e.g., at a 45 degree angle from the interface between the bottom diode region 570 and the silicon substrate 500, intersect the dielectric spacers 550, and terminate within a trapping region 555. In order to trap substantially all of the threading dislocations, it is preferred that the aspect ratio of the trapping region (the ratio of the height of the dielectric spacers 550 to the width of the trench between the spacers 550) be greater than or equal to 1.

[0148] Growth conditions are selected so that the semiconductor material for the active diode region 580 will grow at approximately equal rates on the side of the fin and on the top of the fin. A semiconductor material is conformally grown around the top and sides of the bottom diode region to create an active diode region 580.

[0149] The sample is removed from the reactor, such as a MOCVD reactor if MOCVD is used, and the second layer of dielectric material 530 is removed from the structure by a wet selective etch. For example, if the dielectric material is silicon nitride, then hot phosphoric acid can be a good etchant.

[0150] The structure is returned to the reactor. Growth conditions are selected so that the semiconductor material for the top diode region 590, as shown in Figure 31, will not only grow

at approximately equal rates on the top and the sides of the bottom diode region, but also coat the surface of the refractory metal 520. The top diode region 590 is created by growing a semiconductor material to provide a conformal coating around the top and sides of the active diode region 580. (It is not necessary to continue growing the top diode region 590 so that the top diode regions from adjacent diodes merge as in Figure 3, because the layer of refractory metal 520 will serve as an electrical contact to the top diode region 590.) Simultaneously, a horizontal layer of semiconductor material 595 is created that coats the surface of the refractory metal 520.

[0151] Optionally, it can be advantageous to cover the top diode region 590 and the horizontal layer of semiconductor material 595 with a third layer of dielectric material 600 such as silicon dioxide.

[0152] Standard techniques are employed to create a via 605 through the third layer of dielectric material 600 and through the horizontal layer of semiconductor material 595, as shown in Figure 31. For best results, the via 605 may be relatively far from the diode elements 570, 580, 590.

[0153] Finally, the via 605 is filled by depositing a suitable material 620, such as a plug of tungsten or another suitable material such as would be known in the art, terminating in the top electrical contact 630, as shown in Figure 32. The bottom electrical contact 640 is also created.

[0154] In the illustrated embodiment of the structure shown in Figure 32 as a light-emitting diode, the refractory metal layer 520 may serve not only as a top electrical contact but also as a reflector. Some of the light generated within the diode may propagate downward, toward the silicon substrate 500. A high percentage of that light will strike the refractory metal layer 520. For example, tungsten, when used for refractory metal layer 520, may reflect virtually all that

light upward. The reflected light may exit the structure and contribute to the brightness of the LED. Only a small percentage of the light generated within the diode may pass through the trapping region 555 into the silicon substrate 500, where it may be absorbed and lost to the process.

[0155] One example of an alternative to the embodiment illustrated in Figure 32 is to pattern a hole in place of the first trench and grow the diodes in the shape of columns rather than fins.

[0156] The embodiment shown in Figure 32 is a diode made from compound semiconductors or other lattice mismatched semiconductor materials and can comprise a silicon substrate 500; a layer of dielectric material 510 covering the silicon substrate 155; a layer of refractory metal 520 covering the dielectric layer; a horizontal layer of semiconductor material 595 covering the layer of refractory metal 520; a first trench opening through the layer of semiconductor material 595, through the layer of refractory material 520, and through the layer of dielectric material 510 and thereby exposing the surface of the silicon substrate 500, the first trench having substantially vertical sidewalls, and the ratio of the height of the first trench to the width of the first trench being greater than or equal to 1; dielectric spacers 550 covering the sidewalls of the first trench; a bottom diode region 570 of semiconductor material filling the first trench and extending upward in the shape of a fin; a trapping region 555 in the lowest segment of the bottom diode region 570 wherein threading dislocations 560 intersect the dielectric spacers 550 and terminate; an active diode region 580 of semiconductor material grown conformally around the bottom diode region 570; a top diode region 590 of semiconductor material grown conformally around the active diode region 580 and contacting the horizontal layer of semiconductor material 595; a thick layer of dielectric material 600 covering the top diode region 590 and the horizontal layer of semiconductor material 595; a second trench opening through the

thick layer of dielectric material 600 and through the horizontal layer of semiconductor material, thereby exposing the surface of the layer of refractory metal 520; a metal plug or conductor 620 filling the second trench and physically contacting the layer of refractory metal 520; a top electrical contact 630 physically contacting the metal plug 620; and a bottom electrical contact 640 physically contacting the silicon substrate 640.

[0157] Figure 33 illustrates a method of fabricating the embodiment illustrated in Figure 32. The method comprises the following steps. Step 1500 includes depositing a first layer of dielectric material, such as dielectric material 510, onto the surface of a silicon substrate, such as silicon substrate 500. Step 1505 includes depositing a layer of refractory metal, such as refractory metal 520, onto the first layer of dielectric material. Step 1510 includes depositing a second layer of dielectric material, such as dielectric material 530, onto the layer of refractory metal. Step 1515 includes patterning a first trench through the second layer of dielectric material, through the layer of refractory metal, and through the first layer of dielectric material, to expose the surface of the silicon substrate, this first trench having substantially vertical sidewalls, and the ratio of height to width of this first trench being greater than or equal to 1. Step 1520 includes coating all exposed surfaces (the second layer of dielectric material, the sidewalls of the first trench, and the surface of the silicon substrate at the bottom of the first trench) with a third layer of dielectric material. Step 1525 includes etching away the horizontal surfaces of the third layer of dielectric material, thereby leaving dielectric spacers, such as spacers 550, on the sidewalls of the first trench. Step 1530 includes selecting growth conditions which i) favor growth perpendicular to the plane of the silicon substrate, ii) suppress growth parallel to the plane of the silicon substrate and iii) do not permit semiconductor material to nucleate on either the first layer of dielectric material or the dielectric spacers. Step 1535

includes growing a semiconductor material to form a bottom diode region, such as bottom diode region 570, which fills the first trench and extends upward in the shape of a fin. Step 1540 includes removing the second layer of dielectric material by a selective wet etch. Step 1545 includes selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region. Step 1550 includes growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region, such as active diode region 580. Step 1555 includes selecting growth conditions so that the semiconductor material for the top diode region, such as top diode region 590, will i) grow at approximately equal rates on the top of the active diode region and on the sides of the active diode region, and also ii) coat the surface of the refractory metal. Step 1560 includes growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, while simultaneously growing a horizontal layer of semiconductor material, such as horizontal layer of semiconductor material 595, which coats the surface of the refractory metal. Step 1565 includes coating the top diode region and the horizontal layer of semiconductor material with a third layer of dielectric material, such as dielectric material 600. Step 1570 includes creating a via, such as via 605, through the third layer of dielectric material and through the horizontal layer of semiconductor material. Step 1575 includes filling the via by depositing a plug of metal, such as metal plug or conductor 620, which contacts the layer of refractory metal and terminates in a top electrical contact, such as top electrical contact 630. Step 1580 includes growing a bottom electrical contact, such as bottom electrical contact 640, on the bottom of the silicon substrate.

[0158] Figure 35 illustrates a further embodiment intended primarily, but not necessarily, for light-emitting diodes, which takes advantage of the fact that when gallium nitride grows out of a hole or a trench in a dielectric layer, it naturally grows in the shape of a six-sided pyramid as a result of crystal faceting. To create this embodiment, a silicon substrate 700 is provided, as shown in Figure 34. A layer of dielectric material 710 is deposited. A hole 720 is created in the dielectric material by a lithography process and/or an etch process, thereby exposing a portion of the surface of the silicon substrate. As an option, the surface of the silicon substrate 700 at the bottom of the hole may be cleaned by the process cited earlier.

[0159] A semiconductor material is grown to create the bottom diode region 730, as shown in Figure 35. (In this embodiment, all the semiconductor materials may be III-nitride materials, such as gallium nitride.) The semiconductor material for the bottom diode region 730 fills the hole 720 and naturally grows upward out of the hole in the form of a six-sided pyramid.

[0160] As in other embodiments, the ratio of the depth to the hole 720 to the diameter of the hole 720 is preferably greater than or equal to 1 in order for the structure to be able to trap threading dislocations. Threading dislocations 740 may form at the interface between the bottom diode region 730 and the silicon substrate 700. These threading dislocations may propagate upward at an angle, intersect the sidewalls of the dielectric layer 710, and terminate within the trapping region 750, such that there may be relatively defect-free gallium nitride in the upper portion of the bottom diode region 730.

[0161] A semiconductor material is conformally grown around the pyramidal bottom diode region 730 to form the active diode region 760.

[0162] A semiconductor material is conformally grown around the pyramidal active diode region 760 to create the top diode region 770. As an option, it may be possible to grow the

semiconductor material for the top diode region 770 in such a way that the top diode regions 770 on adjacent diodes merge. The advantage of this strategy may be that a single strip of metal serving as a top electrical contact 780 provides current for multiple diodes because current can flow through the top diode region 770 from one diode to the next.

[0163] Finally, top electrical contact 780 and a bottom electrical contact 790 are created. The top electrical contact 780 can be, for example, a strip of metal or a film of transparent conductor such as indium tin oxide. It may be useful to reduce or minimize the area devoted to the top electrical contact 780 because the top electrical contact 780 blocks the light emitted by the device. Even a "transparent" contact typically will not be 100% transmissive.

[0164] The structure shown in Figure 35 offers various advantages. It can be simpler to grow than the other embodiments described in this disclosure because the gallium nitride naturally grows in six-sided pyramids. The surface area of the p-n diode is larger than the surface area of the silicon substrate 700. This advantage is important because it increases the photon output per unit surface area of the footprint of the device. The bottom diode region is not constrained to be a narrow pillar or fin, as in the above-described embodiments. This could potentially be an advantage over those embodiments, where a narrow bottom diode region might lead to a deleterious series resistance penalty at high current operation. The crystal surfaces of gallium nitride at the interface between the bottom diode region 730 and the active diode region 760, as well as the crystal surfaces of gallium nitride at the interface between the active diode region 760 and the top diode region 770, are semi-polar planes, which means the internal quantum efficiency of the LED will be higher than it would be if the crystal surfaces at those interfaces were polar c-planes.

[0165] As an alternate architecture, the embodiment illustrated in Figure 35 may be configured by creating ART openings in the dielectric layer other than holes, such as, for example trenches.

[0166] Following are examples of process parameters to form the bottom, active, and top diode regions according to embodiments in this disclosure. First, a substrate and a patterned dielectric layer as known in the art are provided. Exemplary process parameters of growth conditions (e.g., CVD) for bottom, active, and top diode regions, for a GaN and InGaN-based LED, according to the embodiment of Figure 35 are as follows. In this example, the bottom diode region can have two layers. Growth conditions for a first GaN layer as a low-temp buffer (e.g., 30 nm thick) include i) pressure: 100 Torr., ii) precursors: TMG and NH3, diluted in H2, iii) temperature: 530C and iv) dopant: N-type dopant is silicon. Growth conditions for a second GaN layer as a hi-temp buffer (e.g., 500 nm thick) include i) pressure: 100 Torr., ii) precursors: TMG and NH3, diluted in H2, iii) temperature: 1030C and iv) dopant: Ntype doping with silicon. In this example, the active diode region can have two layers. Growth conditions for a first layer of InGaN as a quantum well for emission (e.g., 2 nm thick) include i) pressure: 100 Torr., ii) precursors: TMG+TMI (Trimethylindium) +NH3, diluted in N2, iii) temperature: 740C and iv) dopant: no doping. Growth conditions for a second layer of GaN as a barrier layer for carrier confinement (e.g., 15 nm thick) include i) pressure: 100 Torr., ii) precursors: TMG and NH3, diluted in H2, iii) temperature: 860C and iv) dopant: N-type doping with silicon. In this example, the top diode region is at the active diode layer. Growth conditions for a layer of GaN (e.g., 100 nm thick) include i) pressure: 100 Ton., ii) precursors: TMG and NH3, diluted in H2, iii) temperature: 950C and iv) dopant: P-type: dopant is magnesium. The top diode region can operate as a p contact layer.

[0167] The embodiment shown in. Figure 35 is a semiconductor diode from III-nitride semiconductor materials such as gallium nitride on a silicon substrate that can comprise a silicon substrate 700; a dielectric layer 710 containing a hole 720 which exposes the surface of the silicon substrate, the hole 720 having substantially vertical sidewalls, the ratio of the depth of the hole 720 to the diameter of the hole 720 being greater than 1; a bottom diode region 730 of semiconductor material filling the hole and extending upward in the shape of a six-sided pyramid; a trapping region 750 in the lowest segment of the bottom diode region 730 wherein threading dislocations 740 intersect the curved sidewalls of the dielectric material 710 and terminate; an active diode region 760 of semiconductor material grown conformally around the bottom diode region 730; a top diode region 770 of semiconductor material grown conformally around the active diode region 760; a top electrical contact 780; and a bottom electrical contact 790.

[0168] Figure 36 illustrates a method of fabricating the embodiment of Figure 35. It is a method of creating a light-emitting diode made from III-nitride semiconductors on a silicon substrate comprising the following steps. Step 1600 includes depositing a layer of dielectric material, such as dielectric material 710, onto the surface of a silicon substrate, such as silicon substrate 700. Step 1605 includes patterning a hole, such as hole 720, in the layer of dielectric material to expose the surface of the silicon substrate, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole being greater than or equal to one. Step 1610 includes growing a III-nitride semiconductor material to form a bottom diode region, such as bottom diode region 730, which fills the hole and extends upwards in the shape of a six-sided pyramid. Step 1615 includes growing a III-nitride semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region,

such as active diode region 760. Step 1620 includes growing a III-nitride semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 770. Step 1625 includes fabricating a top electrical contact, such as top electrical contact 780, on the exposed surface of the top diode region. Step 1630 includes fabricating a bottom electrical contact, such as bottom electrical contact 790, on the bottom of the silicon substrate.

[0169] The embodiment shown in Figure 38 is a variation of the embodiment of Figure 35 in which the silicon substrate is removed to eliminate the possibility that it will absorb light generated in a light-emitting diode. The structure shown in Figure 34 is first provided. A semiconductor material is grown to create the bottom diode region 730, as shown in Figure 37. The semiconductor material for the bottom diode region 730 fills the hole 710 and grows in the form of a six-sided pyramid.

[0170] A III-nitride semiconductor material is conformally grown around the top and sides of the bottom diode region 730 to create an active diode region 760.

[0171] A III-nitride semiconductor material is conformally grown around the top and sides of the active diode region 760 to form a top diode region 800. In this case, the top diode region 800 continues to grow until the growth fronts from adjacent diodes coalesce. An optional step is to planarize the resultant surface of the top diode region 800, which can be preferable depending on the quality of that surface.

[0172] The structure is inverted, and a handle substrate 810 is bonded to the surface of the top diode region 800 (which is now on the bottom of the structure), as shown in Figure 38. The handle substrate 810 can be part of an LED packaging fixture. In some embodiments the handle

substrate 810 is electrically conductive, and in others it contains conductor elements which will serve as contacts for the top diode region 800.

[0173] The initial silicon substrate 700 is removed by one or more methods such as grinding, etching with a chemical such as tetramethyl ammonium hydroxide, or laser ablation.

[0174] Top electrical contact 820 and bottom electrical contact 830 are created to generate the completed structure shown in Figure 38.

[0175] The embodiment of Figure 38 may offer the same advantages as the embodiment of Figure 35 and may additionally offers greater extraction efficiency as a light-emitting diode because it contains no silicon substrate 700 to absorb any of the internally generated light.

[0176] The embodiment shown in Figure 38 can include a semiconductor diode from III-nitride semiconductor materials such as gallium nitride on a silicon substrate comprising a layer of dielectric material 710 containing a hole 720, the hole 720 having substantially vertical sidewalls, and the ratio of the depth of the hole 720 to the diameter of the hole 720 being greater to or equal to 1; a bottom diode region 730 of semiconductor material which fills the hole 720 and then takes the configuration of a six-sided pyramid; a trapping region 750 within the bottom diode region 730 wherein threading dislocations 740 intersect the sidewall of the hole (160 and terminate; an active diode region 760 of semiconductor material grown conformally around the bottom diode region 730; a top diode region 800 of semiconductor material grown conformally around the active diode region; a handle substrate 810; top electrical contacts 820; and bottom electrical contacts 830.

[0177] Figure 39 illustrates a method of fabricating the embodiment of Figure 38. It is a method of creating a light-emitting diode made from III-nitride semiconductors on a silicon

substrate comprising the following steps. Step 1700 includes depositing a layer of dielectric material, such as dielectric material 710, onto the surface of a silicon substrate, such as silicon substrate 700. Step 1705 includes patterning a hole, such as hole 720, in the layer of dielectric material to expose the surface of the silicon substrate, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole being greater than or equal to 1. Step 1710 includes growing a III-nitride semiconductor material to form a bottom diode region, such as bottom diode region 730, which fills the hole and extends upward in the shape of a six-sided pyramid. Step 1715 includes growing a III-nitride semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region, such as active diode region 760. Step 1720 includes growing a III-nitride semiconductor material conformally around the top and sides of the active diode region to create a top diode region, such as top diode region 800. Step 1725 includes continuing to grow the top diode region until the growth fronts from adjacent diodes coalesce. Step 1730 includes planarizing the surface of the top diode region. Step 1735 includes bonding a handle substrate, such as handle substrate 810, to the surface of the top diode region. Step 1740 includes removing the silicon substrate by a chemical or mechanical process. Step 1745 includes fabricating a top electrical contact, such as top electrical contact 820, on the exposed surface of the layer of the dielectric material. Step 1750 includes fabricating a bottom electrical contact, such as bottom electrical contact 830, on the exposed surface of the handle substrate.

[0178] Embodiments of the disclosure provide novel and useful architectures for diodes made from compound semiconductors or other non-lattice-matched semiconductors deposited on silicon substrates by Aspect Ratio Trapping. The semiconductor diode is the fundamental

building block of solar cells, light-emitting diodes, resonant tunneling diodes, semiconductor lasers, and other devices.

[0179] One aspect of the present disclosure is to reduce the costs of solar cells, light-emitting diodes, and other compound semiconductor devices by creating them on high-quality, large-area, low-cost silicon wafers instead of smaller, more expensive substrates.

[0180] Another aspect of the present disclosure is to improve the extraction efficiency and the internal quantum efficiency of light-emitting diodes by exploiting non-polar planes of III-nitride semiconductors.

[0181] As such, one embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric material including an opening that exposes a portion of the substrate, the opening having an aspect ratio of at least 1, a bottom diode material disposed in and above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate, a top diode material proximate the upper region of the bottom diode material, and an active diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface of the substrate.

[0182] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer, and may have a crystal orientation of (111) or (100). The dielectric material may comprise silicon dioxide or silicon nitride. The semiconductor material may comprise a Group IIIV compound, a Group II-VI compound, a Group IV alloy, or combinations thereof.

[0183] The active diode region may comprise a p-n junction formed by a junction of the top and bottom diode materials. The active diode region may comprise a material different from the

top and bottom diode materials, and the active diode region may form an intrinsic region of a p-i-n junction formed between the top and bottom diode materials. The active diode region may comprise multiple quantum wells formed between the top and bottom diode materials.

[0184] The opening may be a trench or may be a hole having an aspect ratio of at least 1 in two perpendicular axes.

[0185] The bottom diode material may include an n-type dopant, and the top diode material may include a p-type dopant.

[0186] The upper region of the bottom diode material may form a fin above the opening. The upper region of the bottom diode material may form a pillar above the opening.

[0187] The diode may further comprises a contact formed over the top diode region. The contact may comprise a transparent conductor. The diode may further comprise a second contact formed adjacent the substrate.

[0188] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric material including an opening that exposes a portion of the substrate, a bottom diode material including a lower region disposed at least partly in the opening and an upper region extending above the opening, the lower region including a plurality of misfit dislocations that terminate below the upper region, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate, a top diode material proximate the upper region of the bottom diode material, and an active light emitting diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface of the substrate.

[0189] The active light emitting diode region may comprise a p-n junction formed by a junction of the top and bottom diode materials. The active light emitting diode region may comprise a material different from the top and bottom diode materials, and the active light emitting diode region may form an intrinsic region of a p-i-n junction formed between the top and bottom diode materials. The active light emitting diode region may comprise multiple quantum wells formed between the top and bottom diode materials.

[0190] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer. The single crystal silicon wafer may have a crystal orientation of (111) or (100). The dielectric material may comprise silicon dioxide or silicon nitride. The semiconductor material may comprise a Group IIIV compound, a Group II-VI compound, a Group IV alloy, or combinations thereof.

[0191] The opening may be a trench or may be a hole having an aspect ratio of at least 1 in two perpendicular axes.

[0192] The bottom diode material may include an n-type dopant and the top diode material includes a p-type dopant. The upper region of the bottom diode material may form a fin above the opening. The upper region of the bottom diode material may form a pillar above the opening.

[0193] The diode may further comprises a contact formed over the top diode region. The contact may comprises a transparent conductor. The diode may further comprise a second contact formed adjacent the substrate.

[0194] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric layer having a thickness of no more than about 20 nm above the substrate,

the dielectric layer including an opening that exposes a portion of the substrate, a bottom diode material including a lower region disposed at least partly in the opening and an upper region extending above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate, a top diode material proximate the upper region of the bottom diode material, and an active diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface of the substrate.

[0195] The active diode region may comprise a p-n junction formed by a junction of the top and bottom diode materials. The active diode region may comprise a material different from the top and bottom diode materials, and the active diode region may form an intrinsic region of a p-i-n junction formed between the top and bottom diode materials. The active diode region may comprise multiple quantum wells formed between the top and bottom diode materials.

[0196] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer. The single crystal silicon wafer may have a crystal orientation of (111) or (100). The dielectric material may comprise silicon dioxide or silicon nitride. The semiconductor material may comprise a Group III-V compound, a Group II-VI compound, a Group IV alloy, or combinations thereof.

[0197] The opening may be a trench or may be a hole having an aspect ratio of at least 1 in two perpendicular axes.

[0198] The bottom diode material may include an n-type dopant and the top diode material may include a p-type dopant. The upper region of the bottom diode material may form a fin above the opening. The upper region of the bottom diode material may form a pillar above the opening.

[0199] The diode may further comprise a contact formed over the top diode region. The contact may comprise a transparent conductor. The diode may further comprise a second contact formed adjacent the substrate.

[0200] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric material disposed above the substrate, the dielectric material including a plurality of openings that each expose a portion of the substrate, a plurality of bottom diode sections comprising a bottom diode material, each section including a lower region disposed in an opening and an upper region extending above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate, a contiguous top diode section proximate the upper regions of the bottom diode section, the top diode section comprising a top diode material, and a plurality of active diode regions between the top and bottom diode materials, the active diode regions each including a surface extending away from the top surface of the substrate.

[0201] The plurality of active diode regions may comprise a p-n junction formed by a junction of the contiguous top and plurality of bottom diode materials. The plurality of active diode regions may comprise a material different from the contiguous top and plurality of bottom diode materials, and the plurality of active diode regions may form an intrinsic region of a p-i-n junction formed between the contiguous top and plurality of bottom diode materials. The plurality of active diode regions may comprise multiple quantum wells formed between the contiguous top and plurality of bottom diode materials.

[0202] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer. The single crystal silicon wafer may have a crystal orientation of (111) or (100). The dielectric material may comprise

silicon dioxide or silicon nitride. The semiconductor material may comprise a Group IIIV compound, a Group II-VI compound, a Group IV alloy, or combinations thereof.

[0203] The opening may be a trench or may be a hole having an aspect ratio of at least 1 in two perpendicular axes.

[0204] The bottom diode material may include an n-type dopant and the top diode material may include a p-type dopant. The upper regions of the plurality of bottom diode materials may form a fin above the opening. The upper regions of the plurality of bottom diode materials may form a pillar above the opening.

[0205] The diode may further comprise a contact formed over the contiguous top diode region. The contact may comprise a transparent conductor. The diode may further comprise a second contact formed adjacent the substrate.

[0206] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a bottom diode material that is lattice mismatched to the substrate extending above the top surface and including a bottom diode section having a width across the top surface and a height above the top surface, the height being greater than the width, a top diode material proximate the bottom diode material, and an active light emitting diode region between the top and bottom diode materials, the active diode region including a surface extending away from the top surface of the substrate.

[0207] The active light emitting diode region may comprise a p-n junction formed by a junction of the top and bottom diode materials. The active light emitting diode region may comprise a material different from the top and bottom diode materials, and the active light emitting diode region may form an intrinsic region of a p-i-n junction formed between the top

and bottom diode materials. The active light emitting diode region may comprise multiple quantum wells formed between the top and bottom diode materials.

[0208] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer. The single crystal silicon wafer may have a crystal orientation of (111) or (100). The dielectric material may comprise silicon dioxide or silicon nitride.

[0209] The bottom diode material may include an n-type dopant and the top diode material may include a p-type dopant.

[0210] The diode may further comprise a contact formed over the top diode region. The contact may comprise a transparent conductor. The diode may further comprise a second contact formed adjacent the substrate.

[0211] Another embodiment of the present disclosure is directed to a method of making a diode, the method comprising depositing a layer of a dielectric material onto a substrate, patterning first and second openings in the dielectric material to expose portions of the substrate, each of the openings having an aspect ratio of at least 1, forming a first bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in and above the first opening, forming a second bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in and above the second opening, forming a first active diode region adjacent the first bottom diode region, forming a second active diode region adjacent the second bottom diode region, and forming a single top diode region adjacent the first active diode region and the second active diode region.

[0212] The first and second active diode regions may contain multiple quantum wells.

[0213] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate may be a single crystal silicon wafer. The substrate may have a crystal orientation of (111) or (100). The dielectric material may comprise silicon dioxide or silicon nitride.

[0214] The first and second openings may be trenches or may be holes. The semiconductor material may comprise a Group III-V compound, a Group IIVI compound, a Group IV alloy, or combinations thereof.

[0215] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric material above the substrate, the dielectric material including an array of openings, a plurality of bottom diode sections formed in and above the array of openings, each bottom diode section including at least one sidewall that extends away from the dielectric material, the bottom diode sections comprising a semiconductor material that is lattice mismatched to the substrate, a plurality of top diode sections proximate the bottom diode sections, and a plurality of active diode regions between the top and bottom diode sections, the active diode regions each including a surface extending away from the top surface of the substrate.

[0216] Each opening may have an aspect ratio of at least 0.5, at least 1, at least 2 or greater than 3. Each bottom diode section may include at least one sidewall that extends substantially vertically upward above the dielectric material. Each bottom diode section may have an hexagonal cross-section. The openings may be arranged in an hexagonal array. The top diode sections may be formed from a single, contiguous layer of material. The diode may be a light emitting diode.

[0217] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a first dielectric layer above the substrate, a layer of a refractory metal above the first dielectric layer, an opening through the first dielectric layer and the layer of refractory metal, the opening having dielectric sidewalls, a bottom diode region comprising a compound semiconductor material that is lattice mismatched to the substrate, the bottom diode region disposed in and above the opening, a top diode region proximate the bottom diode region, and an active diode region between the top diode region and a top portion of the bottom diode region.

[0218] The opening may have an aspect ratio of at least 1, and may be a trench. The diode may further comprise a second dielectric layer covering at least a portion of the top diode region. The diode may further comprise a second opening extending through the second dielectric layer and a first contact comprising a metal plug, the metal plug filling the second opening and contacting the layer of refractory metal. The diode may further comprise a second contact at the bottom of the substrate.

[0219] Another embodiment of the present disclosure is directed to a method of making a diode, the method comprising depositing a first layer of dielectric material above a substrate, depositing a layer of a refractory metal above the first layer of dielectric material, depositing a second layer of dielectric material above the layer of refractory material, forming a first opening defined by sidewalls extending through the first layer of dielectric material, layer of refractory metal, and second layer of dielectric material to expose a surface of the substrate, forming a layer of dielectric material on the sidewalls of the opening, forming a bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in and above the opening, removing the second dielectric layer, forming an active diode region adjacent a portion of the bottom diode region, and forming a top diode region that adjacent the active diode region.

[0220] The method may further comprise depositing a third layer of dielectric material on the top diode region that conformally covers the active diode region and the refractory metal, creating a via through the third layer of dielectric material and a portion of the top diode region that covers the refractory metal, filling the via with a plug a metal such that the plug is in contact with the layer of refractory metal, and fabricating a bottom electrical contact.

[0221] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric layer above the substrate, the dielectric layer including an opening having an aspect ratio of at least 1, a bottom diode region disposed in and above the opening, the bottom diode region comprising a compound semiconductor material having an hexagonal crystal lattice, the bottom diode region including sidewalls defined by non-polar planes of the compound semiconductor material, a top diode region proximate the bottom diode region, and an active diode region between the top and bottom diode regions.

[0222] The substrate may be a crystalline substrate having a cubic lattice. The non-polar plane may be an a-plane or may be an m-plane. The opening may be a trench or may be a hole.

[0223] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric layer above the substrate including an opening, a semiconductor material that is lattice mismatched to the substrate disposed in the opening, and a pyramidal diode comprising a pyramidal p-n junction disposed above the opening.

[0224] The pyramidal diode may further include a top diode material, an active diode material, and a bottom diode material. The pyramidal diode may have a height of greater than about 3 microns or may have a height of greater than about 5 microns. The pyramidal diode may include a top contact layer having a thickness of less than about 2 microns, or a top contact layer

having a thickness of less than about 0.5 microns. The pyramidal diode may include a bottom contact layer.

[0225] The diode may further comprise multiple pyramidal diodes having the respective top diode materials coalesced together. The diode may further include a transparent top contact layer. The diode may further include a handle substrate.

[0226] The substrate may be selected from the group consisting of silicon, sapphire, and silicon carbide. The semiconductor material may be selected from the group consisting of a Group III-V compound, a Group II-VI compound, and a Group IV alloy.

[0227] Another embodiment of the present disclosure is directed to a method of forming a diode comprising providing a substrate, providing a dielectric including an opening having an aspect ratio of at least 1 above the substrate, forming a compound semiconductor material that is lattice mismatched to the substrate in the opening, forming a diode comprising a p-n junction above the opening, forming a dielectric material having a substantially planar surface above the diode, bonding a handle wafer to the substantially planar surface, and removing the substrate.

[0228] The opening may be a trench or may be a hole. The diode may include a top diode region, a bottom diode region, and an active diode region. The diode may include a plurality of top diode regions, a plurality of bottom diode regions, and a plurality of active diode regions. The plurality of top diode regions may be coalesced together.

[0229] Another embodiment of the present disclosure is directed to a diode comprising a substrate, a dielectric layer above the substrate including an array of openings, the openings having a width less than 100 nm, a plurality of nanostructures comprising a semiconductor material that is lattice mismatched to the substrate disposed in and above the array of openings,

the nanostructures having a substantially uniform height extending at least 100 nm above the dielectric layer, and a plurality of diode junctions formed on the nanostructures, the diode junctions including active regions using the nanostructure sidewalls.

[0230] The nanostructures may be in the form of a fin or pillar. The width of the nanostructure may be selected from the group consisting of about 5 nm, about 10 nm, about 20 nm, and about 50 nm. The height of the nanostructure may be selected from the group consisting of about 100 nm, about 200 nm, about 500 nm, and about 1000 nm.

[0231] Another embodiment of the present disclosure is directed to a diode comprising a first diode material comprising a substantially planar bottom surface and a top surface having a plurality of cavities, a second diode material comprising a substantially planar top surface and a bottom surface extending into the plurality of cavities in the first diode material, and an active diode region between the first and second diode materials.

[0232] The diode may further comprise a substrate having a substantially planar surface adjacent the bottom surface of the first diode material or the top surface of the second diode material.

[0233] The active diode region may comprise a p-n junction formed by a junction of the first and second diode materials. The active diode region may comprise a material different from the first and second diode materials, and the active diode region may form an intrinsic region of a p-i-n junction formed between the first and second diode materials. The active diode region may comprise multiple quantum wells formed between the first and second diode materials.

[0234] A first diode material may comprise a III-V material. The first diode material may comprise GaN. The cavities may include a polar GaN surface.

[0235] The cavities may define trenches or may define holes having an aspect ratio of at least 1. The surface area of the cavities may exceed the surface area of the bottom surface of the first diode material. The surface area of the cavities may be at least 150% of the surface area of the bottom surface of the first diode material, or may be at least 200% of the surface area of the bottom surface of the first diode material.

[0236] Embodiments of the application provide methods, structures or apparatus described with respect to "fin" configured structures based on growth control from trench orientations. As would be recognized by one skilled in the art based on the disclosure herein, the trench orientation could be another shaped opening such as a hole, recess, square or ring, for example, which would result in other three-dimensional semiconductor structures or apparatus.

[0237] Embodiments of the application provide methods, structures or apparatus that may use and/or form by epitaxial growth or the like. For example, exemplary suitable epitaxial growth systems may be a single-wafer or multiple-wafer batch reactor. Various CVD techniques may be used. Suitable CVD systems commonly used for volume epitaxy in manufacturing applications include, for example, an Aixtron 2600 multi-wafer system available from Aixtron, based in Aachen, Germany; an EPI CENTURA single-wafer multi-chamber systems available from Applied Materials of Santa Clara, Calif.; or EPSILON single-wafer epitaxial reactors available from ASM International based in Bilthoven, The Netherlands.

[0238] Any reference in this specification to "one embodiment," "an embodiment," "example embodiment," "another embodiment," "other embodiments," etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further,

when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to affect such feature, structure, or characteristic in connection with other ones of the embodiments. Furthermore, for ease of understanding, certain method procedures may have been delineated as separate procedures; however, these separately delineated procedures should not be construed as necessarily order dependent in their performance. That is, some procedures may be able to be performed in an alternative ordering, simultaneously, etc. In addition, exemplary diagrams illustrate various methods in accordance with embodiments of the present disclosure. Such exemplary method embodiments are described herein using and can be applied to corresponding apparatus embodiments, however, the method embodiments are not intended to be limited thereby.

[0239] Although few embodiments of the present invention have been illustrated and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein. As used in this disclosure, the term "preferably" is non-exclusive and means "preferably, but not limited to." Terms in the claims should be given their broadest interpretation consistent with the general inventive concept as set forth in this description. For example, the terms "coupled" and "connect" (and derivations thereof) are used to connote both direct and indirect connections/couplings. As another example, "having" and "including", derivatives thereof and similar transitional terms or

phrases are used synonymously with "comprising" (i.e., all are considered "open ended" terms) - only the phrases "consisting of" and "consisting essentially of" should be considered as "close ended". Claims are not intended to be interpreted under 112 sixth paragraph unless the phrase "means for" and an associated function appear in a claim and the claim fails to recite sufficient structure to perform such function.

What is claimed is:

1. A diode comprising: a substrate; a dielectric material including an opening that exposes a portion of the substrate, the opening having an aspect ratio of at least 1; a bottom diode material including a lower region disposed at least partly in the opening and an upper region extending above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate; a top diode material proximate and disposed laterally from a sidewall of the upper region of the bottom diode material; and an active diode region between a sidewall of the top diode material and the sidewall of the upper region of the bottom diode material, the active diode region including a surface extending away from a top surface of the substrate.

2. The diode of claim 1 wherein the active diode region comprises a p-n junction formed by a junction of the top and bottom diode materials.

3. The diode of claim 1 wherein the active diode region comprises a material different from the top and bottom diode materials, and the active diode region forms an intrinsic region of a p-i-n junction formed between the top and bottom diode materials.

4. The diode of claim 1 wherein the active diode region comprises multiple quantum wells formed between the top and bottom diode materials.

5. The diode of claim 1 wherein the substrate is selected from the group consisting of silicon, sapphire, and silicon carbide.

6. The diode of claim 1 wherein the substrate is a single crystal silicon wafer.

7. The diode of claim 1 wherein the opening is a trench, and wherein the upper region of the bottom diode material forms a fin above the trench.

8. The diode of claim 1 wherein the opening is a hole having the aspect ratio in two

perpendicular axes, and wherein the upper region of the bottom diode material forms a pillar above the opening.

9. The diode of claim 1 wherein the semiconductor material comprises a material selected from the group consisting essentially of a Group III-V compound, a Group II-VI compound, and a Group IV alloy.

10. The diode of claim 1 wherein the bottom diode material includes an n-type dopant and the top diode material includes a p-type dopant.

11. A diode comprising: a substrate; a bottom diode material that is lattice mismatched to the substrate, the bottom diode material extending above a top surface of the substrate and including a bottom diode section having a width across the top surface and a height above the top surface, the height being greater than the width; a top diode material proximate the bottom diode material; and an active light emitting diode region between the top and bottom diode materials, the active light emitting diode region including a surface at an interface between the active light emitting diode region and the bottom diode material, the surface extending away from the top surface.

12. The diode of claim 11 wherein the active light emitting diode region comprises a p-n junction formed by a junction of the top and bottom diode materials.

13. The diode of claim 11 wherein the active light emitting diode region comprises a material different from the top and bottom diode materials, and the active light emitting diode region forms an intrinsic region of a p-i-n junction formed between the top and bottom diode materials.

14. The diode of claim 11 wherein the active light emitting diode region comprises multiple quantum wells formed between the top and bottom diode materials.

15. The diode of claim 11 wherein the bottom diode material includes an n-type

dopant and the top diode material includes a p-type dopant.

16. A structure comprising: a substrate; a dielectric material including an opening to a surface of the substrate; a bottom diode material including a lower region and an upper region, the lower region being disposed at least partly in the opening, and the upper region having a sidewall extending above the opening, the bottom diode material comprising a semiconductor material that is lattice mismatched to the substrate; an active diode region along the sidewall of the upper region of the bottom diode material, the active diode region having a sidewall laterally distal from the sidewall of the upper region of the bottom diode material; and a top diode material along the sidewall of the active diode region.

17. The structure of claim 16, the opening having an aspect ratio of at least 1.

18. The structure of claim 16, wherein the opening is a trench, and wherein the upper region of the bottom diode material forms a fin above the trench.

19. The structure of claim 16, wherein the opening is a hole having a circular cross sectional area in a plane parallel to the surface of the substrate, and wherein the upper region of the bottom diode material forms a pillar above the opening.