

Description

The present invention relates to a refresh generator system to provide automatic refreshing of a dynamic memory.

Dynamic random access memories (DRAM's) used in most present processor systems, especially microcomputers, store data by the state of charge on capacitive cells. These cells are arranged in a matrix configuration with column and row drive lines and are individually selected by first applying a row address together with a row address strobe (RAS) signal followed by a column address strobe (CAS) signal. Each time a row is addressed, either for read or write, all the cells in that row are refreshed. However a DRAM has a maximum refresh time of a few milliseconds during which all of the cells must be refreshed. In normal processing operations much of the memory may remain unaccessed for such periods. Consequently, arrangements must be made to ensure that all of the rows of the memory are accessed within the maximum refresh time.

In certain memory systems, such as the MCM 6664 memory chip manufactured by Motorola Inc., the chip includes a counter which provides successive row addresses for memory refresh. In such systems, each memory operation includes a read, a write and a refresh cycle, in the last of which the row addresses is defined by the counter value. Such systems have the disadvantage that they perform more refresh cycles than are required to refresh all of the cells within the minimum refresh time.

In the IBM Personal Computer, memory refresh is effected under the control of a programmable direct memory access (DMA) unit. This device is designed to improve system performance by allowing direct data transfer between the memory and external devices. One channel is used for memory refresh and is programmed to provide successive row address counts. In response to a refresh timer output, the DMA gains control of the system by forcing a 'not read' condition to the main processor, an 8088 chip manufactured by Intel Corp., and tristating its systems bus control lines so that the DMA can apply the programmed row address to refresh a memory row. The refresh overhead in this machine, that is, the proportion of total processing time used for refresh, is approximately 7%.

The present invention arose from the requirement to refresh a DRAM in a system in which a DMA gains control of a processor by means of a Hold Request/Acknowledge handshaking sequence rather than the direct control arrangement used in the IBM Personal Computer as described above. The 80286 microprocessor, manufactured by Intel Corp., has a bus hold request input and a hold acknowledge output. The hold request input allows another device to request control of the local bus. When the microprocessor grants control, it floats its bus drivers to the tristate OFF condition and then activates the

hold acknowledge output. The local bus now remains granted to the requesting device until this device de-activates the hold request signal. Using a DMA to effect memory refresh, and with the DMA operating at a cycle time of twice that of the main processor, it was discovered that the refresh overhead was increased to 12%.

Accordingly, an object of the present invention is to provide a memory refresh system with a reduced refresh overhead in a system in which a direct memory access controller has a requirement to use the HOLD facility of the processor.

It is pointed out that a paper published on pages 84-92 of "Electronic Design", Vol. 9, 26th April 1978, proposes a processing system without a DMA which dedicates the HOLD and HLDA facilities of the processor to refreshing. The basic memory organisation disclosed is one in which an address from the processor is segregated into row and column sub-addresses, the row sub-addresses being selectively distributed to the chips of the memory and the column sub-addresses being distributed to all the chips. If no row sub-address is received by a chip, it ignores the column sub-address received. In this context, refreshing "borrows" the row address logic to address a row for refreshing with the processor quiesced by the HOLD/HLDA loop. The identity of the row being determined by the contents of a counter which is advanced at the start of a refresh cycle. Clearly, where a DMA controller contends for the HOLD/HLDA loop, this refresh system cannot be adopted directly.

On the other hand, EP-A-0 071 743 discloses a comparable system incorporating a DMA controller, with the highest priority channel of the DMA controller dedicated to a refresh timer. This channel, as do the other channels of the DMA controller, incorporates an address counter which is advanced each refresh cycle and an auto-load function which wraps the address counter. Since the DMA controller is used for refreshing, there is no contention between the DMA controller and the refresh timer for the HOLD/HLDA loop.

The present invention tackles the problems of a system where there is contention and provides refresh apparatus in or for a data processing system which includes a process which, in response to a hold request (HRQ)—signal relinquishes control of its local bus and generates a hold acknowledge (HLDA)—signal, memory modules which are addressed via a multiplexer with row and column addresses supplied in parallel by the processor and require refreshing by row, and a direct memory access (DMA)—controller having a DMA—clock input derived from the system clock and generating, as required, latched hold request (LRHQ)—signals characterised by a refresh generator inserted between said LRHQ—signal output of the DMA—controller and the HRQ—signal input of the processor and coupling directly to the memory modules and the DMA—clock input, comprising:

first logic means responsive the DMA—clock, inverted, and to a periodic signal from a refresh

timer circuit to generate said HRQ—signal for the processor in response to the timer, and otherwise passing any extant LHRQ—signal to the HRQ—signal input of the processor,

second logic means responsive to said hold acknowledge signal from the processor to generate an inverted refresh control signal,

third logic means responsive to said inverted refresh control signal, to provide a refresh signal to control memory row access,

a counter circuit coupled to be incremented by one in response to each refresh control signal, and

a sequencer circuit responsive to each refresh control signal to generate a first gating signal to gate the current count in the counter circuit, representing a memory row address, to the memory and thereafter to generate a second gating signal to generate a memory read signal and to reset said memory read signal.

The present invention will be described further by way of example with reference to an embodiment thereof as illustrated in the accompanying drawing in which:—

Figure 1 is a block diagram of one form of memory addressing system of the present invention in a microcomputer system;

Figure 2 is a detailed block diagram of a memory refresh system within the addressing system of Figure 1; and

Figure 3 is a waveform diagram illustrating the input and output signals of the system.

Referring to Figure 1, this is a simplified block diagram of the addressing system of a microcomputer incorporating a memory refresh system embodying the present invention. A microprocessor 1, which may be an 80286 chip produced by Intel Corp., is shown with 24 address outputs A0 through A23, a hold acknowledge output HLDA, a clock input CLK and hold request input HRQ. The remaining 41 connections to the 80286 have been omitted from Figure 1 as they form no part of the present invention. The address outputs and clock input are self-explanatory. The HRQ and HLDA connection control ownership of the 80286 local bus. An HRQ input allows another device to request control of the local bus. When the 80286 grants control, it floats its bus drivers to an OFF condition and activates the HLDA output, thus entering a bus hold acknowledge condition. The local bus will now remain granted to the requesting device until HRQ becomes inactive, which results in the 80286 deactivating the HLDA output and regaining control of the local bus. Both HRQ and HLDA are active high signals. Address signals A0 through A16 from processor 1 are applied to an address unit 2 to address a dynamic random access memory system (DRAM) 3. The essential function of address unit 2 is to multiplex the 16 bit address inputs to provide, for each such input, two successive 8 bit outputs on its A0 through A7 output lines. The first of these outputs corresponds with the A0 through A7 inputs and is applied to the memory to provide a row address. The second

corresponds with the A8 through A15 inputs to provide a column address. These addresses are interpreted by memory 3 as row and column addresses respectively in response to the successive application of row address strobe (RAS) and column address strobe (CAS) signals to respective inputs to the memory.

Memory 3 comprises a number of banks of 256×256×1 bit chips, each having a 64K bit capacity. Each bank comprises eight such chips to store 64K bytes, with the chips in a bank connected in common to a single RAS and a single CAS input line. With, for example, four RAS inputs and two CAS inputs, up to eight such banks can be accessed in memory 3, giving a total capacity of 500K bytes.

The RAS and CAS inputs to memory 3 are selected by a memory controller 4, which includes a read-only memory device responsive to address inputs from address outputs A17 through A23 from processor 1 to select RAS and CAS outputs. In fact, this unit has other outputs used, for example, to select the system read-only control memory, but these outputs are not shown for simplicity. The other input to controller 4 is a refresh input REFR, this is used to activate all the RAS outputs simultaneously.

A memory refresh unit 5 includes address outputs A0 through A7, which are applied directly to memory unit 3, a refresh output REFR coupled to memory controller 4 and a HRQ output for processor 1. The refresh unit receives a HLDA input from processor 1 and timer inputs from a timer 6 which itself is responsive to signals from a system clock unit 7.

The specific operation of refresh unit 5 will be discussed in detail below with reference to figure 2. However, in brief, this unit is responsive to each output from timer 6 to develop a HRQ output. When main processor 1 accepts this output it enters its bus hold condition and passes an acknowledge signal to the HLDA input of refresh unit 5. In response to the HLDA signal refresh unit issues a refresh output to the REFR input of memory controller to activate all the RAS lines and also provides a single row address to refresh all the memory cells in each bank of memory chips associated with that address. Refresh unit 5 then de-activates the HRQ output to allow the main processor to gain control of the system busses. For each timer input, a counter in the refresh unit is incremented by one to generate a new address count on outputs A0 through A7 such that these count outputs are incremented from 0 through 255 thereby addressing each memory row in turn for a full refresh operation.

Figure 2 shows details of refresh unit 5 of Figure 1. This unit has three clocking inputs. The first is from timer 6 (Figure 1), which is arranged to generate a signal each 15 μ secs to initiate a refresh operation. The second is an 8 MHz clock from clock 7 (Figure 1), which is the system clock, and the third is a 4 MHz clock, also derived from clock 7, which is also used to drive a programmable direct memory access controller (not shown

in Figure 1) which, as explained above is normally used to control direct data transfer between memory 3 (Figure 1) and I/O devices (not shown) connected to the system. It is this DMA which normally generates a hold request signal (HRQ) for processor 1 to initiate a handshaking sequence, using the hold acknowledge signal (HLDA) to gain control of the bus system from processor 1. This hold request signal from the DMA, after latching, enters the Figure 2 unit as a latched hold request input LHRQ. The LHRQ signal, which is active high, is applied as an inverted input to an AND gate 10 which, when its other input from the -Q output of a flip-flop 11 is high, changes its output from high to low. This low output, in the absence of a high output from AND gate 12, provides a high HRQ signal for processor 1 from an OR gate 13. Thus, DMA hold request signals are passed directly through AND gate 10 and OR gate 13 to processor 1. They are latched by the corresponding HLDA input through AND gate 12.

The HRQ signal is alternatively generated in response to an output from flip-flop 11. This flip-flop is driven by the Q output of a flip-flop 14. As mentioned above, the timer input provides a signal every 15 μ secs. This input clocks the D input, which is permanently high, to the Q output of flip-flop 14. This output is directly connected to the D input of flip-flop 11 and is transferred to the Q output of this flip-flop on the first positive-going excursion of the 4 MHz clock input. It should be noted here that this 4 MHz signal is the inverse of the 4 MHz signal driving the DMA, thus insuring that the LHRQ input from the DMA can not coincide with the clocking of flip-flop 11. When the D input is clocked to the Q output, the -Q output goes low, thereby generating an active high HRQ output through AND gate 10 and OR gate 13. The Q output from flip-flop 11, now high, is applied to the D input of a flip-flop 15 which, on the next positive-going excursion of the 8 MHz system clock, raises its Q output. This output, together with the HLDA input and the HRQ signal, now all high, gate an AND gate 16, which, in response thereto, provides a low -REFRESH signal as shown in Figure 3 on line 17. This signal is inverted by an inverter 18 to provide a high refresh signal REFR, which, as has been explained with reference to Figure 1, causes the generation of the memory RAS signals.

The -REFRESH signal on line 17 activates two circuits, a counter/register circuit 19 and a sequencer comprising AND gates 20 and 21 and a multiple flip-flop circuit 22. Counter/register circuit 19 may be of the type SN54CS590 produced by Texas Instruments Corp. This device comprises an 8-bit binary counter feeding an 8-bit storage register. The storage register has parallel outputs QA through QH. Separate clock inputs RCK and CCK are provided for the register and counter respectively. When these are coupled together as shown the counter state is always one ahead of the register. A gate input -G (active low) gates the register to the output terminals QA

through QH to provide memory address outputs A0 through A7. Thus, for each -REFRESH signal on line 17 the counter is clocked by one and for each gating signals on line 23 an address output is provided. These address outputs are sequenced to provide counts from 0 through 255 and then revert back to 0 for the next sequence. The timing of these addresses is shown on the system address SA0-7 line of Figure 3.

Multiple flip-flop circuit 22, prior to the generation of the -REFRESH signal, provides a low output at each of terminals Q1 through Q4, and, therefore, corresponding high outputs at terminals -Q1 through -Q3. The lower input to AND gate 20, fed from the Q3 output of circuit 22 is, therefore low. The -REFRESH input through line 17 therefore gates AND gate 20 to provide a high signal to input D1 of circuit 22. On the next downward transition of the 8 MHz clock, the high D1 input is transferred to the Q1 output, making -Q1 go low. This output from -Q1 gates counter/register 19 to provide the current count in the register to address lines A0 through A7 to provide the system address bits SA0 through SA7 as shown in Figure 3. As Q1 is coupled to D2 in circuit 22, on the next downward transition of the 8 MHz clock, the Q1 high output is transferred to the Q2 output, and -Q2 goes low. This -Q2 output gates a drive 24 to generate a -memory read (-MEMR) signal as shown in Figure 3. This signal controls read cycles of the memory and replaces a normal memory read control signal from a bus controller. Thus the row, defined by the address from counter/register 19, in each of the memory blocks is accessed and thereby refreshed.

Ignoring, for the moment, the I/O channel ready (IOCHRDY) input to the Figure 2 system, the Q2 signal in circuit 22 is coupled to the D3 input, so, on the next downward transition of the 8 MHz clock, Q3 goes high and -Q3 goes low. The -Q3 output is coupled directly to the D4 input, so, on the next clock downward transition Q4 goes low. This output clears latches 14 and 11 over line 25 to drop the HRQ output. This drop disables AND gate 16, so the -REFRESH on line 17 goes high, as shown in Figure 3. The Q3 output, when it goes high, disables gate 20, so that on the same clock cycle as above, Q1 goes low and -Q1 goes high. Thus the -MEMR from -Q1 goes back to its high state as shown in Figure 3. Thereafter during the next two clock pulses, circuit 22 is reset to its initial state, and the Figure 2 circuit waits for the next timer input to carry out a further refresh cycle using the incremented address in counter/register 19. Thus, in response to 256 timer input signals, the whole memory is refreshed.

The I/O channel ready (IOCHRDY) input to the Figure 2 circuit is used if a device on a channel also includes memory which requires refreshing, but can not achieve such refreshing in the four 8 MHz clock cycles as described above. One example of such a device is a separate processor card with its own memory coupled to the Figure 1 system through an I/O channel. This device is

made responsive to the -MEMR signal to generate an IOCHRDY signal as shown in Figure 3. As can be seen, this signal extends over a further 8 MHz cycle after the first four cycles. As shown in Figure 2, this signal is applied to AND gate 21. Whilst IOCHRDY is in its low state, gate 21 can not pass the high signal from output Q2 to input D3. Thus this Q2 signal, which controls the return of the -REFRESH and -MEMR signals to their inactive state, is not passed to the D3 input of circuit 22 until IOCHRDY goes high. This provides a one cycle delay as shown by the dotted -REFRESH, SA0-7 and -MEMR waveforms. Accordingly, an extra clock cycle period is provided to ensure that the memory in the channel device is refreshed.

As has been mentioned above, the Figure 2 circuit effects a refresh cycle in response to each pulse from timer 6, which pulses occur at 15 μ sec. intervals. This timing is selected to ensure that each memory row is refreshed once every 4 m sec. This is a typical refresh time requirement for DRAM's. Assuming each refresh cycle takes the full 5 cycles of the 8 MHz clock due to the IOCHRDY signal, then the total refresh overhead for the Figure 1 system is:

$$\frac{5 \times 256 \times 125.10^{-9}}{4.10^{-3}} \times 100 = 4\%$$

In other words, 4% of the total processing time of the system is devoted to memory refresh. If each refresh cycle, in the absence of IOCHRDY, takes only 4 cycles of the 8 MHz clock, then this figure reduces to 3.2%. These figures compare very favourably with that of a similar system employing DMA to effect memory refresh, in which the refresh overhead is approximately 12%.

In summary, what has been shown is a DRAM refresh system which is responsive to refresh timer inputs to develop a hold request signal to place a process in a hold state. In response to a hold acknowledge signal from the processor, the refresh system sequences to produce signals which make a refresh cycle look exactly like a memory read cycle. These signals are a refresh signal, from which are developed read address strobe signals, a memory read signal to control the system busses, and a parallel row address byte. A counter in the refresh circuit is incremented by one during each refresh cycle so that in successive refresh cycles, successive row addresses are delivered to the memory.

While the invention has been described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the scope of the invention as defined in the appended claims.

Claims

1. Refresh apparatus in or for a data processing

system which includes a processor (1) which, in response to a hold request (HRQ)—signal relinquishes control of its local bus and generated a hold acknowledge (HLDA)—signal, memory modules (3) which are address via a multiplexer (2) with row and column addresses supplies in parallel by the processor and require refreshing by row, and a direct memory access (DMA)—controller (not shown) having a DMA—clock input (4 MHz) derived from the system clock (8 MHz) and generating as required, latched hold request (LHRQ)—signals characterised by a refresh generator (5) inserted between said LHRQ—signal output of the DMA—controller and the HRQ—signal input of the processor and coupling directly to the memory modules and the DMA—clock input, comprising:

first logic means (14, 11, 10, 13) responsive the DMA—clock, inverted, and to a period signal from a refresh timer circuit (6) to generate said HRQ—signal for the processor in response to the timer, and otherwise passing any extant LHRQ—signal to the HRQ—signal input of the processor,

second logic means (16) responsive to said hold acknowledge signal (HLDA) from the processor to generate an inverted refresh control signal (REFR),

third logic means (18) responsive to said inverted refresh control signal (REFR), to provide a refresh signal (REFR) to control memory row access,

a counter circuit (19) coupled to be incremented by one in response to each refresh control signal, and

a sequencer circuit (20, 21, 22) responsive to each refresh control signal to generate a first gating signal (on 23) to gate the current count in the counter circuit, representing a memory row address, to the memory and thereafter to generate a second gating signal (at -Q2) to generate a memory read signal (MEMR) and to reset said memory read signal.

2. Refresh apparatus according to claim 1 in which the first logic means includes flip-flop (14, 11) responsive to the periodic signal to provide the HRQ—signal until reset.

3. Refresh apparatus according to claim 1 in which the second logic means comprises an AND gate (16) coupled to receive the HRQ—signal, the HLDA—signal from the processor and a further signal (from 15) derived from the periodic signal to generate the REFR—signal.

4. Refresh apparatus according to claim 1 in which the counter circuit includes a counter incremented by the REFR—signal and having its output coupled to a register circuit responsive to the first gating signal to gate out its content.

5. Refresh apparatus according to claim 1 in which the sequencer circuit comprises a sequence of flip-flop circuits, with an output of each, except the last, coupled to the input of the following flip-flop.

6. Refresh apparatus according to claim 5 in which the true output (Q1) of the first flip-flop in

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In other words, 4% of the total processing time of the system is devoted to memory refresh. If each refresh cycle, in the absence of IOCHRDY, takes only 4 cycles of the 8 MHz clock, then this figure reduces to 3.2%. These figures compare very favourably with that of a similar system employing DMA to effect memory refresh, in which the refresh overhead is approximately 12%.

In summary, what has been shown is a DRAM refresh system which is responsive to refresh timer inputs to develop a hold request signal to place a process in a hold state. In response to a hold acknowledge signal from the processor, the refresh system sequences to produce signals which make a refresh cycle look exactly like a memory read cycle. These signals are a refresh signal, from which are developed read address strobe signals, a memory read signal to control the system busses, and a parallel row address byte. A counter in the refresh circuit is incremented by one during each refresh cycle so that in successive refresh cycles, successive row addresses are delivered to the memory.

While the invention has been described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the scope of the invention as defined in the appended claims.

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first logic means (14, 11, 10, 13) responsive the DMA—clock, inverted, and to a period signal from a refresh timer circuit (6) to generate said HRQ—signal for the processor in response to the timer, and otherwise passing any extant LHRQ—signal to the HRQ—signal input of the processor,

second logic means (16) responsive to said hold acknowledge signal (HLDA) from the processor to generate an inverted refresh control signal (REFR),

third logic means (18) responsive to said inverted refresh control signal (REFR), to provide a refresh signal (REFR) to control memory row access,

a counter circuit (19) coupled to be incremented by one in response to each refresh control signal, and

a sequencer circuit (20, 21, 22) responsive to each refresh control signal to generate a first gating signal (on 23) to gate the current count in the counter circuit, representing a memory row address, to the memory and thereafter to generate a second gating signal (at -Q2) to generate a memory read signal (MEMR) and to reset said memory read signal.

2. Refresh apparatus according to claim 1 in which the first logic means includes flip-flop (14, 11) responsive to the periodic signal to provide the HRQ—signal until reset.

3. Refresh apparatus according to claim 1 in which the second logic means comprises an AND gate (16) coupled to receive the HRQ—signal, the HLDA—signal from the processor and a further signal (from 15) derived from the periodic signal to generate the REFR—signal.

4. Refresh apparatus according to claim 1 in which the counter circuit includes a counter incremented by the REFR—signal and having its output coupled to a register circuit responsive to the first gating signal to gate out its content.

5. Refresh apparatus according to claim 1 in which the sequencer circuit comprises a sequence of flip-flop circuits, with an output of each, except the last, coupled to the input of the following flip-flop.

6. Refresh apparatus according to claim 5 in which the true output (Q1) of the first flip-flop in



the sequence is coupled to the input (D3) of the second flip-flop in the sequence, and the complement output (-Q1) of the first flip-flop provides the first gating signal.

7. Refresh apparatus according to claim 6 in which the true output (Q2) of the second flip-flop is coupled to the input (D3) of the third flip-flop in the sequence, and the complement output (-Q2) of the second flip-flop provides the second gating signal.

8. Refresh apparatus according to claim 7 in which the complement output (-Q3) of the third flip-flop is coupled to the input (D4) of the fourth flip-flop in the sequence and the true output (Q3) of the third flip-flop is applied to an AND gate (20), which couples the REFR-signal to the input of the first flip-flop, to disable this AND gate when high.

9. Refresh apparatus according to claim 8 in which the true output (Q4) of the fourth flip-flop is coupled (to 14) to clear the HRQ-signal when high.

10. Refresh apparatus according to claim 7 wherein the true output (Q2) of the second flip-flop is coupled to the input (D3) of the third flip-flop of the sequence via an AND gate enabled by signal (IOCHRDY) indicating that a remote memory that requires refreshing is so refreshed.

Patentansprüche

1. Auffrischungs-vorrichtung in einer oder für eine Datenverarbeitungsanlage, die einen Prozessor (1), der auf ein Halteanforderungs(HRQ)-Signal ansprechend die Steuerung seines lokalen Bus aufgibt und eine Haltebestätigung(HLDA)-Signal erzeugt, Speicherbausteine (3), die über einen Multiplexer (2) mit Zeilen- und Spaltenadressen adressiert werden, die parallel vom Prozessor geliefert werden und reihenweise aufgefrischt werden müssen, und einen Direktspeicherzugriffs(DMA)-Steuerteil (nicht dargestellt) umfaßt, der einen DMA-Eingangstakt (4 MHz) der aus dem Systemtakt (8 MHz) abgeleitet wird, aufweist und, auf Anforderung verriegelte Halteanforderungs(LRHQ)-Signale erzeugt, gekennzeichnet durch einen Auffrischungsgenerator (5), der zwischen dem LHRQ-Signalausgang des DMA-Steuerteils und dem HRQ-Signal-Eingang des Prozessors liegt und direkt mit den Speicherbausteinen und dem DMA-Eingangstakt gekoppelt ist, und

eine erste logische Einrichtung (14, 11, 10, 13), die auf den invertierten DMA-Takt und auf ein periodisches Signal von einer Auffrischungszeitgeberschaltung (6) anspricht, um das HRQ-Signal für den Prozessor auf den Zeitgeber ansprechend zu erzeugen und sonst irgendein vorhandenes LHRQ-Signal zum HRQ-Signaleingang des Prozessors durchläßt,

eine zweite logische Einrichtung (16), die auf das Haltebestätigungssignal (HLDA) vom Prozessor anspricht, um ein invertiertes Auffrischungssteuersignal (REFR) zu erzeugen,

eine dritte logische Einrichtung (18), die auf das

invertierte Auffrischungssteuersignal (REFR) anspricht, um ein Auffrischungssignal (REFR) zum Steuern des Speicherzeilenzugriffes zu erzeugen,

eine Zäblerschaltung (19), die so geschaltet ist, daß sie auf jedes Auffrischungssteuersignal ansprechend um Eins aufzählt, und

eine Zuordnungsschaltung (20, 21, 22) umfaßt, die auf jedes Auffrischungssteuersignal anspricht, um ein erste Gattersignal (auf 23) zu erzeugen, um den laufenden Zählerstand in der Zälerschaltung, der eine Speicherzeilenadresse wiedergibt, zu dem Speicher zu leiten, und danach ein zweites Gattersignal (bei -Q2) zu erzeugen, um ein Speicherlesesignal (MEMR) zu erzeugen und das Speicherlesesignal rückzusetzen.

2. Auffrischungs-vorrichtung nach Anspruch 1, bei der die erste logische Einrichtung eine Flip-Flop-Einrichtung (14, 11) einschließt, die auf das periodische Signal ansprechen, um das HRQ-Signal bis zum Rücksetzen zu liefern.

3. Auffrischungs-vorrichtung nach Anspruch 1, bei der die zweite logische Einrichtung ein UND-Glied (16) umfaßt, das so geschaltet ist, daß es das HRQ-Signal, das HLDA-Signal vom Prozessor und ein weiteres Signal (von 15) empfängt, das vom periodischen Signal abgeleitet wird, um daß REFR-Signal zu erzeugen.

4. Auffrischungs-vorrichtung nach Anspruch 1, bei der die Zälerschaltung einen Zähler enthält, der durch das REFR-Signal aufzählt und mit seinem Ausgang mit einer Registerschaltung gekoppelt ist, die auf das erste Gattersignal anspricht, um seinen Inhalt herauszuleiten.

5. Auffrischungs-vorrichtung nach Anspruch 1, bei der die Zuordnungsschaltung einer Folge von Flip-Flop-Schaltungen umfaßt, die jeweils außer der letzten mit einem Ausgang mit dem Eingang des folgenden Flip-Flops verbunden sind.

6. Auffrischungs-vorrichtung nach Anspruch 5, bei der der wahre Ausgang (Q1) des ersten Flip-Flops in der Folge mit dem Eingang (D3) des zweiten Flip-Flops in der Folge verbunden ist und der komplementäre Ausgang (-Q1) des ersten Flip-Flops das erste Gattersignal liefert.

7. Auffrischungs-vorrichtung nach Anspruch 6, bei der der wahre Ausgang (Q2) des zweiten Flip-Flops mit dem Eingang (D3) des dritten Flip-Flops in der Folge verbunden ist und der komplementäre Ausgang (-Q2) des zweiten Flip-Flops das zweite Gattersignal liefert.

8. Auffrischungs-vorrichtung nach Anspruch 7, bei der der komplementäre Ausgang (-Q3) des dritten Flip-Flops mit dem Eingang (D4) des vierten Flip-Flops in der Folge verbunden ist und das wahre Ausgangssignal des dritten Flip-Flops an einem UND-Glied (20) liegt, das das REFR-Signal an den Eingang des ersten Flip-Flops legt, um diese UND-Glied zu sperren, wenn es einen hohen Pegel hat.

9. Auffrischungs-vorrichtung nach Anspruch 8, bei der der wahre Ausgang (Q4) des vierten Flip-Flops so geschaltet ist (an 14), daß das HRQ-Signal gelöscht wird, wenn er einen hohen Pegel hat.



10. Auffrischungs Vorrichtung nach Anspruch 7, bei der der wahre Ausgang (Q2) des zweiten Flip-Flops mit dem Eingang (D3) des dritten Flip-Flops in der Folge über ein UND-Glied verbunden ist, das durch ein Signal (IOCHRDY) durchgeschaltet wird, das anzeigt, daß ein entfernter Speicher, der ein Auffrischen benötigt, so aufgefrischt wird.

Revendications

1. Un dispositif de rafraîchissement, incorporé ou destiné à un système informatique comportant un processeur (1) qui, en réponse à un signal HRQ de requête de suspension, renonce au contrôle de son bus local et produit un signal HLDA d'accusé de réception de suspension, des modules de mémoire (3) qui sont adressés, via un multiplexeur (2), par des adresses de rangée et de colonne appliquées en parallèle par le processeur et qui ont besoin d'un rafraîchissement rangée par rangée, ainsi qu'un contrôleur DMA d'accès direct à la mémoire (non représentée) pourvu d'une entrée d'horloge DMA (4 MHz) dérivée de l'horloge système (8 MHz) et produisant à volonté des signaux verrouillés LHRQ de requête de suspension, caractérisé par un générateur de rafraîchissement (5):

—inséré entre la sortie du signal LHRQ du contrôleur DMA et l'entrée du signal HRQ du processeur, et relié directement aux modules de mémoire et à l'entrée d'horloge DMA,

—et comportant:

des premiers moyens logiques (14, 11, 10, 13), fonctionnant en réponse à l'horloge DMA inversée et à un signal périodique provenant d'un circuit temporisateur de rafraîchissement (6) de manière à produire, en réponse au temporisateur, le signal HRQ destiné au processeur et, dans le cas contraire, à transférer vers l'entrée de signal HRQ du processeur tout signal LHRQ présent,

des seconds moyens logiques (16), fonctionnant en réponse au signal HLDA d'accusé de réception de suspension en provenance du processeur de manière à produire un signal de contrôle de rafraîchissement inversé —REFR,

des troisièmes moyens logiques (18), fonctionnant en réponse à ce signal de contrôle de rafraîchissement inversé —REFR de manière à produire un signal de rafraîchissement REFR permettant de contrôler l'accès aux rangées de mémoire,

un circuit de comptage (19), relié de manière à pouvoir être incrémenté d'une unité en réponse à chaque signal de contrôle de rafraîchissement, et

un circuit séquenceur (20, 21, 22) fonctionnant en réponse à chaque signal de contrôle de rafraîchissement de manière à produire un premier signal d'ouverture de porte (sur 23) permettant de laisser passer vers la mémoire la valeur de compte courante se trouvant dans le circuit compteur, qui représente une adresse de rangée de la mémoire, puis de produire ensuite un second signal d'ou-

verture de porte (en —Q2) afin de produire un signal de lecture de la mémoire —MEMR et remettre à son état initial ce signal de lecture de la mémoire.

2. Le dispositif de rafraîchissement de la revendication 1, dans lequel les premiers moyens logiques comportent des moyens bistables (14, 11) fonctionnant en réponse au signal périodique afin de délivrer le signal HRQ jusqu'à remise à l'état initial.

3. Le dispositif de rafraîchissement de la revendication 1, dans lequel les seconds moyens logiques comportent une porte ET (16) disposée de manière à recevoir le signal HRQ, le signal HLDA en provenance du processeur ainsi qu'un autre signal (provenant de 15) dérivé du signal périodique, pour produire le signal REFR.

4. Le dispositif de rafraîchissement de la revendication 1, dans lequel le circuit de comptage comporte un compteur incrémenté par le signal REFR, et dont la sortie est reliée à un circuit à registre fonctionnant en réponse au premier signal d'ouverture de porte pour en laisser sortir le contenu.

5. Le dispositif de rafraîchissement de la revendication 1, dans lequel le circuit séquenceur comporte une série de circuits bistables dont chacun, à l'exception du dernier, possède une sortie reliée à l'entrée du bistable suivante.

6. Le dispositif de rafraîchissement de la revendication 1, dans lequel la sortie vraie (Q1) du premier bistable de la série est reliée à l'entrée (D3) du second bistable de la série, l'entrée complémentée (—Q1) du premier bistable donnant le premier signal d'ouverture de porte.

7. Le dispositif de rafraîchissement de la revendication 1, dans lequel la sortie vraie (Q2) du second bistable est reliée à l'entrée (D3) du troisième bistable de la série, la sortie complémentée (—Q2) du second bistable donnant le second signal d'ouverture de porte.

8. Le dispositif de rafraîchissement de la revendication 1, dans lequel la sortie complémentée (—Q3) du troisième bistable est reliée à l'entrée (D4) du quatrième bistable de la série et la sortie vraie (Q3) du troisième bistable est appliquée à une porte ET (20) qui applique le signal REFR à l'entrée du premier bistable afin de désactiver cette porte ET lorsqu'il est au niveau haut.

9. Le dispositif de rafraîchissement de la revendication 1, dans lequel la sortie vraie (Q4) du quatrième bistable est appliquée (à 14) de manière à effacer le signal HRQ lorsqu'il est au niveau haut.

10. Le dispositif de rafraîchissement de la revendication 1, dans lequel la sortie vraie (Q2) du second bistable est reliée à l'entrée D3 du troisième bistable de la série via une porte ET activée par un signal (IOCHRDY) indiquant que l'on rafraîchit de cette manière une mémoire distante nécessitant un rafraîchissement.

