ABSTRACT

METHOD OF FABRICATING A MOSFET DEVICE USING A SPIKE RAPID THERMAL OXIDATION PROCEDURE

A method of forming a conductive gate structure on an underlying gate insulator layer, without the use of a plasma dry etch conductive gate definition procedure, has been developed. After formation of source/drain extension (SDE) and heavily doped source/drain regions, an opening is formed in a planarized dielectric layer exposing the top surface of a semiconductor alloy layer, or exposing the top surface of a semiconductor substrate, while the planarized dielectric layer and adjacent insulator spacers overlay the source/drain regions. A multiple spike, rapid thermal oxidation (RTO) procedure is employed to grow a gate insulator layer on the region of semiconductor alloy, or semiconductor, exposed in the opening, with the low temperature RTO procedure, and the planarized dielectric layer overlying the source/drain regions, suppressing out diffusion of SDE dopants. A conductive layer is next deposited and then planarized via a chemical mechanical polishing procedure, resulting in the definition of a conductive gate structure on the gate insulator layer, with the conductive gate structure formed without employment of plasma dry etching eliminating the risk of plasma induced damage of the gate insulator layer.