NON-ETCH BACK SOG PROCESS FOR HOT ALUMINUM METALLIZATIONS

ABSTRACT

A process has been developed in which planar, multilevel metallizations, are used to fabricate semiconductor devices. The process features initially forming tall, narrow photoresist plugs, and filling the spaces between photoresist plugs with a planarizing layer of a composite dielectric, which includes a spin on glass layer. Removal of the photoresist plug results in the creation of a narrow via hole. The composite dielectric was deposited by initially using a non-porous, silicon oxide layer, followed by the planarizing spin on glass layer. Therefore metal via fills will interface the non-porous, silicon oxide layer.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)