CLAIMS

1. A ~~P~~process for transferring a thin layer ~~(5)~~ to a carrier substrate ~~(1)~~, comprising the following steps:
- preparing a carrier substrate ~~(1)~~ using a preparation process comprising the provision of a base substrate ~~(3)~~ that has, on a main face, a charge-trapping layer ~~(2)~~ and the formation of a dielectric layer ~~(4)~~ having a thickness greater than 200 nm on the charge-trapping layer ~~(2)~~, the formation of the dielectric layer ~~(4)~~ simultaneously implementing the deposition and the ion sputtering of the dielectric layer;

- joining, by means of molecular bonding and without preparing the free face of the dielectric layer ~~(4)~~ by polishing, a donor substrate to the dielectric layer ~~(4)~~ of the carrier substrate ~~(1)~~, the donor substrate featuring a weakened plane defining the thin layer ~~(5)~~;
- splitting the donor substrate at the weakened plane so as to release the thin layer ~~(5)~~ and transfer it to the carrier substrate ~~(1)~~.

2. The ~~P~~process according to ~~the preceding~~ claim 1, wherein the preparation process comprises the formation of a bow compensation layer ~~(32)~~ on a back face of the base substrate ~~(3)~~, opposite the main face.

3. The ~~P~~process according to ~~the preceding~~ claim 2, wherein the bow compensation layer ~~(32)~~ has a thickness of between 500 nm and 1000 nm.

4. The ~~P~~process according to one of the preceding claims, wherein the base substrate ~~(3)~~ is a monocrystalline silicon substrate exhibiting a resistivity higher than 600 ohm.cm.

5. The ~~P~~process according to one of the preceding claims, wherein the charge-trapping layer ~~(2)~~ comprises polycrystalline silicon.

6. The ~~P~~process according to one of the preceding claims, wherein
the charge-trapping layer ~~(2)~~ comprises carbon.

7. The ~~P~~process according to one of the preceding claims, wherein
the charge-trapping layer ~~(2)~~ has a thickness of between 1 micron and 20 microns.

8. The ~~P~~process according to one of the preceding claims, wherein
the dielectric layer ~~(4)~~ consists of silicon oxide.

9. The ~~P~~process according to one of the preceding claims, wherein
the dielectric layer ~~(4)~~ comprises a barrier layer made of silicon nitride or of silicon oxynitride.

10. The ~~P~~process according to one of the preceding claims, wherein the dielectric layer ~~(4)~~ has a thickness of between 200 nm and 10 microns, and preferably between 600 nm and 10 microns.

11. The ~~P~~process according to one of the preceding claims, wherein the deposition/sputtering ratio is between 1 and 10, preferably between 2 and 5.

12. The ~~P~~process according to one of the preceding claims, wherein the dielectric layer ~~(4)~~ is formed at a temperature of between 300°C and 450°C, preferably between 350°C and 400°C.

13. The ~~P~~process according to one of the preceding claims, wherein the dielectric layer ~~(4)~~ is formed in an atmosphere exhibiting a pressure lower than atmospheric pressure.

14. The ~~P~~process according to one of the preceding claims, further comprising an operation of annealing the dielectric layer ~~(4)~~ in a neutral atmosphere and at a temperature exceeding the temperature of formation of the dielectric layer, preferably lower than 950°C.

15. The ~~P~~process according to one of the preceding claims, wherein the free face of the dielectric layer ~~(4)~~ exhibits a roughness lower than 0.5 nm in terms of RMS value over a field of measurement of 10 microns by 10 microns.

16. The ~~P~~process according to one of the preceding claims, wherein the donor substrate is devoid of any dielectric surface layer.