INTERPOSER FOR RECESSED FLIP-CHIP PACKAGE

Abstract:

The specification describes a recessed chip IC package in which the IC chip is bonded to a silicon translator, and power and ground planes for IC power and ground interconnections are formed on separate interconnect levels of the translator. The multilevel interconnection capability of the translator allows crossovers, and allows power and ground pins from the IC chip to be both isolated from signal I/Os, and consolidated into fewer interconnections going to the next board level. The thermal mismatch between the silicon translator and conventional printed wiring board materials is addressed by using an interposer which is essentially a ball grid array of plated-through holes that transfers the interconnect pattern from the translator to the printed wiring board. The interposer may have a composition with a coefficient of thermal expansion (CTE) that lies between the CTE of silicon and the CTE of the board material. It may also be provided with holes or slots for additional stress relief.

This Sheet Has Been Replaced

