PULSED VOLTAGE BOOST FOR SUBSTRATE PROCESSING

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to a system used in semiconductor device manufacturing. More specifically, embodiments of the present disclosure relate to a plasma processing system used to process a substrate.

Description of the Related Art

[0002] Reliably producing high aspect ratio features is one of the key technology challenges for the next generation of semiconductor devices. One method of forming high aspect ratio features uses a plasma-assisted etching process in which a plasma is formed in a processing chamber and ions from the plasma are accelerated towards a surface of a substrate to form openings in a material layer disposed beneath a mask layer formed on the surface of the substrate.

[0003] In a typical plasma-assisted etching process, the substrate is positioned on a substrate support disposed in a processing chamber, a plasma is formed over the substrate, and ions are accelerated from the plasma towards the substrate across a plasma sheath, i.e., region depleted of electrons, formed between the plasma and the surface of the substrate.

[0004] It has been found that pulsing techniques have to periodically and suddenly consume a large amount of plasma generated bulk electrons to establish the DC bias, and the amount of bulk electrons consumed is often on the order of the number of free electrons found in the generated plasma. Therefore, the consumption of bulk electrons cause severe perturbation to plasma stability and sometimes cause the plasma to extinguish. As an example, assume a plasma processing system has a plasma density of 5e10cm^{-3}, gap of 2cm (1 inch gap minus sheath thickness, about 0.5 cm) and wafer diameter of 30cm. In such a system, the total available electrons in the volume above the wafer is 7e13. Further assume a sheath capacitance of 200pF and sheath voltage of 8000V (typical for high aspect ratio etch applications). The number of electrons used to charge the wafer surface is about 1e13. So in about tens of nanoseconds, about 15 percent of the bulk electrons is drawn from the plasma to establish the DC bias. This consumption repeats at the pulsing frequency, which may be around 400kHz. The bulk

electron consumption is a significant perturbation to plasma sustainability and stability. This scenario may only worsen with the evolving processes using higher ion energies. During processing, variations in the plasma created by plasma instability will affect the with-in-wafer (WIW) and wafer-to-wafer (WTW) process performance, and thus device yield and other related process results.

[0005] Accordingly, there is a need in the art for plasma processing and biasing methods that are able to provide desirable plasma-assisted etching process results.

SUMMARY

[0006] Embodiments provided herein generally include apparatus, plasma processing systems and methods for generation of a waveform for plasma processing of a substrate in a processing chamber.

[0007] One embodiment of the present disclosure is directed to a plasma processing system. The plasma processing system generally includes a processing chamber, a plurality of switches, an electrode disposed in the processing chamber, a voltage source, and a capacitive element. The voltage source is selectively coupled to the electrode via one of the plurality of switches. The capacitive element is selectively coupled to the electrode via one of the plurality of switches. The capacitive element and the voltage source are coupled to the electrode in parallel. The plurality of switches are configured to couple the capacitive element and the voltage source to the electrode during a first phase, couple the capacitive element and the electrode to a ground node during a second phase, and couple the capacitive element to the electrode during a third phase.

[0008] One embodiment of the present disclosure is directed to a method of processing a substrate. The method generally includes coupling a capacitive element and a voltage source to an electrode disposed within a processing chamber during a first phase, where the capacitive element and the voltage source are coupled to the electrode in parallel. The method also includes coupling the capacitive element and the electrode to a ground node during a second phase. The method further includes coupling the capacitive element to the electrode during a third phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above -recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope and may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic cross-sectional view of a processing system, according to one or more embodiments, configured to practice the methods set forth herein.

[0011] Figure 2A shows a voltage waveform that may be applied to an electrode of a processing chamber, according to one or more embodiments.

[0012] Figure 2B shows a voltage waveform that is established on a substrate due to a voltage waveform applied to an electrode of a processing chamber.

[0013] Figure 3 illustrates an example ion energy distribution (IED).

[0014] Figure 4 illustrates a functionally equivalent, simplified electrical circuit of a plasma processing system that may establish a voltage boost at an electrode, in accordance with certain embodiments of the present disclosure

[0015] Figure 5 is a timing diagram illustrating state of switches of the plasma processing system, in accordance with certain embodiments of the present disclosure.

[0016] Figures 6A-6C are circuit diagrams illustrating the states of the switches during corresponding phases depicted in Figure 5, in accordance with certain embodiments of the present disclosure

[0017] Figure 7 is a process flow diagram illustrating a method for establishing a boost voltage at an electrode.

[0018] Figure 8A shows an additional voltage waveform that may be established at an electrode of a processing chamber, in accordance with certain embodiments of the present disclosure.

[0019] Figure 8B shows an additional voltage waveform that is established on a substrate due to a voltage waveform applied to an electrode of a processing chamber.

[0020] Figure 9 is an additional functionally equivalent, simplified electrical circuit of a plasma processing system, in accordance with certain embodiments of the present disclosure.

[0021] Figure 10 is an additional functionally equivalent, simplified electrical circuit of a plasma processing system with a separate voltage source for a boost capacitor, in accordance with certain embodiments of the present disclosure.

[0022] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements disclosed in one aspect may be beneficially utilized on other aspects without specific recitation.

DETAILED DESCRIPTION

[0023] With technology node advancing towards 2nm, fabrication of smaller features with larger aspect ratios involve atomic precision for plasma processing. For etching processes where the plasma ions play an important role, ion energy control is challenging the semiconductor equipment industry. Traditionally, RF biased techniques use a sinusoidal wave to excite plasma and accelerate ions.

[0024] Some embodiments of the present disclosure are generally directed to techniques and apparatus that use the concept of a charge pump to increase wafer surface voltage without or reduced consumption of plasma electrons. In certain aspects, the electrons from an external circuit (such as a capacitive element coupled in parallel with the electrode of the processing chamber) may be used to boost the DC bias at the electrode. The techniques and apparatus for boosting the DC bias at the electrode described herein may reduce the load to plasma electrons and/or facilitate higher energy substrate processing operations.

Plasma Processing System Examples

[0025] Figure 1 is a schematic cross-sectional view of a plasma processing system 10 configured to perform one or more of the plasma processing methods set forth

herein. In some embodiments, the processing system 10 is configured for plasma-assisted etching processes, such as a reactive ion etch (RIE) plasma processing. However, it should be noted that the embodiments described herein may be also be used with processing systems configured for use in other plasma-assisted processes, such as plasma-enhanced deposition processes, for example, plasma-enhanced chemical vapor deposition (PECVD) processes, plasma-enhanced physical vapor deposition (PEPVD) processes, plasma-enhanced atomic layer deposition (PEALD) processes, plasma treatment processing or plasma-based ion implant processing, for example, plasma doping (PLAD) processing.

[0026] As shown, the processing system 10 is configured to form a capacitively coupled plasma (CCP), where the processing chamber 100 include an upper electrode (e.g., chamber lid 123) disposed in a processing volume 129 facing a lower electrode (e.g., the substrate support assembly 136) also disposed in the processing volume 129. In a typical capacitively coupled plasma (CCP) processing system, a radio frequency (RF) source is electrically coupled to one of the upper or lower electrode delivers an RF signal configured to ignite and maintain a plasma (e.g., the plasma 101), which is capacitively coupled to each of the upper and lower electrodes and is disposed in a processing region therebetween. Typically, the opposing one of the upper or lower electrodes is coupled to ground or to a second RF power source for additional plasma excitation. As shown, the processing system 10 includes a processing chamber 100, a support assembly 136, and a system controller 126.

[0027] The processing chamber 100 typically includes a chamber body 113 that includes the chamber lid 123, one or more sidewalls 122, and a chamber base 124, which collectively define the processing volume 129. The one or more sidewalls 122 and chamber base 124 generally include materials that are sized and shaped to form the structural support for the elements of the processing chamber 100 and are configured to withstand the pressures and added energy applied to them while a plasma 101 is generated within a vacuum environment maintained in the processing volume 129 of the processing chamber 100 during processing. In one example, the one or more sidewalls 122 and chamber base 124 are formed from a metal, such as aluminum, an aluminum alloy, or a stainless steel alloy.

[0028] A gas inlet 128 disposed through the chamber lid 123 is used to deliver one or more processing gases to the processing volume 129 from a processing gas source 119 that is in fluid communication therewith. A substrate 103 is loaded into, and removed from, the processing volume 129 through an opening (not shown) in one of the one or more sidewalls 122, which is sealed with a slit valve (not shown) during plasma processing of the substrate 103.

[0029] In some embodiments, a plurality of lift pins (not shown) movably disposed through openings formed in the substrate support assembly 136 are used to facilitate substrate transfer to and from a substrate supporting surface 105A. In some embodiments, the plurality of lift pins 132 are disposed above and are coupled to and/or are engageable with a lift pin hoop (not shown) disposed in the processing volume 129. The lift pin hoop may be coupled to a shaft (not shown) that sealingly extends through the chamber base 124. The shaft may be coupled to an actuator (not shown) that is used to raise and lower the lift pin hoop. When the lift pin hoop is in a raised position, it engages with the plurality of lift pins 132 to raise the upper surfaces of the lift pins above the substrate supporting surface 105A, lifting the substrate 103 therefrom and enabling access to a non-active (backside) surface the substrate 103 by a robot handler (not shown). When the lift pin hoop is in a lowered position, the plurality of lift pins 132 are flush with or recessed below the substrate supporting surface 105A, and the substrate 103 rests thereon.

[0030] The system controller 126, also referred to herein as a processing chamber controller, includes a central processing unit (CPU) 133, a memory 134, and support circuits 135. The system controller 126 is used to control the process sequence used to process the substrate 103, including the substrate biasing and/or voltage boosting method(s) described herein. The CPU 133 is a general-purpose computer processor configured for use in an industrial setting for controlling the processing chamber and sub-processors related thereto. The memory 134 described herein, which is generally non-volatile memory, may include random access memory, read-only memory, floppy or hard disk drive, or other suitable forms of digital storage, local or remote. The support circuits 135 are conventionally coupled to the CPU 133 and comprise cache, clock circuits, input/output subsystems, power supplies, and the like, and combinations thereof. Software instructions (program) and data can be coded and stored within the

memory 134 for instructing a processor within the CPU 133. A software program (or computer instructions) readable by CPU 133 in the system controller 126 determines which tasks are performable by the components in the processing system 10.

[0031] Typically, the program, which is readable by CPU 133 in the system controller 126, includes code, which, when executed by the processor (CPU 133), performs tasks relating to the plasma processing schemes described herein. The program may include instructions that are used to control the various hardware and electrical components within the processing system 10 to perform the various process tasks and various process sequences used to implement the methods described herein. In one embodiment, the program includes instructions that are used to perform one or more of the operations described below in relation to Figure 7.

[0032] The plasma control system generally includes a first source assembly 196 for establishing at least a first pulsed voltage (PV) waveform at a bias electrode 104 (on a complex load as depicted in Figure 4), and a second source assembly 197 for establishing at least a second PV waveform at an edge control electrode 115. The first PV waveform or the second PV waveform may be generated using one or more components (e.g., PV sources) within a waveform generator assembly 150, which may correspond to a voltage source and/or current source as described in more detail herein with respect to Figure 4. In some embodiments, the waveform generator delivers an RF signal to the support base 107 (e.g., power electrode or cathode) and/or bias electrode 104 which may be used to generate (maintain and/or ignite) a plasma 101 in a processing region disposed between the substrate support assembly 136 and the chamber lid 123. In some embodiments, as shown in Figure 1, a separate waveform generator assembly 150 within a third source assembly 198 includes at least an RF source that is configured to deliver an RF signal to the support base 107 (e.g., power electrode or cathode).

[0033] The applied RF signal provided from the first source assembly 196, the second source assembly 197 or the third source assembly 198 may be configured to generate (maintain and/or ignite) a plasma 101 in a processing region disposed between the substrate support assembly 136 and the chamber lid 123. In some embodiments, the RF signal is used to ignite and maintain a processing plasma 101 using the processing gases disposed in the processing volume 129 and fields

generated by the RF power (RF signal) delivered to the support base 107 and/or bias electrode 104. In some aspects, the RF signal may be generated by an RF source (not shown) disposed within the waveform generator assembly 150. The processing volume 129 is fluidly coupled to one or more dedicated vacuum pumps through a vacuum outlet 120, which maintain the processing volume 129 at sub-atmospheric pressure conditions and evacuate processing and/or other gases, therefrom. In some embodiments, the substrate support assembly 136, disposed in the processing volume 129, is disposed on a support shaft 138 that is grounded and extends through the chamber base 124. In some embodiments, the RF signal generator may be configured to deliver an RF signal having a frequency that is greater than 40 MHz, such as between about 40 MHz and about 200 MHz.

[0034] In some embodiments, a capacitive element 152 may be selectively coupled to the bias electrode 104 and/or the support base 107, as further described herein with respect to Figure 4. In certain cases, the capacitive element 152 may be electrically coupled to the bias electrode 104 and/or the support base 107 via the power delivery line 157. The capacitive element 152 may provide a voltage boost during ESC recharge stage to reduce the bulk electrons consumed from the plasma. The voltage boost may reduce or prevent the perturbation to plasma sustainability and stability caused by the consumption of bulk electrons from the plasma.

[0035] The substrate support assembly 136, as briefly discussed above, generally includes the substrate support 105 (e.g., an electrostatic chuck (ESC) substrate support) and support base 107. In some embodiments, the substrate support assembly 136 can additionally include an insulator plate 111 and a ground plate 112, as is discussed further below. The support base 107 is electrically isolated from the chamber base 124 by the insulator plate 111, and the ground plate 112 is interposed between the insulator plate 111 and the chamber base 124. The substrate support 105 is thermally coupled to and disposed on the support base 107. In some embodiments, the support base 107 is configured to regulate the temperature of the substrate support 105, and the substrate 103 disposed on the substrate support 105, during substrate processing. In some embodiments, the support base 107 includes one or more cooling channels (not shown) disposed therein that are fluidly coupled to, and in fluid communication with, a coolant source (not shown), such as a refrigerant source or

water source having a relatively high electrical resistance. In some embodiments, the substrate support 105 includes a heater (not shown), such as a resistive heating element embedded in the dielectric material thereof. Herein, the support base 107 is formed of a corrosion-resistant thermally conductive material, such as a corrosion-resistant metal, for example aluminum, an aluminum alloy, or a stainless steel and is coupled to the substrate support with an adhesive or by mechanical means.

[0036] Typically, the substrate support 105 is formed of a dielectric material, such as a bulk sintered ceramic material, such as a corrosion-resistant metal oxide or metal nitride material, for example, aluminum oxide (Al_2O_3), aluminum nitride (AlN), titanium oxide (TiO), titanium nitride (TiN), yttrium oxide (Y_2O_3), mixtures thereof, or combinations thereof. In embodiments herein, the substrate support 105 further includes the bias electrode 104 embedded in the dielectric material thereof.

[0037] In one configuration, the bias electrode 104 is a chucking pole used to secure (i.e., chuck) the substrate 103 to the substrate supporting surface 105A of the substrate support 105 and to bias the substrate 103 with respect to the processing plasma 101 using one or more of the pulsed-voltage biasing schemes described herein. Typically, the bias electrode 104 is formed of one or more electrically conductive parts, such as one or more metal meshes, foils, plates, or combinations thereof.

[0038] In some embodiments, the bias electrode 104 is electrically coupled to a clamping network, which provides a chucking voltage thereto, such as static DC voltage between about -5000 V and about 5000 V, using an electrical conductor, such as the coaxial power delivery line 106 (e.g., a coaxial cable). As will be discussed further below, the clamping network includes a DC power supply 155 (e.g., a high voltage DC (HVDC) supply) and a filter 151 (e.g., a low-pass filter).

[0039] The substrate support assembly 136 may further include the edge control electrode 115 that is positioned below the edge ring 114 and surrounds the bias electrode 104 and/or is disposed a distance from a center of the bias electrode 104. In general, for a processing chamber 100 that is configured to process circular substrates, the edge control electrode 115 is annular in shape, is made from a conductive material, and is configured to surround at least a portion of the bias

electrode 104. In some embodiments, such as shown in Figure 1, the edge control electrode 115 is positioned within a region of the substrate support 105. In some embodiments, as illustrated in Figure 1, the edge control electrode 115 includes a conductive mesh, foil, and/or plate that is disposed a similar distance (i.e., Z-direction) from the substrate supporting surface 105A of the substrate support 105 as the bias electrode 104.

[0040] The edge control electrode 115 can be biased by use of a waveform generator assembly that is different from the waveform generator assembly 150, which is used to bias the bias electrode 104. In some embodiments, the edge control electrode 115 can be biased by use of a waveform generator assembly 150 that is also used to bias the bias electrode 104 by splitting part of the power to the edge control electrode 115. In one configuration, a first waveform generator assembly 150 of the first source assembly 196 is configured to bias the bias electrode 104, and a second waveform generator assembly 150 of a second source assembly 197 is configured to bias the edge control electrode 115.

[0041] In one embodiment, a power delivery line 157 electrically connects the output of the waveform generator assembly 150 of the first source assembly 196 to the bias electrode 104. While the discussion below primarily discusses the power delivery line 157 of the first source assembly 196, which is used to couple a waveform generator assembly 150 to the bias electrode 104, the power delivery line 158 of the second source assembly 197, which couples a waveform generator assembly 150 to the edge control electrode 115, will include the same or similar components. The electrical conductor(s) within the various parts of the power delivery line 157 may include: (a) one or a combination of coaxial cables, such as a flexible coaxial cable that is connected in series with a rigid coaxial cable, (b) an insulated high-voltage corona-resistant hookup wire, (c) a bare wire, (d) a metal rod, (e) an electrical connector, or (f) any combination of electrical elements in (a) – (e).

[0042] In some embodiments, the processing chamber 100 further includes the quartz pipe 110, or collar, that at least partially circumscribes portions of the substrate support assembly 136 to prevent the substrate support 105 and/or the support base 107 from contact with corrosive processing gases or plasma, cleaning gases or plasma, or byproducts thereof. Typically, the quartz pipe 110, the insulator plate 111,

and the ground plate 112 are circumscribed by a liner 108. In some embodiments, a plasma screen 109 is positioned between the cathode liner 108 and the sidewalls 122 to prevent plasma from forming in a volume underneath the plasma screen 109 between the liner 108 and the one or more sidewalls 122.

[0043] Figure 2A shows an example voltage waveform that may be established at an electrode (e.g., the bias electrode 104 and/or support base 107) of a processing chamber. Figure 2B illustrates an example of different types of voltage waveforms 225 and 230 established at a substrate due to different voltage waveforms, similar to the voltage waveform shown in Figure 2A, that are separately established at an electrode within the processing chamber. The waveforms include two stages: an ion current stage and a sheath collapse stage, as shown. At the beginning of the ion current stage, a drop in substrate voltage creates a high voltage sheath above the substrate, accelerating positive ions to the substrate. In aspects, the drop of the substrate voltage may be boosted using a capacitive element (e.g., the capacitive element 152) as a source for bulk electrons. The voltage boost may reduce the bulk electrons consumed from the plasma and improve the sustainability and stability of the plasma during the etching process.

[0044] The positive ions that bombard the surface of the substrate during the ion current stage deposit a positive charge on the substrate surface, which if uncompensated causes a gradually increasing substrate voltage during the ion current stage, as illustrated by voltage waveform 225 in Figure 2B. However, the uncontrolled accumulation of positive charge on the substrate surface undesirably gradually discharges the sheath and chuck capacitors, slowly decreasing the sheath voltage drop and bringing the substrate potential closer to zero, as illustrated by voltage waveform 225. The accumulation of positive charge results in the voltage droop in the voltage waveform established at the substrate (Figure 2B). However, a voltage waveform that is established at the electrode that has a negative slope during the ion current stage, as shown in Figure 2A, can be generated so as to establish a square shaped region (e.g., near zero slope) for an established substrate voltage waveform, as shown by curve 230 in Figure 2B. Implementing the slope in the waveform established at the electrode during the ion current stage may be referred to as ion current compensation. The voltage difference between the beginning and end of the

ion current phase determines an ion energy distribution function (IEDF) width. The greater the voltage difference, the wider the IEDF width. To achieve monoenergetic ions and a narrower IEDF width, operations are performed to flatten the substrate voltage waveform in the ion current phase using the ion current compensation. In some embodiments of the present disclosure, an RF signal is overlaid on the voltage waveform shown in Figure 2A.

[0045] Figure 3 is a graph illustrating an IED function (IEDF), in accordance with certain embodiments of the present disclosure. As shown, the IEDF includes a mono-energy peak 302 that may be produced using a specific waveform at the electrode during the ion current compensation stage. The energy associated with the energy peak may be less than a few hundred eVs (e.g., less 1K eV). In certain cases, the energy associated with the energy peak may be a few hundred eVs to tens of thousands eVs, depending on aspect ratio of the feature to be formed in substrate. For instance, in some cases, the energy associated with the energy peak may be between 4k eV to 10k eV. Some embodiments are directed to techniques for implementing the ion energy distribution shown in Figure 3 or other suitable ion energy distributions, for example, as depicted in Figure 8B.

Voltage Boost for Substrate Processing

[0046] Certain embodiments of the present disclosure are generally directed to techniques and apparatus for boosting the voltage at an electrode, such as a bias electrode (e.g., the bias electrode 104 depicted in Figure 1) and/or a support base (e.g., the support base 107 depicted in Figure 1), of a processing chamber. The voltage boost described herein may reduce the consumption of bulk electrons from the plasma and facilitate desirable plasma-assisted etching process results.

[0047] Figure 4 is a functionally equivalent, simplified electrical circuit 400 of a plasma processing system (e.g., the processing system 10) that may establish a voltage boost at an electrode, in accordance with certain embodiments of the present disclosure. As shown, the electrical circuit 400 may include switches 402a-402f (collectively referred to as switches 402 and labeled as S1-S6), a voltage source 404, a current source 406, a capacitive element 152, an equivalent capacitance of the substrate support 105 (labeled as C_{ESC}), an input node 408 (representative of the bias

electrode 104 and/or support base 107 in the processing chamber), and a complex load 410, which may be representative of a standard electrical plasma model as further described herein. In aspects, the processing may include a substrate support (e.g., the substrate support 105) that comprises a dielectric layer (e.g., the dielectric material of the substrate support 105) disposed over the electrode (e.g., the bias electrode 104 and/or support base 107).

[0048] In the electrical circuit 400, a voltage boost on the pulsed voltage from the voltage source 404 and/or current source 406 may be established at an electrode (which may be represented by the input node 408) using the capacitive element 152 during a portion of the process of establishing the waveform at the electrode, such as the waveform depicted in Figure 2A. The electrical circuit 400 illustrates a simplified model of the interaction among the waveform generator assembly (which may be represented by the voltage source 404 and/or current source 406), capacitive element 152, and certain elements (e.g., the substrate support and plasma) within the processing chamber 100, and generally illustrate the basic elements used during operation of the processing chamber 100. For clarity purposes, the following definitions are used throughout the present disclosure: (1) unless a reference is specified, all potentials are referenced to ground; (2) the voltage at any physical point (like a substrate or a biasing electrode) is likewise defined as the potential of this point with respect to ground (zero potential point); (3) the cathode sheath is implied to be an electron-repelling, ion-accelerating sheath that corresponds to a negative substrate potential with respect to plasma; (4) the sheath voltage (also referred to sometimes as “sheath voltage drop”), V_{sh}, is defined as the absolute value of the potential difference between the plasma and the adjacent surface (e.g. of the substrate or the chamber wall); and (5) the substrate potential is the potential at the substrate surface facing the plasma.

[0049] The complex load 410 is depicted as a standard electrical plasma model that represents the processing plasma 101 as three series elements. The first element being an electron-repelling cathode sheath (which sometimes may also be referred to as the “plasma sheath” or merely the “sheath”) adjacent to the substrate 103. The cathode sheath is represented by a conventional three-part circuit element comprising: (a) the diode D_{SH}, which when open represents the sheath collapse, (b) the current

source I_i, representing the ion current flowing to the substrate in the presence of the sheath, and (c) the capacitor C_{SH} (e.g., ~100-300 pF), which represents the sheath for the main portion of the biasing cycle (e.g., the ion current stage of the waveform depicted in Figure 2A), during which the ion acceleration and the etching occur. The second element being a bulk plasma, which is represented by a single resistor R_{plasma} (e.g., resistor 412 = ~ 5 – 10 Ohms). The third element being an electron-repelling wall sheath forming at the chamber walls. The wall sheath is likewise represented by a three-part circuit element comprising: (a) the diode D_{wall}, (b) the current source I_{iwall} representing the ion current to the wall, and (c) the capacitor C_{wall} (e.g., ~5 – 10 nF), which represents the wall sheath primarily during the ESC recharging phase of the waveform at the electrode. The interior surface of the grounded metal walls can also be coated with a thin layer of a dielectric material, which may provide a capacitance (not shown), such as ~300-1000nF, coupled in series between the complex load 410 and the ground node 414. The parasitic and stray capacitances of the ESC assembly (e.g., the substrate support 105) and the inductance of the ESC assembly may not be critical to the voltage boost scheme described herein and are not depicted in Figure 4. In certain cases, these factors (among others) may be considered in determining the values of certain electrical components (such as the capacitance of the capacitive element 152, capacitance of C_{ESC}, etc.) and/or the characteristics (e.g., voltage levels, duration, and/or the RF signal) of the waveform established at the electrode.

[0050] The capacitive element 152 may be implemented as one or more capacitors, such as a ceramic capacitor and/or a multi-layered dielectric capacitor. For example, the capacitive element 152 may include multiple capacitors coupled together in a network, such as a parallel network and/or series network. In certain cases, the capacitive element 152 may be rated to operate at high voltages, such as voltage levels above 10 kV. The capacitive element 152 may have a capacitance within a range of 500 picofarads (pF) to 1 nanofarad (nF). The capacitance value of the capacitive element 152 may be close to or higher than C_{ESC} and/or C_{SH}. That is, the capacitive element may have a capacitance equal to or greater than at least one of a substrate support capacitance (e.g., C_{ESC}) or a sheath capacitance (e.g., C_{SH}) of the processing chamber.

[0051] The capacitive element 152 may be selectively coupled to the electrode (e.g., the input node 408) of the processing chamber via at least one of the switches 402 (e.g., the switch 402c). The capacitive element 152 may be selectively coupled to the voltage source 404 and the ground node 414, for example, via at least one of the switches 402 (e.g., the switches 402d, 402e, and 402f). The capacitive element 152 and the voltage source 404 may be selectively coupled in parallel with the electrode (e.g., the input node 408). That is, the capacitive element 152 and the voltage source 404 may be selectively coupled to the electrode in parallel with each other. In certain aspects, the capacitive element 152 is a separate electrical component from the substrate support capacitance (C_{ESC}) and/or sheath capacitance (C_{SH}). In certain cases, the capacitive element 152 may be integrated with and/or co-located with the waveform generator assembly 150, such as the voltage source 404 and/or current source 406. In certain cases, the capacitive element 152 may be integrated with and/or co-located with the substrate support capacitance (C_{ESC}) and/or sheath capacitance (C_{SH}) to provide a suitable boost voltage as described herein.

[0052] The capacitive element 152 may provide a source for bulk electrons that is separate from the plasma. In certain cases, the capacitive element 152 may improve the sustainability and stability of the plasma by reducing the bulk electrons consumed from the plasma to establish the DC bias at the electrode.

[0053] The switches 402 may be implemented as high voltage solid-state relays. In certain cases, the switches 402 may be implemented as a high voltage multiplexer and/or demultiplexer. In this example, the switches 402 may include a first switch 402a, second switch 402b, third switch 402c, fourth switch 402d, fifth switch 402e, and sixth switch 402f. The first switch 402a may be coupled between the voltage source 404 and the input node 408, which may be electrically coupled to the electrode or representative of the electrode. The second switch 402b may be coupled between the input node 408 and the ground node 414. The third switch 402c may be coupled between a first terminal 416 of the capacitive element 152 and the input node 408. The fourth switch 402d may be coupled between a second terminal 418 of the capacitive element 152 and the input node 408. The fifth switch 402e may be coupled between the first terminal 416 of the capacitive element 152 and the ground node 414.

The sixth switch 402f may be coupled between the second terminal 418 of the capacitive element 152 and the ground node 414.

[0054] In certain cases, the state of the switches 402 (e.g., opened or closed) may be controlled by the system controller 126. For example, the system controller 126 may be in communication with control inputs (not shown) of the switches 402, such that control signals from the system controller 126 toggle the states of the switches 402. The system controller 126 may control the individual state of each switch 402 with a separate control signal applied to the respective switch. As further described herein with respect to Figures 5 and 6A-6C, the switches 402 may be configured to couple the capacitive element 152 and the voltage source 404 to the electrode (e.g., the input node 408) during a first phase (which may be referred to as the ESC recharging phase), couple the capacitive element 152 and the electrode to the ground node 414 during a second phase (which may be referred to as the voltage negation phase), and couple the capacitive element 152 to the electrode during a third phase (which may be referred to as the voltage boost phase). In aspects, the second phase may occur after the first phase, and the third phase may occur after the second phase. For certain aspects, the switches 402 may decouple the electrode from the capacitive element 152 and the voltage source 404 during the second phase and decouple the electrode from the ground node during the third phase.

[0055] The voltage source 404 may be a component of a waveform generator assembly (e.g., the waveform generator assembly 150). That is, the waveform generator assembly may include the voltage source 404, which may include a pulsed-voltage DC waveform generator and/or RF generator (also referred to as an RF signal generator). The voltage source 404 may be selectively coupled to the electrode (e.g., the input node 408) via one of the switches 402 (e.g., the switch 402a). For example, the switch 402a may be coupled in series between the voltage source 404 and the input node 408.

[0056] Similarly, the current source 406 may be a component of the waveform generator assembly. The current source 406 may be used to implement the ramp voltage during the ion current stage, for example, as described herein with respect to Figure 2A. The current source may be configured to apply an ion compensation current to the processing chamber (e.g., the electrode) during a fourth phase (e.g., the ion

current stage as depicted in Figure 2A). In aspects, the switches 402 may be configured to couple the capacitive element 152 to the processing chamber (e.g., the electrode) during the fourth phase, which may occur after the third phase. The current source 406 may be coupled to the electrode. In certain cases, the voltage source 404, current source 406, and capacitive element 152 may be coupled in parallel to the electrode (e.g., the input node 408).

[0057] Those of skill in the art will understand that the electrical circuit 400 is merely an example, and other electrical circuits (such as the circuits depicted in Figures 9 and 10) may be used in addition to or instead of the circuit illustrated to provide the voltage boost at the electrode and reduce the bulk electron consumption from the plasma. While the examples depicted in the present disclosure are described herein with respect to using a positive voltage pulse for the substrate processing to facilitate understanding, aspects of the present disclosure may also be applied to using a negative voltage pulse to establish the waveform at the electrode.

[0058] Figure 5 is a timing diagram 500 illustrating states of the switches 402 (labeled as S1-S6, respectively) of the electrical circuit 400, and Figures 6A-6C are circuit diagrams illustrating the states of the switches 402 during corresponding phases depicted in Figure 5, in accordance with certain embodiments of the present disclosure.

[0059] Referring to Figure 5, the waveform at the electrode may be established in a first phase 502, a second phase 504, a third phase 506, and a fourth phase 508. The first phase 502 can take from 20 nanoseconds (ns) to 2000 ns to allow enough electrons to be collected at the wafer surface. The second phase 504 and/or the third phase 506 can take from tens of nanoseconds to hundreds of nanoseconds, such as 20 ns to 500 ns. The fourth phase 508 can take greater than 50% of the waveform cycle, such as 85~90% of the waveform cycle. The frequency of the voltage function could range from 50kHz to 5000kHz.

[0060] During the first phase 502, switches 402a, 402d, and 402e (S1, S4, and S5) are closed to charge the substrate support 105 (C_{ESC}) and plasma sheath capacitance(s) (C_{SH} and C_{WALL}), as well as the capacitive element 152 (C_{BOOST}), as shown in Figure 6A. The charging time for these capacitors may be shorter or longer

than the duration depicted in Figure 5. During the first phase 502, the first switch 402a is configured to close; the second switch 402b is configured to open; the third switch 402c is configured to open; the fourth switch 402d is configured to close; the fifth switch 402e is configured to close; and the sixth switch 402f is configured to open.

[0061] The capacitive element 152, C_{ESC}, and C_{SH} may be charged to a voltage V_{BOOST} during the first phase 502. Plasma bulk electrons are attracted to the wafer surface due to the rising edge of the waveform shown in Figure 5. The electrons may not establish a negative DC sheath potential yet, for example, due to there being equal amounts of positive charge on the other electrode. An equivalent capacitance depicted as C_{ESC} may form between the wafer surface and the electrode, and there may be an equal amount of positive charge on the electrode to cancel the field generated by those electrons.

[0062] During the second phase 504, the second switch 402b and sixth switch 402f are closed as shown in Figure 6B. The first switch 402a, the fourth switch 402d, and the fifth switch 402e are configured to open during the second phase 504, and the second switch 402b and sixth switch 402f are configured to close during the second phase to couple the second terminal 418 of the capacitive element 152 and the input node 408 to the ground node 414. Effectively, the substrate support capacitance C_{ESC} is coupled to the ground node 414.

[0063] As the second switch 402b closes, the potential at the electrode may be forced to the voltage level at the ground node 414 (such as 0 Volts). As a capacitor's voltage drop cannot change instantaneously, the voltage on the wafer surface becomes negative thereby establishing a negative V_{dc} on the wafer surface. For example, with the second switch 402b in a closed state, the voltage at the electrode may be reduced to first voltage level.

[0064] The sixth switch 402f closes and pulls the potential of the connected capacitive element 152 to ground. The potential of at the capacitive element 152 becomes a negative voltage. During the second phase 504, the capacitive element 152 may not be coupled to the input node 408 and the substrate support. The negative DC voltage (V_{dc}) on the wafer surface after the second switch 402b closes can be

approximated by using the magnitude of the falling edge ΔV and the ratio between the C_{ESC} and sheath capacitance C_{sheath}:

$$|V_{dc}| = |\Delta V| \times \frac{C_{ESC}}{(C_{ESC}+C_{sheath})} \quad (1)$$

where C_{sheath} is the capacitance of the wafer sheath capacitance (C_{SH}) in series with the ground sheath capacitance (C_{WALL}). In certain cases, C_{sheath} may be approximated by the wafer sheath capacitance (C_{SH}) due to the ground sheath capacitance (C_{WALL}) being much larger.

[0065] During the third phase 506, the third switch 402c and sixth switch 402f are closed as shown in Figure 6C. The second switch 402b is configured to open, and the third switch 402c is configured to close during the third phase, such that the first terminal 416 of the capacitive element 152 is coupled to the input node 408. With the third switch 402c closed, the capacitive element 152 may further reduce the voltage at the electrode to a second voltage level less than the first voltage level. The third switch 402c connects the capacitive element 152 to the input node 408, which may further enhance V_{dc} on the wafer surface and pull V_{dc} more negative.

[0066] The voltage at the electrode may be given by:

$$|V_{dc}| = |\Delta V| \times \frac{C_{ESC}}{(C_{ESC}+C_{sheath})} + |V_{BOOST}| \times \frac{C_{ESC}}{(C_{ESC}+C_{sheath})} \quad (2)$$

[0067] In certain cases, |Vboost| may be higher than |ΔV|. For example, |Vboost| may be 1750 Volts, and |ΔV| may be 1000 Volts. In this example, the capacitive element 152 may reduce the number of electrons required to accumulate on the wafer surface by 2.75 times for the same amount of V_{dc}.

[0068] The fourth phase 508 is the ion current compensation phase, which may be implemented as described herein with respect to Figures 2A and 2B. During the fourth phase 508, the electrode voltage may have a negative slope to compensate ion current. The states of switches 402 may remain the same as the states established at the end of the third phase 506. That is, the third switch 402c and sixth switch 402f may remain closed during the fourth phase 508.

[0069] The oncoming ion current neutralizes the negative discharges on the wafer surface and discharges the sheath capacitor (e.g., C_{SH}). The wafer voltage may be kept at a constant voltage to provide single peak IED as described herein with respect to Figures 2B and 3. The current source 406 can be used to pump electrons to the circuit to compensate for the ion current. In doing so, the current source establishes a voltage waveform having a negative slope at the electrode. In fourth phase 508, the plasma ions bombard the wafer surface and induce etching reactions. The fourth phase 508 may be considered the etching period and may be made as long as possible to facilitate the desired etching (e.g., 1000 ns to 10,000 ns). The length may be limited by the charging speed of the wafer surface or the maximum voltage of the current source (if current compensation is performed).

[0070] The ion compensation current (I_{ion}) can be calibrated using ion energy/flux diagnostics or calculated by sampling the electrode voltage (V0) (e.g., to calculate time derivative of V0) and the value of the sheath capacitance:

$$I_{ion} = (C_{sheath} + C_{boost}) \frac{dV0}{dt} \qquad (3)$$

where C_{boost} is the capacitance of the capacitive element 152. For example, the first tens to hundreds of the cycles can be used to sample the electrode voltage and calculate I_{ion} for ion current compensation. The current compensation may then be implemented for the subsequent cycles. The current source 406 may be configured to adjust the ion compensation current in response to a change in voltage over time measured at the electrode based at least in part on a capacitance of the capacitive element, for example, as given by Equation (3). An increased capacitance of the capacitive element 152 may slow down the decay of V_{dc}. C_{boost} may be made as large as possible in the voltage rating allowed range.

[0071] Figure 7 is a process flow diagram illustrating a method 700 for boosting the voltage at the electrode. The method 700 may be performed by a plasma processing system, such as the processing system 10.

[0072] At activity 702, a capacitive element (e.g., the capacitive element 152) and a voltage source (e.g., the voltage source 404) may be coupled to an electrode (e.g., represented by the input node 408) disposed within a processing chamber (e.g., the

processing chamber 100) during a first phase (e.g., the first phase 502). The capacitive element 152 and the voltage source 404 may be coupled to the electrode in parallel, for example, as depicted in Figure 4. As an example, with respect to the electrical circuit 400, the first switch 402a, the fourth switch 402d, and the fifth switch 402e may be closed during the first phase. The second switch 402b, the third switch 402c, and the sixth switch 402f are opened during the first phase.

[0073] At activity 704, the capacitive element 152 and the electrode may be coupled to a ground node (e.g., the ground node 414) during a second phase (e.g., the second phase 504). During the second phase, the electrode may be decoupled from the voltage source and the capacitive element. As an example, with respect to the electrical circuit 400, the first switch 402a, fourth switch 402d, and fifth switch 402e are opened during the second phase. The second switch 402b and sixth switch 402f are closed during the second phase to couple the capacitive element to the input node (e.g., the input node 408). With the second switch 402b closed, a voltage at the electrode may be reduced to a first voltage level.

[0074] At activity 706, the capacitive element 152 may be coupled to the electrode during a third phase (e.g., the third phase 506). During the third phase, the electrode may decoupled from the ground node. As an example, with respect to the electrical circuit 400, the second switch 402b may be opened during the third phase, and the third switch may be closed to couple the first terminal 416 of the capacitive element 152 to the input node 408. With the third switch 402c closed, the voltage at the electrode may be reduced to a second voltage level less than the first voltage level.

[0075] At activity 708, a current source (e.g., the current source 406) may apply an ion compensation current to the electrode during a fourth phase (e.g., the fourth phase 508). In aspects, the capacitive element 152 may be coupled to the electrode during the fourth phase. For certain aspects, the current source may adjust the ion compensation current in response to a change in voltage over time measured at the electrode based at least in part on a capacitance of the capacitive element, for example, as given by the Equation (3).

[0076] In certain aspects, the method 700 may also include generating a plasma over a substrate supporting surface (e.g., the substrate support surface 105A) of a

substrate support (e.g., the substrate support 105) disposed in the processing chamber. The plasma and ion current compensation may facilitate the etching of the substrate as described herein.

[0077] In certain aspects, the timing of when the charged capacitive element is coupled to the electrode may be adjusted, for example, to produce multiple ion energies and/or adjust the width of an ion energy in an etching cycle.

[0078] Figure 8A shows an example voltage waveform that may be established at an electrode (e.g., the bias electrode 104 and/or support base 107) of a processing chamber, in accordance with certain embodiments of the present disclosure. As depicted, closing the third switch 402c in the third phase may be delayed compared to the waveform depicted in Figures 2A and 5. For example, the second phase may be have a longer duration than the duration depicted in Figures 2A and 5. An IEDF with two ion energies as depicted in Figure 8B may be produced with the delayed coupling of the capacitive element. As shown, the IEDF includes a low energy peak 802 and a high energy peak 804.

[0079] For certain aspects, the current source may be coupled in series with the capacitive element. For example, Figure 9 is an additional functionally equivalent, simplified electrical circuit 900 of a plasma processing system (e.g., the processing system 10) that may establish a voltage boost at an electrode, in accordance with certain embodiments of the present disclosure. The current source 406 may be selectively coupled to the processing chamber (e.g., the electrode) via the switches 402 (e.g., the third switch 402c), which may be configured to couple the current source to the processing chamber during the fourth phase. In this example, the capacitive element 152 may be selectively coupled in series between the current source 406 and the electrode (e.g., the input node 408). In the electrical circuit 900, the sixth switch 402f may be excluded.

[0080] The ion current may be adjusted according to the following expression:

$$I_{ion} = C_{sheath}\frac{dV0}{dt} \qquad (4)$$

[0081] As a result, the electrical circuit 900 may enable a lower ion current compared to the electrical circuit 400.

[0082] In certain aspects, a separate voltage source may be used to charge the capacitive element. For example, Figure 10 is an additional functionally equivalent, simplified electrical circuit 1000 of a plasma processing system (e.g., the processing system 10) that may establish a voltage boost at an electrode, in accordance with certain embodiments of the present disclosure. In the electrical circuit 1000, the voltage source may include a first voltage source 404a selectively coupled to the electrode (e.g., the input node 408) and a second voltage source 404b selective coupled to the capacitive element 152. In this example, the sixth switch 402f may be coupled in parallel with the second voltage source 404b and the fourth switch 402d. The fifth switch 402e may be coupled in series between the capacitive element 152 and the ground node 414.

[0083] During the first phase, the first switch 402a, fourth switch 402d, and the fifth switch 402e may be closed, while the second switch 402b, third switch 402c, and sixth switch 402f may be open. During the second phase, the sixth switch 402f and second switch 402b may be closed, while the first switch 402a, third switch 402c, and fourth switch 402d may be open. During the third phase, the third switch 402c and sixth switch 402f may be closed, while the first switch 402a, second switch 402b, and fifth switch 402e may be open.

[0084] In certain cases, the capacitive element 152 and the second voltage source 404b may be used to compensate ion current. For example, the third switch 402c may be closed at the middle of the fourth phase to produce a step down in voltage during the ion current compensation stage.

[0085] Similar to the concept of Voltage Triplers and Quadruplers, multiple stages of the boost capacitance can be used to further increase the wafer DC voltage. Such embodiments may use more switches and/or relays.

[0086] It will be appreciated that the techniques and apparatus described herein may reduce the number of plasma electrons consumed to establish the DC bias. As such, the techniques and apparatus described herein may improve plasma stability and extend the achievable maximum ion energy for substrate processing.

[0087] The term “coupled” is used herein to refer to the direct or indirect coupling between two objects. For example, if object A physically touches object B and object

B touches object C, then objects A and C may still be considered coupled to one another—even if objects A and C do not directly physically touch each other. For instance, a first object may be coupled to a second object even though the first object is never directly physically in contact with the second object.

[0088] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of processing a substrate, comprising:

coupling a capacitive element and a voltage source to an electrode disposed within a processing chamber during a first phase, wherein the capacitive element and the voltage source are coupled to the electrode in parallel;

coupling the capacitive element and the electrode to a ground node during a second phase; and

coupling the capacitive element to the electrode during a third phase.

2. The method of claim 1, further comprising:

generating a plasma over a substrate supporting surface of a substrate support disposed in the processing chamber, the substrate support comprising the electrode and a dielectric layer disposed between the electrode and the substrate supporting surface;

wherein coupling during the second phase further comprises decoupling the electrode from the voltage source and the capacitive element; and

wherein coupling during the third phase further comprises decoupling the electrode from the ground node.

3. The method of claim 1, wherein coupling during the first phase comprises:

closing a first switch coupled between the voltage source and an input node that is electrically coupled to the electrode;

closing a second switch coupled between a first terminal of the capacitive element and the input node; and

closing a third switch coupled between a second terminal of the capacitive element and the ground node.

4. The method of claim 3, wherein coupling during the first phase further comprises:

opening a fourth switch coupled between the input node and the ground node;

opening a fifth switch coupled between the first terminal of the capacitive element and the ground node; and

opening a sixth switch coupled between the second terminal of the capacitive element and the input node.

5. The method of claim 4, wherein coupling during the second phase comprises:

opening the first switch, the second switch, and the third switch; and

closing the fourth switch and the fifth switch to couple the first terminal of the capacitive element and the input node to the ground node.

6. The method of claim 5, wherein coupling during the third phase comprises:

opening the fourth switch; and

closing the sixth switch to couple the second terminal of the capacitive element to the input node.

7. The method of claim 1, further comprising applying, by use of a current source, an ion compensation current to the electrode during a fourth phase.

8. The method of claim 7, wherein the capacitive element is coupled to the electrode during the fourth phase.

9. The method of claim 7, further comprising:

generating a plasma over a substrate supporting surface of a substrate support disposed in the processing chamber, the substrate support comprising the electrode and a dielectric layer disposed between the electrode and the substrate supporting surface; and

wherein applying the ion compensation current comprises adjusting the ion compensation current in response to a change in voltage over time measured at the electrode based at least in part on a capacitance of the capacitive element.

10. The method of claim 1, wherein:

coupling during the second phase comprises reducing a voltage at the electrode to a first voltage level; and

coupling during the third phase comprises reducing the voltage at the electrode to a second voltage level less than the first voltage level.

11. A plasma processing system, comprising:

a plurality of switches;

an electrode disposed within a processing chamber;

a voltage source selectively coupled to the electrode via one of the plurality of switches; and

a capacitive element selectively coupled to the electrode via the one of the plurality of switches, wherein the capacitive element and the voltage source are coupled to the electrode in parallel, and wherein the plurality of switches are configured to:

couple the capacitive element and the voltage source to the electrode during a first phase,

couple the capacitive element and the electrode to a ground node during a second phase, and

couple the capacitive element to the electrode during a third phase.

12. The plasma processing system of claim 11, wherein:

the processing chamber comprises a substrate support that comprises a dielectric layer disposed over the electrode;

wherein the plurality of switches are configured to:

decouple the electrode from the capacitive element and the voltage source during the second phase, and

decouple the electrode from the ground node during the third phase.

13. The plasma processing system of claim 12, wherein the plurality of switches comprise:

a first switch coupled between the voltage source and an input node that is electrically coupled to the electrode, wherein the first switch is configured to close during the first phase;

a second switch coupled between a first terminal of the capacitive element and the input node, wherein the second switch is configured to close during the first phase; and

a third switch coupled between a second terminal of the capacitive element and the ground node, wherein the third switch is configured to close during the first phase.

14. The plasma processing system of claim 13, wherein the plurality of switches comprise:

a fourth switch coupled between the input node and the ground node, wherein the fourth switch is configured to open during the first phase;

a fifth switch coupled between the first terminal of the capacitive element and the ground node, wherein the fifth switch is configured to open during the first phase; and

a sixth switch coupled between the second terminal of the capacitive element and the input node, wherein the sixth switch is configured to open during the first phase.

15. The plasma processing system of claim 14, wherein:

the first switch, the second switch, and the fifth switch are configured to open during the second phase; and

the fourth switch and the fifth switch are configured to close during the second phase to couple the first terminal of the capacitive element and the input node to the ground node.

16. The plasma processing system of claim 15, wherein:

the fourth switch is configured to open during the third phase; and

the sixth switch is configured to close during the third phase to couple the second terminal of the capacitive element to the input node.

17. The plasma processing system of claim 11, further comprising:

a current source coupled to the electrode; and

wherein the current source is configured to apply an ion compensation current to the processing chamber during a fourth phase.

18. The plasma processing system claim 17, wherein the plurality of switches are configured to couple the capacitive element to the processing chamber during the fourth phase.

19. The plasma processing system of claim 17, wherein:

the processing chamber comprises a substrate support that comprises a dielectric layer that is disposed over the electrode; and

the current source is configured to adjust the ion compensation current in response to a change in voltage over time measured at the electrode based at least in part on a capacitance of the capacitive element.

20. The plasma processing system of claim 11, the plurality of switches are configured to:

couple the electrode to the ground node during the second phase to reduce a voltage at the electrode to a first voltage level; and

couple the capacitive element to the electrode during the third phase to reduce the voltage at the electrode to a second voltage level less than the first voltage level.