ABSTRACT

A HIGH GAIN LATERAL PNP AND NPN BIPOLAR TRANSISTOR AND PROCESS COMPATIBLE WITH CMOS FOR MAKING BICMOS CIRCUITS

A method and lateral bipolar transistor structure are achieved, with high current gain, compatible with CMOS processing to form BiCMOS circuits. Making a lateral PNP bipolar involves forming an N^- well in a P^- doped silicon substrate. A patterned Si_3N_4 layer is used as an oxidation barrier mask to form field oxide isolation around device areas by the LOCOS method. A polysilicon layer over device areas is patterned to leave portions over the intrinsic base areas of the L-PNP bipolar an implant block-out mask. A buried N^- base region is implanted in the substrate under the emitter region. A photoresist mask and the patterned polysilicon layer are used to implant the P^{++} doped emitter and collector for the L-PNP. The emitter junction depth x_j intersects the highly doped N^+ buried base region. This N^+ doped base under the emitter reduces the current gain of the unwanted (parasitic) vertical PNP portion of the L-PNP bipolar to reduce the current gain of the V-PNP. The built-in potential V_{bi} of the emitter-base junction also increases further the current gain of the V-PNP thereby increasing the gain of the L-PNP bipolar transistor. By reversing the polarity of the dopants, L-NPN components can also be made. Also by implanting a tetravalent impurity such as Ge, Si, or C, the current gain of the L-PNP can be further improved.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)

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