

ABSTRACT

A method of manufacturing an integrated circuit device includes providing a substrate including a cell array area and a peripheral circuit area; forming a conductive layer in the cell array area and the peripheral circuit area; forming a capping insulating layer on the conductive layer; forming, in the cell array area, a direct contact and a bit line by using the capping insulating layer as a first etching mask; forming a spacer structure on side walls of the direct contact and on side walls of the bit line; forming a buried contact that is between the direct contact and the bit line and a first side wall of the side walls of the bit line; forming an insulating spacer on the cell array area and the peripheral circuit area; and forming, in the peripheral circuit area, a gate structure by using the insulating spacer as a second etching mask.

FIG. 3A