

TELEVISION TUNING APPARATUS

BACKGROUND

The present invention pertains to the frequency
5 alignment of a plurality of tunable filters of a tuner which have a
tuning frequency responses which are determined by the
magnitudes of respective control signals.

Tunable filters responsive to the magnitude of a
control signal, e.g., a tuning voltage, are employed to select one RF
10 carrier from a plurality of received RF carriers, and for generating
a local oscillator (LO) signal having the appropriate frequency for
heterodyning the selected RF carrier to produce the IF signal.
When the passband of the RF filters do not properly track with
each other and the frequency of the local oscillator signal, the
15 desired resultant IF signal may be degraded and the possibility of
crosstalk from adjacent TV channels is increased.

Tunable filters usually include a voltage controlled
capacitance (varactor) diode as a frequency control element
because a varactor diode exhibits a capacitance vs. voltage
20 characteristic when they are reverse biased.

Owing to the normal tolerances of components
employed in tuning systems and to normal production variations,
it is necessary that the tunable filters in the RF tuner be initially
adjusted in production. This is because the varactor diodes in the
25 RF filters and local oscillator circuits do not have precisely the
same capacitance characteristics over the voltage range
corresponding to the tuning band of frequencies. This initial
adjustment typically involves mechanically "trimming" inductive
and capacitive elements so that the frequency responses of the
30 various tuned circuits are aligned and track one another
throughout one or more frequency bands. However, these
alignment adjustments are often time-consuming, sometimes
requiring an iterative alignment procedure.

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SUMMARY OF THE INVENTION

The invention concerns an arrangement including a microprocessor controller, PROM memory, and a digital to analog converter (DAC) arrangement for generating a plurality of control
5 voltages for trimming respective ones of a plurality of varactor controlled tunable filters. The controller couples digital control signals to the respective DACs which generate respective analog control voltages which are applied to the respective tunable filters. A tuning voltage generated by a closed control loop, such
10 as phased locked loop also under the control of the controller, is combined with the output control voltages generated by the respective DAC's in a resistance divider arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

15 Figure 1 is a block diagram of a tuner of a television system which may utilize an arrangement constructed according to aspects of the present invention.

Figure 2 is a schematic of an arrangement constructed according to the present invention which may be employed in the
20 television system shown in Figure 1.

Figure 3 is an block diagram representation of the arrangement shown in Figure 2.

Figure 4 is a schematic diagram of a modification of the arrangement shown in Figure 2 including a temperature
25 compensation circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1, shows a tuner section 10 of a television apparatus and includes an input 12 for receiving television RF
30 carriers provided by an antenna, cable system, or other input device, such as a VCR. The received RF signals are filtered by an input RF filter 14 to attenuate undesired signals. The output signals of filter 14 are amplified by RF amplifier 16. The output signals of amplifier 16 are coupled to a double tuned RF output
35 filter 18 which includes two tunable circuits 20 and 22. The RF signals from circuit 22 are coupled to mixer 24 and are



heterodyned with the output signal of a local oscillator 26 which has its frequency controlled by phase locked loop (PLL) 28 in response to a tuning voltage V_{to} . The output of mixer 24 is an IF signal which is amplified and filtered by IF amplifier 30.

5 Tunable filters 14, 20, 22 each include a tuned circuit comprising an inductor and a varactor diode connected in parallel combination. The varactor diodes of tuning filters 14, 20 and 22 receive respective tuning voltages V_{c14} , V_{c20} and V_{c22} .

Tuning voltages V_{c14} , V_{c20} and V_{c22} for tuned
10 circuits 14, 20, and 22 are generated by a respective DAC and combiner units 32, 34, and 36 in response to digital signals fed from microprocessor (uP) 40 and the tuning voltage V_{to} of PLL 28. When a channel is selected, microprocessor 40 generates digital trimming or adjustment control signals which are
15 determined from data stored in PROM 42 and which are coupled to addressable DAC's 32, 34, and 36. Microprocessor controller 40 also provides the appropriate division factor (usually referred to as "N") in digital form to PLL 28. In response to the digital division factor, N, PLL 28 generates an analog tuning voltage V_{to}
20 to adjust the frequency of local oscillator 26 by changing the capacitance of a varactor diode 44 associated with local oscillator 26. Tuning voltage V_{to} is also coupled via line 46 to DAC and combining units 32, 34, and 36.

In production at the factory, the optimum trimming
25 voltages provided by respective DACs of units 32, 34, and 36 for tuning the varactor diodes of tuning circuits 14, 20, 22 are determined. The tuning voltages V_{c14} , V_{c20} and V_{c22} for tunable circuits 14, 20 and 22 respectively are a combination of the analog voltage corresponding to the digital trimming controls
30 signal received from PROM 42 via microprocessor 40 and tuning voltage V_{to} received on line 46 from PLL 28, as will be discussed more fully below.

During production, the digital trimming control signals to be provided by microprocessor 40 for optimal tuning of tuning
35 circuits 14, 20, and 22 are received via bus line 48 and written into PROM 42. At a later time, when a viewer enters a channel



select signal via bus line 51, a digital channel select signal is passed to PLL 28 via line 52 and the digital trimming control data is read from PROM 42.

Referring now to Figure 2, there is shown the DAC and combining circuitry within each of units 32, 34, and 36 shown in block form in Figure 1. The output signal of microprocessor 40 corresponding to the digital trimming data stored in PROM 42 is a pulse width modulated (PWM) pulse signal. The PWM signal controls electronic switch 50. Switch 50 is coupled between one end of a voltage divider comprising resistors 52 and 54 and signal ground. The other end of the voltage divider receives a reference voltage Vref. Reference voltage Vref is the combination of a divided down version of PLL tuning voltage Vto and a constant voltage Vo according to the equation $V_{ref} = kV_{to} + V_o$ (see Figure 3). A voltage V1 developed at the junction of resistors 54 and 52 is fed to non-inverting input 56 of operational amplifier (op amp) 58. A voltage Vr is fed to inverting input 60 through resistor 62. Voltage Vr provides an adjustable "offset" voltage for centering the output tuning voltage Vc within the adjustment tuning range for the particular band of frequencies which are being tuned. Output terminal 64 is coupled to output filter 66 comprising resistor 68 and capacitor 70, with feedback being provided from terminal 64 to terminal 60 by resistor 72 and capacitor 74.

A block diagram version of the circuit shown in Figure 2 is shown in Figure 3, wherein like members have like designations. Figure 3 shows the combination of a version of voltage Vto (amplified by a factor Ko) and constant voltage Vo to form Vref. Voltage V1 is combined with a version of voltage Vr amplified by a factor G to produce an output signal at line 64. The later signal is lowpass filtered by low pass filter 66 to produce tuning voltage Vc.

Mathematically, the control voltage can be expressed as:

$$V_c = (K_o V_{to} + V_o)(1 - K_2 K_{dac})(G + 1) - G V_r$$

if $G K_o = 1$, $V_r = V_o$, and $K_2(G + 1) = 2$, the above equation simplifies to:

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$$V_c = V_{to} + K_o V_{to} + V_o - 2K_{dac}(K_o V_{to} + V_o).$$

If $K_o = 0.16$ and $V_o = 1$, then ± 1 volt for $V_c = 0$, and ± 5 volts for $V_c = 25$.

Figure 4 shows a temperature compensation circuit 75 for temperature compensating the circuit of Figure 2.

Temperature compensation circuit 75 is substituted for the source of "offset" voltage V_r of the arrangement shown in Figure 2. The bases of each of transistors 80, 82 are coupled to a source of voltage V_{r1} through resistor 76, with the collector of transistor 80 being coupled to V_{r1} through resistor 78 and the collector of transistor 82 being coupled directly to source of voltage V_{r1} . The emitters of transistors 80 and 82 are respectively coupled to ground through resistors 84 and 86 with output voltage V_r being taken across resistor 86. A temperature compensated version of V_r is provided by transistor 82. The base-to-emitter voltage change of transistor 82 with changes of temperature are tracked by the base-emitter voltage change of transistor 80.

The application of V_{to} from the PLL reduces the number of channels requiring alignment and therefore the total amount of data requiring storage in the PROM. If the tuning voltage (V_c) for the tunable filters 14, 20, and 22 were responsive only to the DACs, not only would the DACs need to be high resolution DACs, but each channel would require alignment data. However, with the tuning voltage V_c being responsive to V_{to} , the tuning voltage V_c will change with channel even for the same DAC output. This first approximation provided by the application of V_{to} is sufficient for alignment over a small range of channels, thus reducing the number of channels requiring unique data. Both the reduced range of the DAC and the fewer number of channels requiring unique alignment data means that much less data needs to be stored in the PROM with a subsequent savings of cost of the PROM.

The voltage divider of resistors 52, 54 maintains the first approximation offered by the application of V_{to} . If the divider were not present (resistor 52 being replaced by a short circuit wire), the voltage V_1 at 56, and consequently the tuning



voltage V_c , would be zero for a DAC setting of zero. Thus, for channels requiring a large V_{to} , the adjustment range of V_c afforded by the DAC would also be large (zero volts to more than V_{to}) and the DAC resolution would have to be larger. The inclusion of the resistive voltage divider 52, 54 prevents the tuning voltage V_c from reaching below a predetermined minimum when the DAC output voltage is zero volts and V_{to} is large.

With the proper selection of component values, the application of V_{to} , as represented by V_{ref} combined with the resistive voltage divider 52, 54, work to provide a tuning voltage V_c substantially equal to V_{to} when the DAC is set to the mid-range tuning for a particular channel. As the DAC setting is increased or decreased from mid-range, the tuning voltage V_c is offset from V_{to} . Further, the offset tuning range provided by the DAC is proportional to V_{to} providing a greater tuning range at high channels where the varactor sensitivity is less and a lower tuning range at low channels where greater voltage resolution is needed.

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CLAIMS

1. In a tuning system including input means for receiving a plurality of RF signals corresponding to respective channels; frequency selection means for selecting one of said
5 plurality of RF signals corresponding to a respective selected channel, conversion means for producing at an output an information bearing signal in accordance with the modulation of a selected RF signal, apparatus comprising:

a plurality of tunable circuits coupled between said
10 input and said output and cooperating to control the frequency characteristics of said apparatus between said input and said output;

each of said tunable circuits including a reactive element having a reactive value determined by the magnitude of
15 a respective analog control signal;

means for providing a plurality of digital control signals in response to a selected channel

means for generating an analog tuning voltage having a magnitude responsive to said selected channel;

20 means for combining a scaled version of said analog tuning voltage with respective ones of said digital control signals to produce respective analog control signals; and

means for coupling said analog control signals to respective ones of said tunable circuits.

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2. The apparatus of claim 1 wherein said combining means includes a plurality of voltage dividers each having first and second ends;

means for coupling said analog tuning voltage to said
30 first ends of respective ones of said voltage dividers;

means for converting said digital control signals to respective pulse control signals; and

means for selectively coupling a reference potential to said second ends of respective ones of said voltage dividers in
35 response to respective ones of said pulse control signals.

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3. The apparatus of claim 1 wherein said means for providing said digital control signals includes memory means for storing digital data related to said digital control signals; and processor means for causing said data to be read from said
5 memory means.

4. The apparatus of claim 1 wherein the analog tuning voltage generated by said means for generating said analog tuning voltage comprises a closed loop for generating a local oscillator
10 signal for said conversion means;

said local oscillator signal having a frequency determined by said selected channel and being control by said analog tuning voltage.

15 5. Tuning apparatus, comprising:

a local oscillator signal having a frequency controlled in response to a the magnitude of a tuning signal; said local oscillator being including in a closes loop which is responsive to digital selection word representing a desired channel;

20 an RF section having a least one filters tunable in response to the magnitude of an analog control signal;

a memory for storing a digital adjustment signal; to said digital selection word, and for converting said digital adjustment signal to a pulse signal;

25 a voltage divider having first and second ends and a point intermediate said ends;

means for coupling said tuning signal to said first end of said voltage divider;

means for selectively coupling said second end of said
30 voltage divider to a point of reference potential in response to said pulse signal;

means for coupled to said intermediate point for developing said analog control signal for said tunable filter.



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