TITLE OF THE INVENTION

LAND GRID ARRAY SEMICONDUCTOR DEVICE PACKAGES, ASSEMBLIES INCLUDING SAME, AND METHODS OF FABRICATION

BACKGROUND OF THE INVENTION

[0001] Field of the Invention. The present invention relates generally to packaging of semiconductor devices and, more particularly, to semiconductor device packages incorporating a land grid array package therein, wherein the land grid array package may be configured to bear additional components, to enhance repairability, or both, as well as methods of fabricating such packages and related assemblies.

[0002] Discusion of Related Art. Semiconductor dice are becoming ever-smaller in dimension, both from advances in fabrication technology and as so-called "shrinks" of initial semiconductor die designs are developed to increase the number of dice which may be fabricated on a wafer or other bulk semiconductor substrate. As a consequence, it becomes more difficult to employ lead frame-based packaging techniques using, for example, wire bonds to directly connect bond pads of a die to lead fingers of a lead frame due to diminishing size of bond pads as well as decreasing pitch (spacing) between adjacent bond pads, rendering it difficult, if not impossible in some circumstances, to place inner ends of lead fingers of a lead frame in close proximity to bond pads to which they are to be wire bonded. In addition, below a certain minimum bond pad size and pitch, it becomes impossible to position a wire bonding capillary head accurately enough to avoid contact with, and possible damage to, adjacent bond pads.

[0003] Further, when bond pads are arranged along a central axis of a semiconductor die, such as is conventional in so-called "leads over chip," or "LOC" packages, one may be faced with a choice between overcrowding lead fingers to place them in close proximity to the bond pads, or forming overly long wire bonds between the bond pads and remotely placed inner ends of lead fingers and risking potential breakage of the wire bonds or shorting between adjacent wire bonds when the package is being transfer-molded in an encapsulant by so-called "wire bond sweep" initiated by the flow front of the molten encapsulant moving over the active surface of the semiconductor die.

[0004] In addition, most conventional packages do not facilitate high device density in conjunction with high multi-die device yields in terms of utilizing available "real estate" on a printed circuit board or other higher-level packaging. Further, most conventional packages do not afford the capability to readily assemble dissimilar components into a single package so as to provide, for example, a so-called "system-in-a-package" or to provide a repair capability to the package either before or after all of the components thereof have been assembled and connected. In addition, such capabilities are not afforded by existing land grid array packages suitable for use on a variety of carriers, for example lead frames as well as printed circuit boards.

[0005] Therefore, it would be desirable to provide a semiconductor device assembly packaging configuration which would accommodate ever-smaller semiconductor dice and their smaller, more closely pitched bond pads, and which would also facilitate the fabrication of highly reliable multi-die assemblies offering relatively high device densities and enhanced repairability.

BRIEF SUMMARY OF THE INVENTION

[0006] The present invention comprises a semiconductor device package including a land grid array package. The present invention further comprises semiconductor device package including a land grid array package having an electrical component in the form of at least one active component, at least one passive component, or both, connected thereto.

[0007] In one embodiment, the present invention comprises at least one semiconductor die mounted to an interposer substrate, with wire bonds extending from bond pads of the semiconductor die to terminal pads on the side of the interposer substrate to which the at least one semiconductor die is mounted. The terminal pads of the interposer substrate are electrically connected to a land grid array pattern of pads or lands extending along one or more edges of the interposer substrate and to a two-dimensional (in the X and Y directions), more centrally located array pattern of pads, both pad patterns located on the opposing side of the interposer substrate from the at least one semiconductor die. The at least one semiconductor die and wire bonds are overmolded with an encapsulant, leaving the opposing side of the interposer substrate

free of encapsulant, to form a land grid array package also providing a two-dimensional pad array suitable for open/short testing and functional testing of the assembly before the land grid array package is incorporated in a higher-level assembly.

[0008] The latter, two-dimensional pad array may also be employed in accordance with the present invention, for connection of one or more active components, one or more passive components, or both types of components, to the land grid array package. In addition, pads of the two-dimensional pad array may be employed in a repair function, to connect pads by wire bonding to lead fingers of a lead frame in case there are open, or shorted power, ground, bias or signal paths in the interposer. Further, some or all of the two-dimensional array of pads may be connected to different terminal pads than those to which the lands are connected, to ease routing difficulties and simplify design of the interposer substrate by enabling some terminal pads to be connected to lead fingers of a lead frame through lands as described below, while others may be connected to lead fingers by wire bonds extending from pads of the two-dimensional array.

[0009] It is also contemplated that the pads of the two-dimensional array may be bumped with a conductive material to facilitate connection of other components or wire bonds thereto.

[0010] In fabrication of a lead frame-based semiconductor device package according to the present invention, lead fingers of a lead frame superimposed on the opposing side of the interposer substrate may be bonded directly to the land grid array lands. Further, as noted above, some of the lead fingers may be connected to pads of the two-dimensional array through wire bonds, either to ease routing difficulties on the interposer substrate or to repair defective power, ground, bias, or signal paths. A conventional trim and form operation may be used to remove the lead frame surrounding the lead fingers as well as tie bars or dam bars extending therebetween, and form the outer ends of the lead fingers to final shape and length.

[0011] Before or after connection of the land grid array package to the lead frame, one or more passive components (e.g., resistor, inductor, capacitor), one or more active components (e.g., another semiconductor die) or both, may be mechanically and electrically connected to pads of the two-dimensional array. As noted above, these pads may be conductively bumped with discrete conductive elements to facilitate such

connections or, for example, a flip-chip configured die bearing discrete conductive elements thereon may be connected directly to the pads. If a flip-chip configured or other discrete conductive element connector array-type semiconductor die is connected to the land grid array package, a dielectric underfill may also be disposed between the die and the interposer substrate and around the discrete conductive elements.

[0012] In fabrication of a carrier substrate-based semiconductor device package according to the present invention, conductive pads of circuitry carried on or within a carrier substrate to which the land grid array package is mounted may be wire bonded directly to the land grid array lands. Further, as noted above, some of the conductive pads may be connected to pads of the two-dimensional array of pads to bypass defective electrical paths or to simplify the structure of the interposer substrate. The wire bonds may be encapsulated with a protective dielectric material.

[0013] Before or after connection of the land grid array package to the carrier substrate, one or more passive components (e.g., resistor, inductor, capacitor), one or more active components (e.g., another semiconductor die) or both, may be mechanically and electrically connected to pads of the two-dimensional array. As noted above, these pads may be conductively bumped to facilitate such connections or, for example, a flip-chip configured die bearing discrete conductive elements thereon may be connected directly to the pads. If a flip-chip configured or other discrete conductive element connector array-type semiconductor die is connected to the land grid array package, a dielectric underfill may also be disposed between the die and the interposer substrate and around the discrete conductive elements.

[0014] Methods of fabricating lead frame-based semiconductor device packages including a land grid array package are also encompassed by the present invention, as are land grid array packages suitable for use in the semiconductor device assemblies of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a perspective view of one land grid array package configuration according to the present invention with a near side of the package cut away to depict internal components;

[0016] FIG. 2 is a top elevation of the land grid array package of FIG. 1;

[0017] FIG. 2A is an enlarged view of the circled area in FIG. 2;

[0018] FIG. 3 is an enlarged, side sectional elevation of a portion of another land grid array package configuration according to the present invention;

[0019] FIG. 4 is a perspective view of a land grid array package according to the present invention prior to, and after, assembly with a lead frame;

[0020] FIG. 5 is a schematic view of an embodiment of a land grid array package assembled with a lead frame according to the present invention before and after a trim and form operation;

[0021] FIG. 6 is a perspective view of a land grid array package according to the invention after assembly with a lead frame and passive and active components, and depicting a wire bond connection to a lead finger of the lead frame in addition to the direct land connections;

[0022] FIG. 7 is a side elevation of the land grid array package of FIG. 7; and

[0023] FIG. 8 is a side elevation of a land grid array package according to the present invention disposed on and connected to a carrier substrate in the form of a printed circuit board.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0024] In the description which follows, like features and elements have been identified by the same or similar reference numerals for ease of identification and enhanced understanding of the disclosure hereof. Such identification is by way of convenience for the reader only, however, and is not limiting of the present invention or an implication that features and elements of various components and embodiments identified by like reference numerals are identical or constrained to identical functions.

[0025] Referring now to FIG. 1 of the invention, land grid array package 100 comprises first and second semiconductor dice 102 and 104, each of which bears bond pads 106 adjacent opposing peripheral edges thereof, according to a selected pinout design, which may be customized using a redistribution layer to relocated inner lead bond locations to more peripheral, outer lead bond locations of bond pads 106. As can be seen in FIG. 1, semiconductor die 104 is slightly shorter in length than semiconductor die 102,

so that as semiconductor die 104 is mounted by its back side 108 to the active surface 110 of semiconductor die 102, bond pads 106 of semiconductor die 102 remain exposed. Semiconductor die 102 is mounted by its back side 108 to interposer substrate 112, the bond pads of each semiconductor die 102 and 104 being electrically connected to terminal pads 114 disposed in rows along opposing edges of interposer substrate 112 by wire bonds 116 extending therebetween. The side of interposer substrate 112 bearing semiconductor dice 102 and 104 is encapsulated in an encapsulant structure of dielectric material 105 covering the semiconductor dice 102 and 104, wire bonds 116 and terminal pads 114. Desirably, the encapsulant structure extends to the lateral periphery of interposer substrate 112. Encapsulation may be effected by conventional techniques such as, by way of example only, transfer molding, injection molding and pot molding.

[0026] Some or all of terminal pads 114 may be electrically connected through a conductive via to an associated conductive land 118 in a row of lands 118 extending along the same edge, but on an opposing side of, interposer substrate 112. Some or all of terminal pads 114 may also be electrically connected through a via (which may be the same or a different via) and a conductive trace to a conductive pad 120 of an array of pads 120 located in a central region of interposer substrate 112 between the rows of lands 118 and on the same side of interposer substrate 112 thereas. It is, thus, contemplated that a terminal pad 114 may be connected to a land 118 and redundantly connected to a pad 120, only to a land 118 or only to a pad 120. Thus, semiconductor dice 102 and 104 may be electrically accessed through contact with test pads 120 or through lands 118 or both, depending on the selected design for interposer substrate 112. Pads 120 may be used for open/short testing and functional testing of the semiconductor dice 102 and 104 of land grid array package 100 prior to final assembly with other components or for other purposes as described below. The pinouts of the lands 118 as well as the pads 120 may, of course, be customized for, respectively, connection to a lead frame or conductive pads of a carrier substrate such as, for example, a printed circuit board as further described below as well as for testing. The dimensions and pinouts of land grid array package may be selected for compatibility with all Flash and random access (RAM) memory semiconductor devices.

[0027] Referring now to FIG. 2, the configuration of the central, two-dimensional array of pads 120 may be clearly seen, pads 120 being exposed, for example, through 0.300 mm openings in a solder mask on interposer substrate 112. As shown, the location, or identification of Pin A1 of the pinout pattern of lands 118 may be identified by a fiducial mark 122 at a corner of interposer substrate 112 immediately inboard of a row of lands 118. Such a fiducial mark 122 is useful for both operator and machine vision recognition and proper orientation and placement of land grid array package 100 for testing as well as assembly purposes. FIG. 2A depicts the configuration and pitch (spacing) P of lands 118, which are matched to the width and pitch of lead fingers of a lead frame to be assembled with land grid array package 100 as described below.

[0028] FIG. 3 is an enlarged, side sectional view of a portion of another embodiment of a land grid array package 200 according to the present invention. Land grid array package 200 includes only a single semiconductor die 102 with bond pads 106 along opposing peripheral edges thereof. Semiconductor die 102 is mounted by its back side 108 to interposer substrate 212 by an adhesive element or layer 103, with wire bonds 116 extending between and electrically connecting bond pads 106 with terminal pads 114 of interposer substrate 212.

[0029] Interposer substrate 212, as with interposer substrate 112, includes a dielectric core or member 113 which carries conductive material thereon comprising terminal pads 114, conductive traces 115, lands 118 and pads 120, terminal pads 114 being electrically connected to lands 118 and test pads 120 by conductive traces 115 and conductively lined or filled via structures 117. Dielectric core 113 may comprise any suitable electrically insulative material such as, by way of example only, a polyimide film or sheet, BT resin, FR-4 or FR-5 laminate, or a ceramic, and terminal pads 114, conductive traces 115, conductively lined or filled via structures 117, lands 118 and pads 120 may be formed of any suitable conductive material such as, by way of example only, copper or aluminum. These conductive structures may be formed by conventional blanket deposition of the conductive material on dielectric core 113 and into via structures 117, followed by conventional application of a photoresist, masking, exposing and developing to define the conductive structures on each side of dielectric core 113,

and etching away portions of the conductive material exposed by the photoresist pattern. Alternatively, interposer substrates 112 and 212 may be provided as a dielectric core 113 sandwiched between two conductive sheets, via structures 117 formed therethrough and conductively lined or filled, and then the conductive structures formed on the major surfaces thereof by conventional masking and etching. As may be easily seen in FIG. 3, a solder mask or other patterned dielectric layer 121 may be employed to cover both sides of interposer substrate 212 (as well as interposer substrate 112 of FIG. 1) to fill conductively lined (if not completely conductively filled) via structures 117, and leave terminal pads 114, lands 118 and pads 120 exposed.

[0030] Land grid array packages 100, 200 may then be open/short tested as well as functionally tested using pads 120 before further assembly with a lead frame or carrier substrate and other components, as further described below.

[0031] As depicted in FIG. 4, a land grid array package 100, 200 (shown in an inverted position as depicted in more detail in FIG. 1) may then be aligned with a lead frame 300 comprising two opposing lead frame segments 302 each including a plurality of lead fingers 304 separated by transversely extending segments 306, which as illustrated comprise tie bars integrally formed with lead fingers 304. For the sake of clarity, additional components mounted to interposer substrate 112, 212 as described below have been omitted from the drawing. Inner ends 308 of lead fingers 304 are placed over lands 118, and mechanically and electrically connected thereto by solder 310, which may be preplaced in a paste form, as by stenciling, on lands 118 or on inner ends 308, lands 118 being formed or coated with a solder-wettable material. The solder is reflowed to bond inner ends 308 to lands 118 by application of heat. Rather than soldering, lands 118 may be mechanically and electrically connected to inner ends 308 of lead fingers 304 using a conductive or conductor-filled epoxy, which may be cured to a B-stage (tacky) prior to assembly of the components and then further cured to form a solid, permanent bond.

[0032] As shown in FIG. 5, the assembly of lead frame 300 with land grid array package 100, 200, after assembly with additional components as described below (not shown for clarity in FIG. 5), may have a thin layer of dielectric material 316 applied as shown in broken lines to cover pads 120 and, optionally, inner ends 308 of lead fingers

304. Such a layer may comprise, for example, a polymer coating such as a polyimide, applied by a dispensing nozzle or spray head. A photopolymer may also be employed, applied by commercially available equipment and exposed to an appropriate wavelength of light (typically UV) to cure the photopolymer after or as it is applied. Lead fingers 304 may then be formed into a final configuration and transversely extending segments 306 removed in a conventional trim and form operation, as shown.

[0033] As depicted in FIGS. 6 and 7, a land grid array package 100, 200 may have pads 120 of the two-dimensional array of pads conductively bumped with discrete conductive elements 320, as by use of a wire bond capillary head or formation or disposition and bonding of preformed conductive bump, ball, stud, column or pillar structures thereon as is known to those of ordinary skill in the art, to facilitate connection of other components to land grid array package 100, 200, or connecting wire bonds thereto. As depicted in FIGS. 6 and 7, land grid array package 100, 200 may be mechanically and electrically connected as described above to lead fingers 304 of a lead frame 300.

[0034] In one aspect of the present invention, one or more passive components (e.g., resistor, inductor, capacitor) 330 may be mechanically and electrically connected to pads 120 and, thus, to semiconductor dice 102, 104 and ultimately to higher-level packaging through discrete conductive elements 320. Similarly, one or more active components (semiconductor device) 332 may also be connected to pads 120 and, thus, to semiconductor dice 102, 104 and ultimately to higher-level packaging through discrete conductive elements 320. As noted above, if an active component 332 as depicted in FIG. 6 is configured as a flip-chip or otherwise bears its own array of discrete conductive elements arranged to align with a plurality of pads 120, those pads 120 need not be bumped and the discrete conductive elements carried by the active component may be used to connect directly to those pads 120. As shown in FIG. 6, both passive and active components may be connected to land grid array package 100, 200. As also shown in FIG. 6, wire bonds 334 may be formed between discrete conductive elements 320 (or, optionally directly on pads 120) and inner ends 308 of lead fingers 304 of lead frame 300. Such wire bonds may be used to bypass faulty signal, ground, bias or power paths within

interposer substrate 112, 212, or to simplify the design and fabrication of the conductive paths within and on interposer substrate 112, 212.

[0035] As noted above, a dielectric layer 316 (not shown in FIG. 6 for clarity) may be disposed over interposer substrate 112, 212, as well as over passive and active components 330, 332 and wire bonds 334. If a component, such as illustrated active component 332, defines a considerable open volume 336 thereunder, a dielectric underfill 338 such as is used in conventional flip-chip and array-type assemblies may be disposed within volume 338 and around discrete conductive elements 320 to fill the open volume and enhance the mechanical connection of active component 332 to interposer substrate 112, 212 and another dielectric layer as described above applied over the assembly thereafter. Alternatively, a silicone "glob top" type of encapsulant may be disposed within open volume 336 and over components 330, 332, wire bonds 334 and inner ends 308 of lead fingers 304 in a single process.

[0036] FIG. 8 depicts a land grid array package 100, 200 which is disposed on and connected to a carrier substrate 400 in the form of, for example, a printed circuit board such as, without limitation, a motherboard. Land grid array package 100, 200 is oriented with interposer substrate 112, 212 facing away from carrier substrate 400, and may be bonded thereto using, for example, a flowable adhesive or a dielectric tape or film carrying an adhesive layer on both sides thereof (not shown), as is conventional. Wire bonds 420 may then be formed between lands 118 and conductive pads 404 in communication with circuitry carried by carrier substrate 400. Lands 118, wire bonds 420 and conductive pads 404 may then be encapsulated by any of the techniques previously described. Passive and active components 330, 332 as well as wire bonds 334, may also be encapsulated as described above. It should be noted that wire bonds 420 may be extended from pads 120 more proximate a periphery of interposer substrate 112, 212 to conductive pads 404 and, if interposer substrate is provided with some electrically isolated pads 120, more interior pads 120 may be connected to conductive pads 404 using two wire bond segments using an electrically isolated pad 120 as a "jumper" pad.

[0037] While the present invention has been described in terms of certain illustrated embodiments and variations thereof, it will be understood and appreciated by those of ordinary skill in the art that the invention is not so limited. Rather, additions,

deletions and modifications to the illustrated embodiments may be effected without departing from the spirit and scope of the invention as defined by the claims which follow.

CLAIMS

What is claimed is:

1. A semiconductor device package, comprising:

an interposer substrate comprising a dielectric member, a plurality of terminals proximate and extending along at least one peripheral edge thereof on one side thereof and an array of lands proximate and extending along a same at least one peripheral edge on an opposing side of the interposer substrate, terminals of the plurality being respectively electrically connected to lands of the land array through conductive via structures extending through the dielectric member, the interposer substrate further comprising a two-dimensional array of pads substantially centrally located on the opposing side of the interposer substrate, and wherein terminals of the plurality are respectively electrically connected to pads of the two-dimensional pad array;

at least one semiconductor die mounted by a back side thereof to the one side of the interposer substrate and having a plurality of bond pads on an active surface thereof proximate and extending along at least one peripheral edge thereof adjacent the at least one peripheral edge of the interposer substrate respectively electrically connected to the plurality of terminals; and

an encapsulant structure disposed over the at least one semiconductor die and the one side of the interposer substrate;

2. The semiconductor device package of claim 1, further comprising at least one electrical component mechanically and electrically connected to the interposer substrate through pads of the two-dimensional pad array.

3. The semiconductor device package of claim 2, wherein the at least one electrical component is selected from the group consisting of passive components and active components.

4. The semiconductor device package of claim 2, further comprising discrete conductive bumps disposed on at least some of the pads of the two-dimensional pad array, the at least one electrical component being connected to the pads through some of the discrete conductive elements.

5. The semiconductor device package of claim 2, further comprising discrete conductive bumps disposed on at least some of the pads of the two-dimensional pad array.

6. The semiconductor device package of claim 2, further comprising a lead frame comprising a plurality of lead fingers having inner ends respectively disposed over lands of the land array on the opposing side of the interposer substrate and mechanically and electrically connected thereto.

7. The semiconductor device package of claim 6, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and an inner end of at least one lead finger.

8. The semiconductor device package of claim 6, wherein at least the inner ends of the lead fingers and the opposing side of the interposer substrate are covered with a dielectric material.

9. The semiconductor device package of claim 6, wherein the at least one electrical component is covered with a dielectric material.

10. The semiconductor device package of claim 2, further comprising:

a carrier substrate to which the land grid array package is affixed by a side thereof opposite the interposer substrate, the carrier substrate including a plurality of conductive pads on a surface thereof to which the land grid array package is affixed; and

wire bonds extending between lands of the land array and conductive pads of the plurality of conductive pads.

11. The semiconductor device package of claim 10, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate.

12. The semiconductor device package of claim 11, wherein the wire bond bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate comprises two segments joined at an electrically isolated pad of the two-dimensional pad array.

13. The semiconductor device package of claim 10, wherein at least the lands of the land array, the wire bonds and the conductive pads are covered with a dielectric material.

14. The semiconductor device package of claim 10, wherein the at least one electrical component is covered with a dielectric material.

15. The semiconductor device package of claim 1, wherein the at least one peripheral edge of each of the interposer substrate and the at least one semiconductor die comprises two opposing peripheral edges.

16. The semiconductor device package of claim 1, wherein the plurality of bond pads are electrically connected to the plurality of terminals with wire bonds.

17. The semiconductor device package of claim 1, wherein the at least one semiconductor die comprises two semiconductor dice, one semiconductor die being mounted by a back side thereof on the interposer substrate, another semiconductor die being mounted by a back side thereof on the active surface of the one semiconductor die and sized to leave the bond pads of the first semiconductor die exposed.

18. The semiconductor device package of claim 17, wherein the bond pads of each of the one semiconductor die and the another semiconductor die are electrically connected to the plurality of terminals with wire bonds.

19. The semiconductor device package of claim 1, wherein the encapsulant structure extends to peripheral edges of the interposer substrate.

20. The semiconductor device package of claim 4, further comprising a dielectric underfill material disposed in an open volume between the at least one electrical component and the opposing side of the interposer substrate and about the discrete conductive elements by which the at least one electrical component is connected to the pads of the two-dimensional pad array.

21. The semiconductor device package of claim 2, wherein the at least one electrical component comprises a plurality of components including at least one passive component and at least one active component.

22. A method of fabricating a semiconductor device package, the method comprising:

providing an interposer substrate comprising a dielectric member, a plurality of terminals proximate and extending along at least one peripheral edge thereof on one side thereof and an array of lands proximate and extending along a same at least one peripheral edge on an opposing side of the interposer substrate, terminals of the plurality being respectively electrically connected to lands of the land array through conductive via structures extending through the dielectric member, the interposer substrate further comprising a two-dimensional array of pads substantially centrally located on the opposing side of the interposer substrate, and wherein terminals of the plurality are respectively electrically connected to pads of the two-dimensional pad array;

mounting at least one semiconductor die by a back side thereof to the one side of the interposer substrate with a plurality of bond pads on an active surface thereof proximate and extending along at least one peripheral edge thereof adjacent the at least one peripheral edge of the interposer substrate;

respectively electrically connecting the plurality of bond pads to the plurality of terminals; and

disposing an encapsulant structure over the at least one semiconductor die and the one side of the interposer substrate.

23. The method of claim 22, further comprising mechanically and electrically connecting at least one electrical component to the interposer substrate through pads of the two-dimensional pad array.

24. The method of claim 23, further comprising selecting the at least one electrical component from the group consisting of passive components and active components.

25 The method of claim 23, further comprising disposing discrete conductive bumps on at least some of the pads of the two-dimensional pad array and connecting the at least one electrical component to the pads through some of the discrete conductive elements.

26. The method of claim 23, further comprising disposing discrete conductive bumps on at least some of the pads of the two-dimensional pad array.

27. The method of claim 2, further comprising providing a lead frame including a plurality of lead fingers, disposing inner ends thereof respectively over lands of the land array on the opposing side of the interposer substrate and mechanically and electrically connecting the inner ends thereto.

28. The method of claim 27, further comprising extending a wire bond between at least one pad of the two-dimensional pad array and an inner end of at least one lead finger.

29. The method of claim 27, further comprising covering at least the inner ends of the lead fingers and the opposing side of the interposer substrate with a dielectric material.

30. The method of claim 27, further comprising covering the at least one electrical component with a dielectric material.

31. The method of claim 23, further comprising:

affixing a carrier substrate to the land grid array package by a side thereof opposite the interposer substrate, the carrier substrate including a plurality of conductive pads on a surface thereof to which the land grid array package is affixed; and

extending wire bonds between lands of the land array and conductive pads of the plurality of conductive pads.

32. The method of claim 31, further comprising extending a wire bond between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate.

33. The method of claim 32, wherein extending the wire bond bond between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate comprises extending the wire bond in two segments joined at an electrically isolated pad of the two-dimensional pad array.

34. The method of claim 31, further comprising covering at least the lands of the land array, the wire bonds and the conductive pads with a dielectric material.

35. The method of claim 31, further comprising covering the at least one electrical component with a dielectric material.

36. The method of claim 22, further comprising selecting the at least one peripheral edge of each of the interposer substrate and the at least one semiconductor die to comprise two opposing peripheral edges.

37. The method of claim 22, further comprising electrically connecting the plurality of bond pads to the plurality of terminals with wire bonds.

38. The method of claim 22, further comprising:
selecting the at least one semiconductor die to comprise two semiconductor dice;
mounting one semiconductor die by a back side thereof on the interposer substrate;
mounting another semiconductor die by a back side thereof on the active surface of the one semiconductor die in a manner to leave the bond pads of the first semiconductor die exposed.

39. The method of claim 38, further comprising electrically connecting the bond pads of each of the one semiconductor die and the another semiconductor die to the plurality of terminals with wire bonds.

40. The method of claim 22, further comprising forming the encapsulant structure to extend to peripheral edges of the interposer substrate.

41. The method of claim 25, further comprising disposing a dielectric underfill material in an open volume between the at least one electrical component and the opposing side of the interposer substrate and about the discrete conductive elements by which the at least one electrical component is connected to the pads of the two-dimensional pad array.

42. The method of claim 23, further comprising selecting the at least one electrical component to comprise a plurality of components including at least one passive component and at least one active component.

43. The method of claim 22, further comprising testing the at least one semiconductor die after mounting to the interposer substrate and connection of the plurality of bond pads to the plurality of terminals and before assembly thereof with additional structures.

44. The method of claim 43, wherein testing comprises at least one of open/short testing and functional testing.