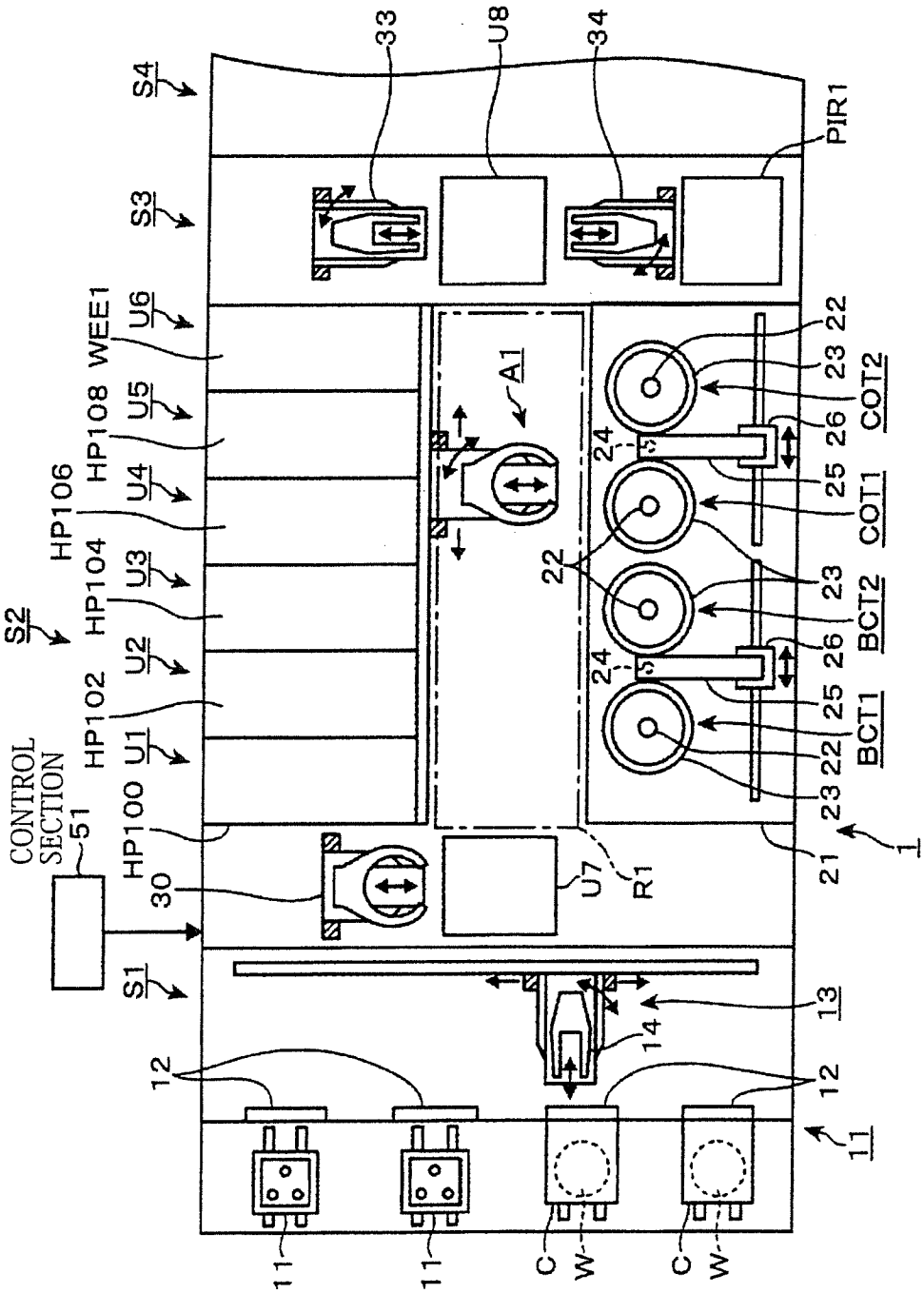

S4
S3
S2
S1
33
U8
34
PIR1
U6
WEE1
U5
HP108
U4
HP106
U3
HP104
U2
HP102
U1
HP100
CONTROL SECTION
51
30
A1
U7
R1
22
23
24
25
26
COT2
COT1
BCT2
BCT1
21
1
13
14
12
11
C
W

FIG. 1

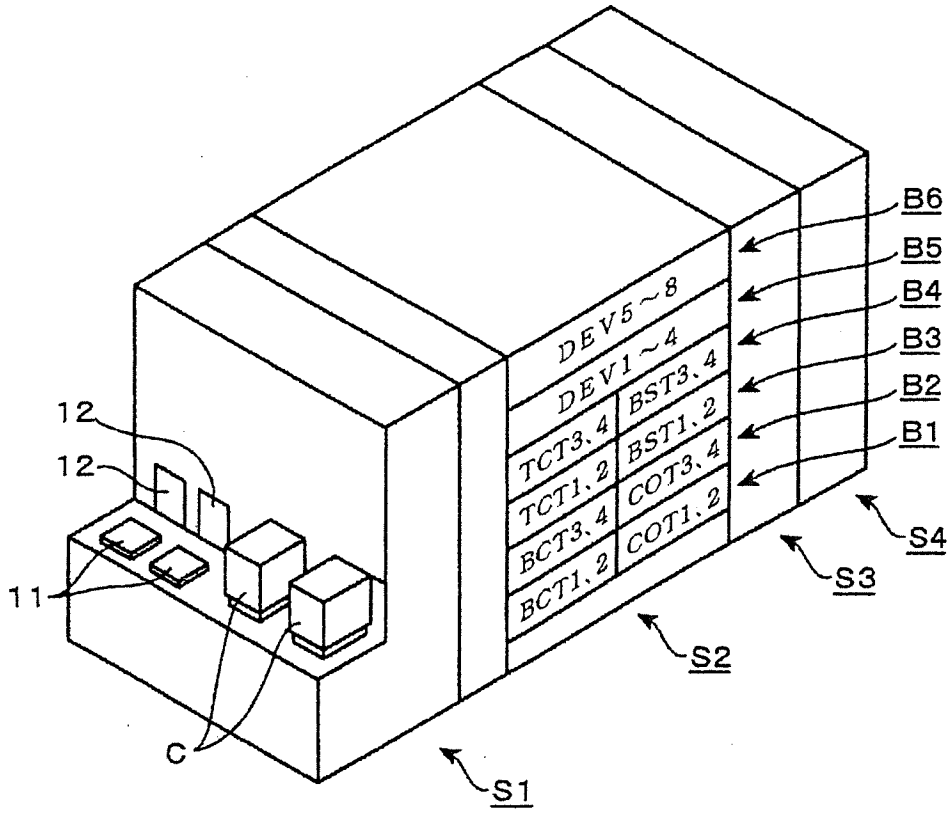

B6
B5
B4
B3
B2
B1
DEV5～8
DEV1～4
TCT3, 4
TCT1, 2
BCT3, 4
BCT1, 2
BST3, 4
BST1, 2
COT3, 4
COT1, 2
12
12
11
C
S1
S2
S3
S4

FIG. 2

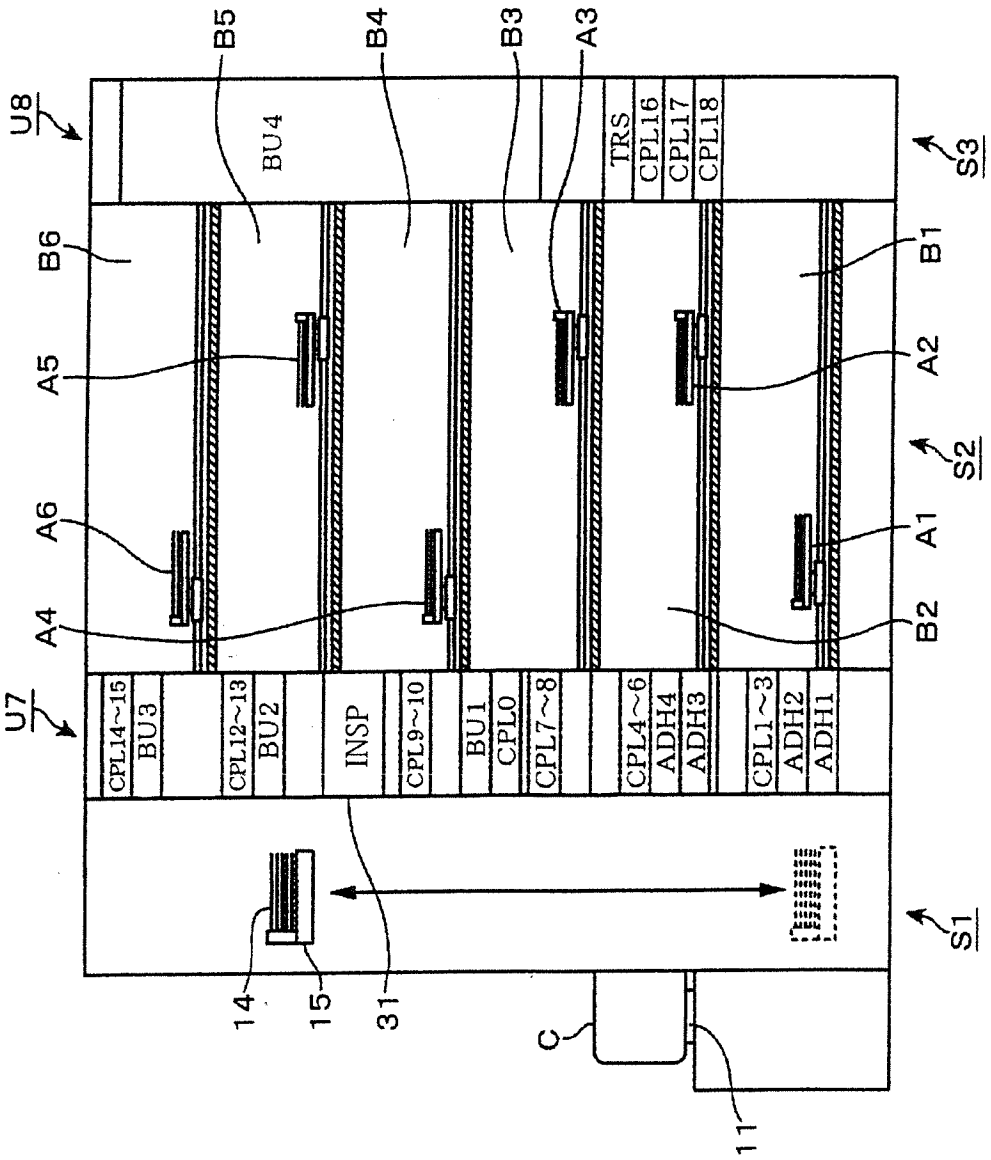

U8
U7
B5
B4
B3
A3
B6
A5
A6
A4
B1
A2
A1
B2
S3
S2
S1
BU4
TRS
CPL16
CPL17
CPL18
CPL14~15
BU3
CPL12~13
BU2
INSP
CPL9~10
BU1
CPL0
CPL7~8
CPL4~6
ADH4
ADH3
CPL1~3
ADH2
ADH1
14
15
31
C
11

FIG. 3

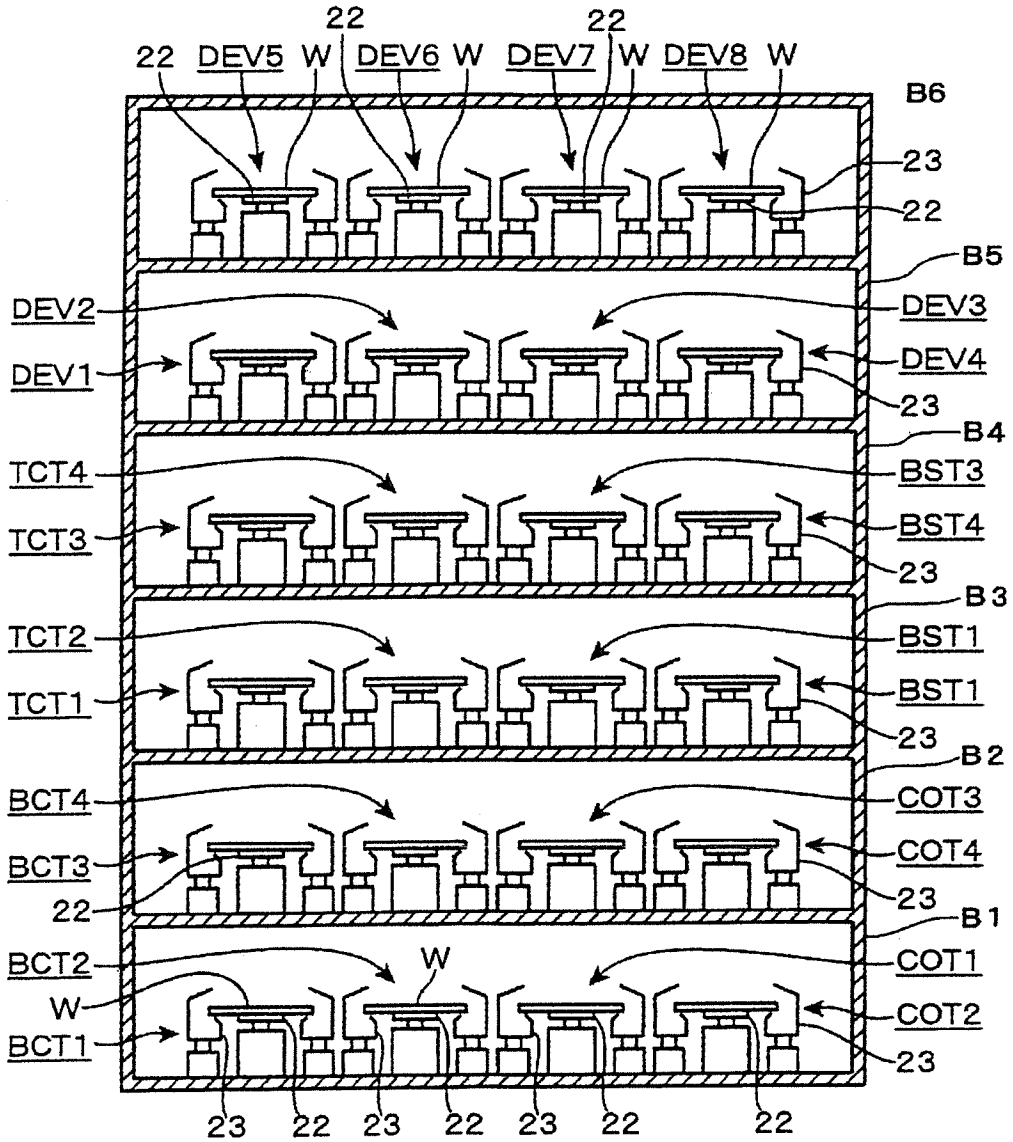

22
22
22 DEV5 W DEV6 W DEV7 W DEV8 W
B6
23
22
B5
DEV2
DEV3
DEV1
DEV4
23
B4
TCT4
BST3
TCT3
BST4
23
B3
TCT2
BST1
TCT1
BST1
23
B2
BCT4
COT3
BCT3
COT4
22
23
B1
BCT2
W
COT1
W
COT2
BCT1
23
23 22 23 22 23 22 22

FIG. 4

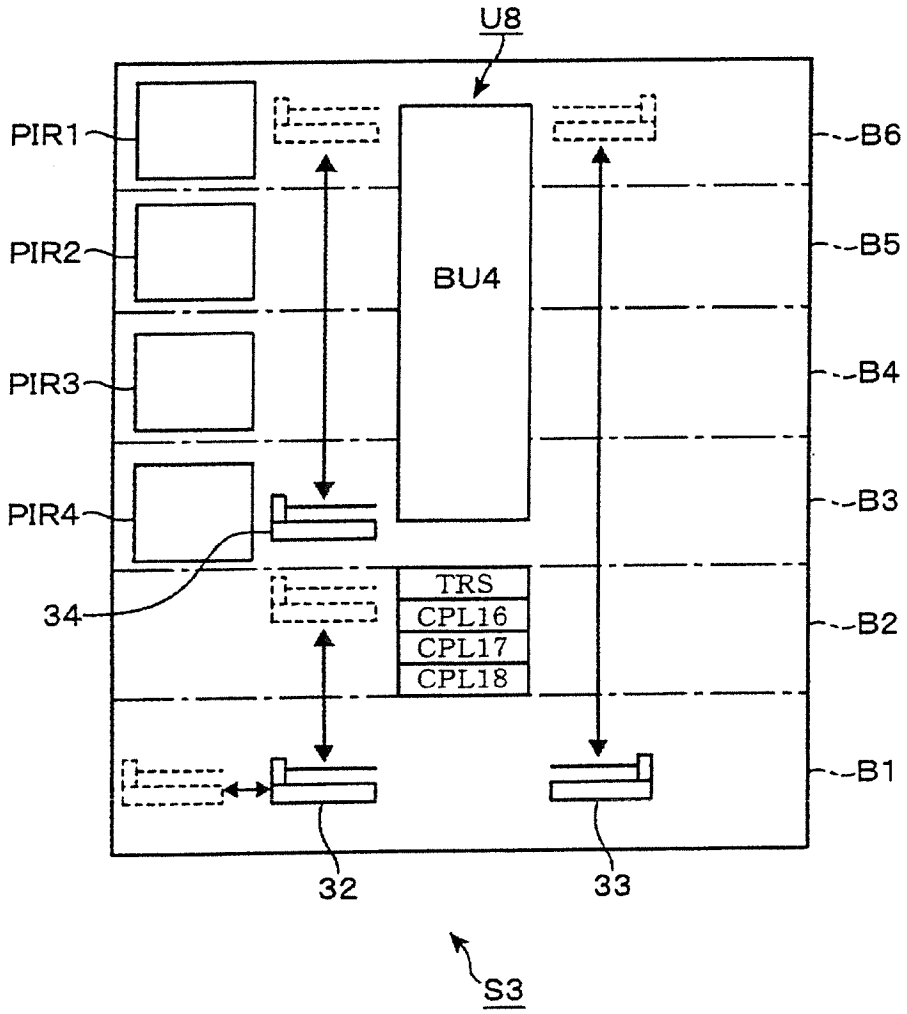

U8
PIR1
PIR2
PIR3
PIR4
34
BU4
TRS
CPL16
CPL17
CPL18
B6
B5
B4
B3
B2
B1
32
33
S3

FIG. 5

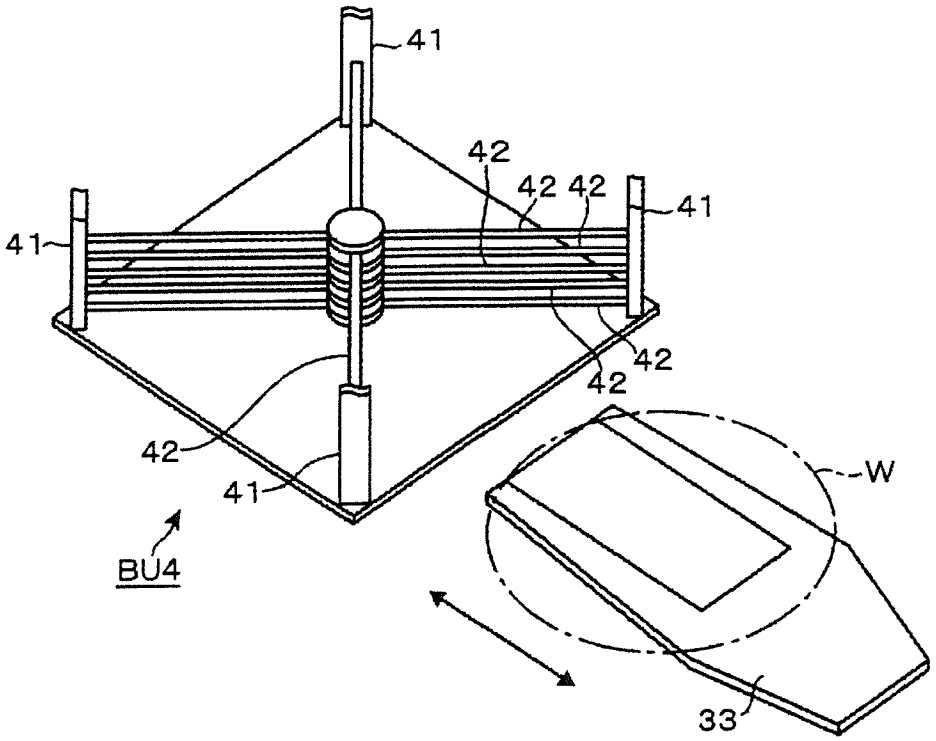


FIG. 6

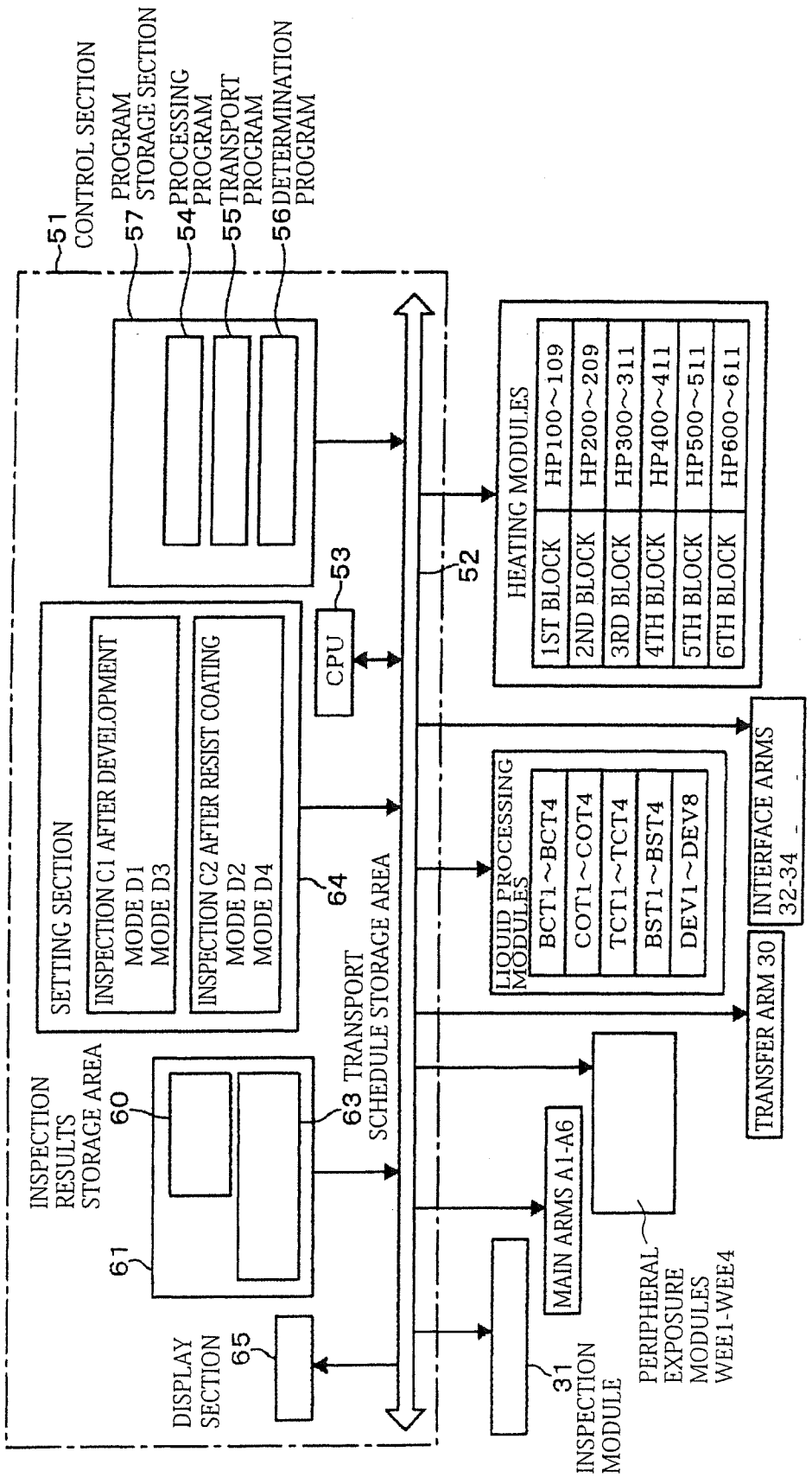

51
CONTROL SECTION
PROGRAM STORAGE SECTION
57
54 PROCESSING PROGRAM
55 TRANSPORT PROGRAM
56 DETERMINATION PROGRAM
CPU
53
52
SETTING SECTION
INSPECTION C1 AFTER DEVELOPMENT
MODE D1
MODE D3
INSPECTION C2 AFTER RESIST COATING
MODE D2
MODE D4
64
HEATING MODULES
1ST BLOCK HP100~109
2ND BLOCK HP200~209
3RD BLOCK HP300~311
4TH BLOCK HP400~411
5TH BLOCK HP500~511
6TH BLOCK HP600~611
LIQUID PROCESSING MODULES
BCT1~BCT4
COT1~COT4
TCT1~TCT4
BST1~BST4
DEV1~DEV8
INTERFACE ARMS 32-34
TRANSFER ARM 30
INSPECTION RESULTS STORAGE AREA
60
63 TRANSPORT SCHEDULE STORAGE AREA
61
MAIN ARMS A1-A6
PERIPHERAL EXPOSURE MODULES WEE1-WEE4
DISPLAY SECTION
65
31
INSPECTION MODULE

FIG. 7

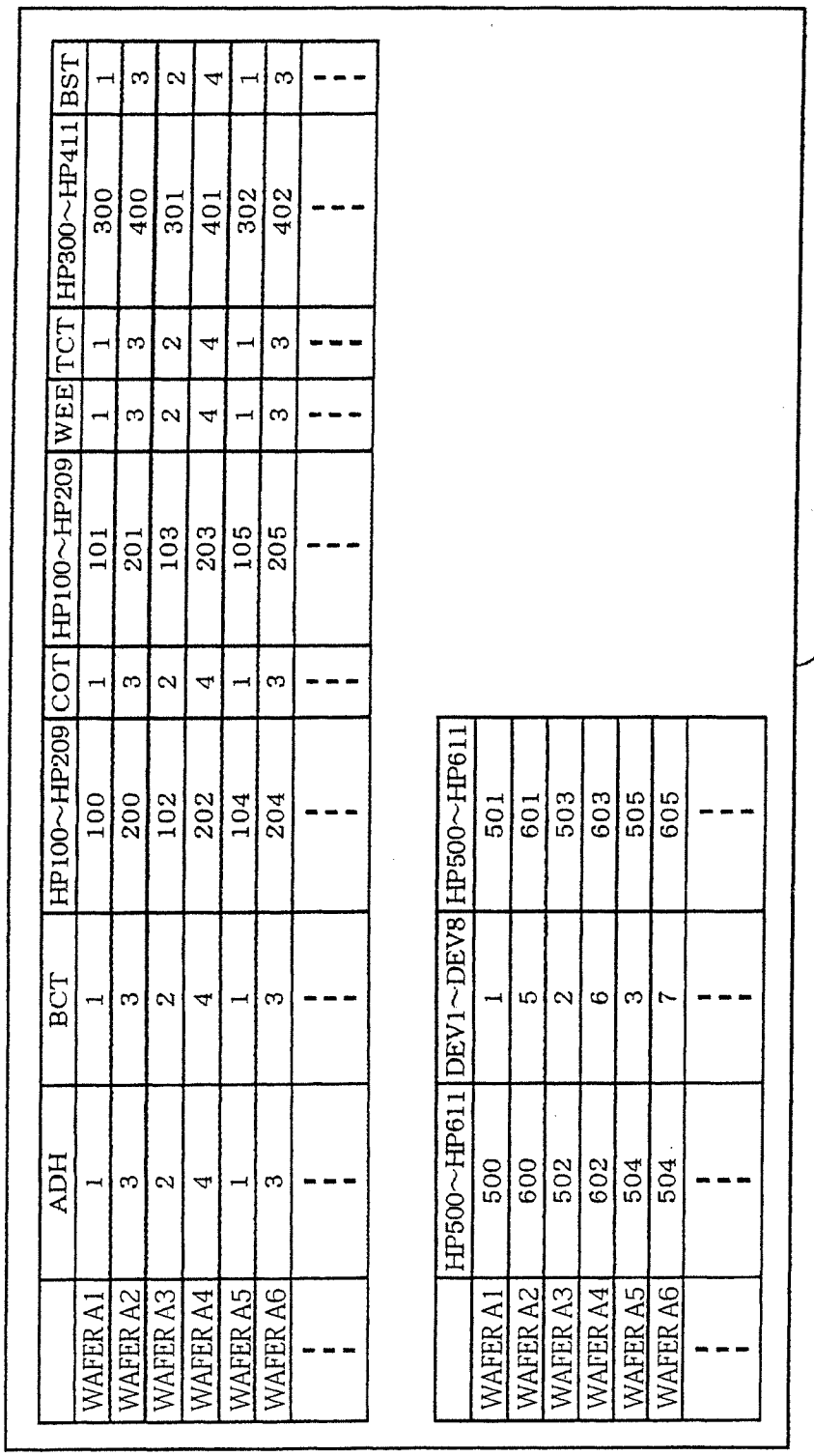

ADH
BCT
HP100~HP209
COT
HP100~HP209
WEE
TCT
HP300~HP411
BST
WAFER A1
WAFER A2
WAFER A3
WAFER A4
WAFER A5
WAFER A6
HP500~HP611
DEV1~DEV8
HP500~HP611
63

FIG. 8

	INSPECTION ITEM					RELEVANT MODULE	RELEVANT UNIT BLOCK
	PATTERN COLLAPSE	POOR RESIST DISSOLUTION	BUBBLES AFTER DEVELOPMENT	- - -	SCUM DEFECT		
TRANSPORT STOP CRITERIA	2/5	1/5	1/5	- - -	IMMEDIATE STOP		
WAFER A1	NONE	NONE	NONE	- - -	NONE		
WAFER A2	NONE	NONE	NONE	- - -	NONE		
WAFER A3	NONE	FOUND	NONE	- - -	NONE	DEV1 - - -	B1, B3, B5
WAFER A4	NONE	NONE	NONE	- - -	NONE		
WAFER A5	NONE	NONE	FOUND	- - -	NONE	DEV5 - - -	B2, B4, B6
WAFER A6	NONE	NONE	NONE	- - -	NONE		
- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -

60

FIG. 9

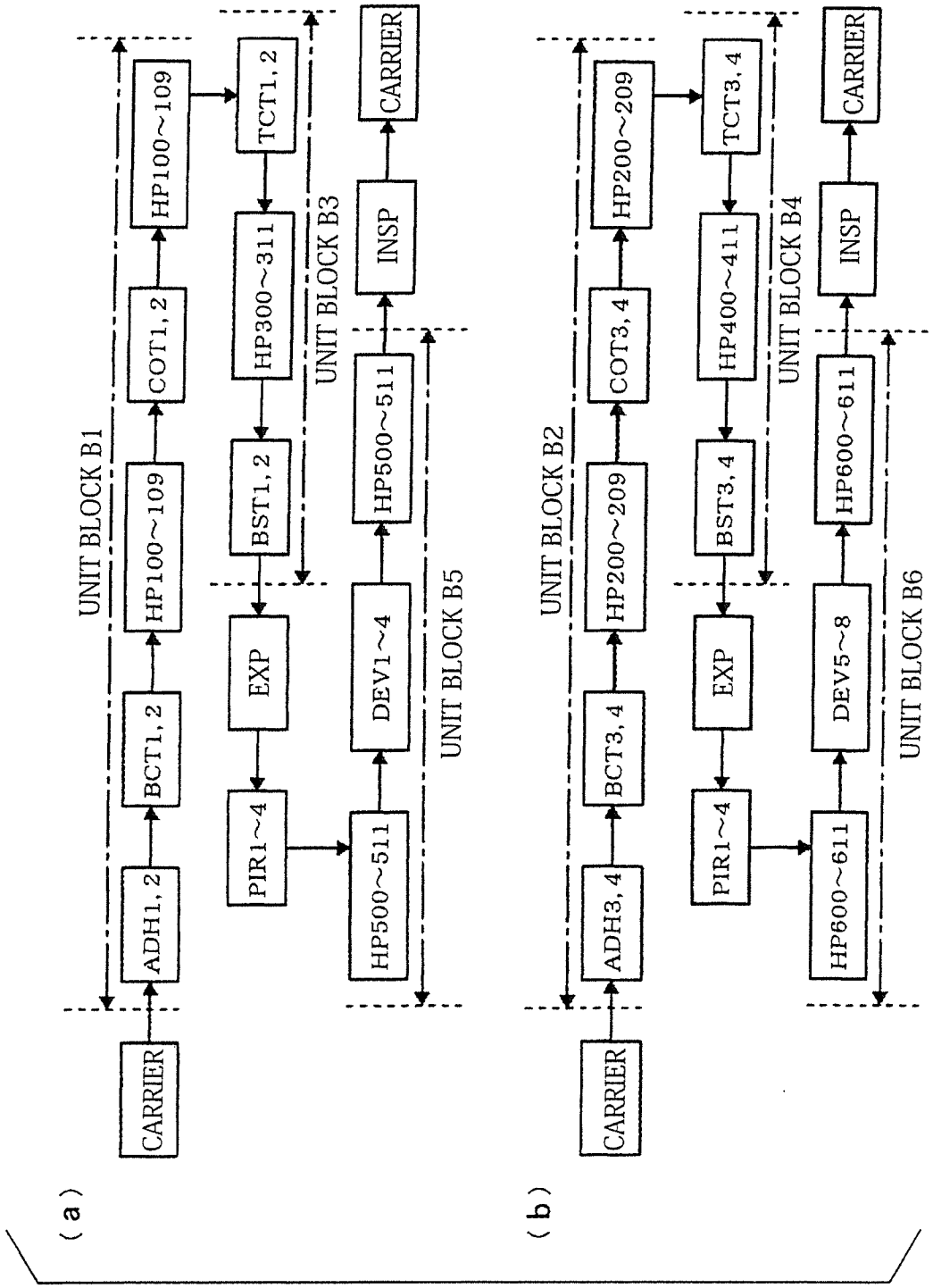

(a)
CARRIER
ADH1, 2
BCT1, 2
HP100~109
COT1, 2
HP100~109
TCT1, 2
UNIT BLOCK B1
EXP
BST1, 2
HP300~311
UNIT BLOCK B3
PIR1~4
HP500~511
DEV1~4
HP500~511
INSP
CARRIER
UNIT BLOCK B5
(b)
CARRIER
ADH3, 4
BCT3, 4
HP200~209
COT3, 4
HP200~209
TCT3, 4
UNIT BLOCK B2
EXP
BST3, 4
HP400~411
UNIT BLOCK B4
PIR1~4
HP600~611
DEV5~8
HP600~611
INSP
CARRIER
UNIT BLOCK B6

FIG. 10

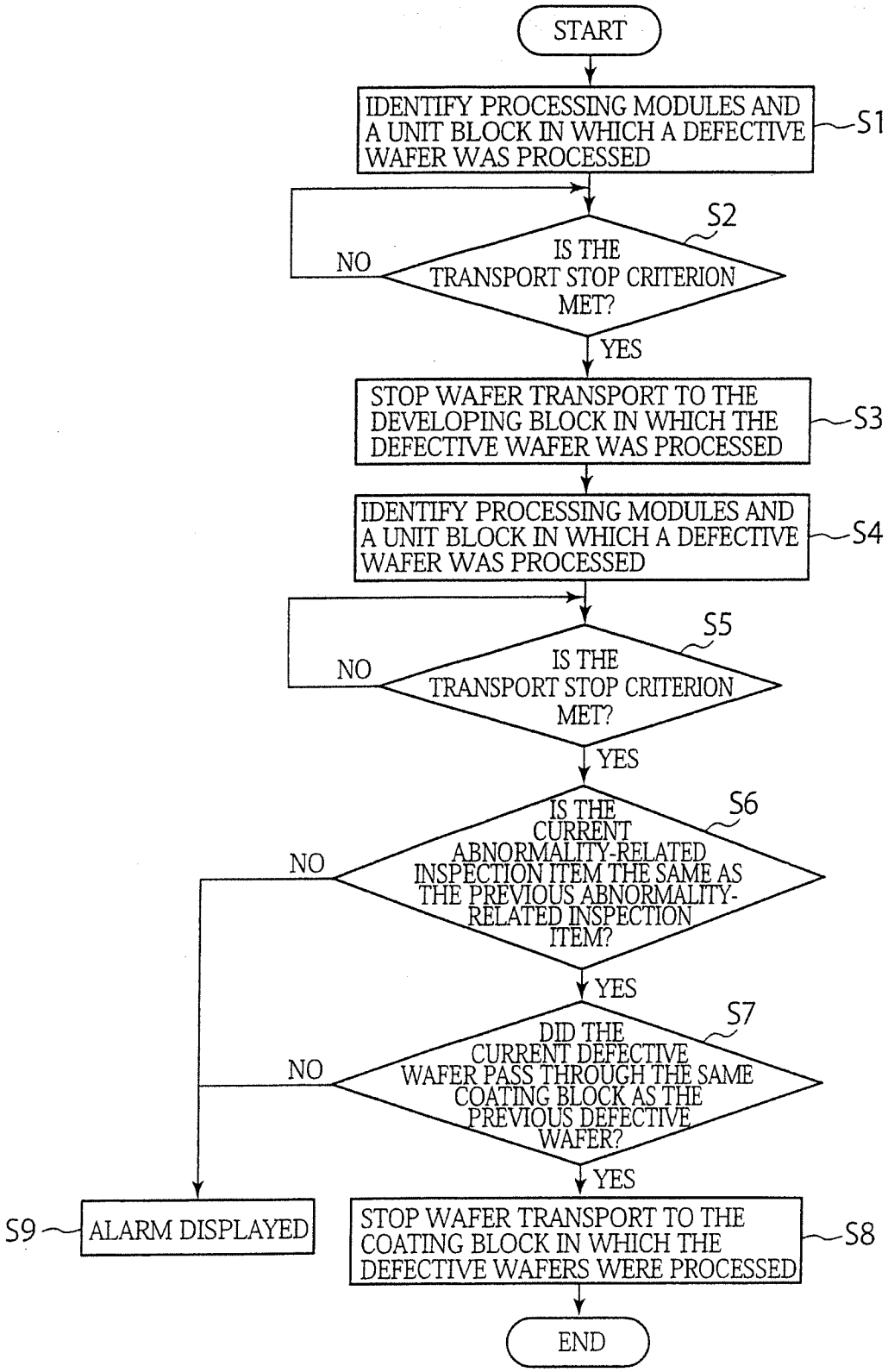

START
IDENTIFY PROCESSING MODULES AND A UNIT BLOCK IN WHICH A DEFECTIVE WAFER WAS PROCESSED
S1
S2
IS THE TRANSPORT STOP CRITERION MET?
NO
YES
STOP WAFER TRANSPORT TO THE DEVELOPING BLOCK IN WHICH THE DEFECTIVE WAFER WAS PROCESSED
S3
IDENTIFY PROCESSING MODULES AND A UNIT BLOCK IN WHICH A DEFECTIVE WAFER WAS PROCESSED
S4
S5
IS THE TRANSPORT STOP CRITERION MET?
NO
YES
S6
IS THE CURRENT ABNORMALITY-RELATED INSPECTION ITEM THE SAME AS THE PREVIOUS ABNORMALITY-RELATED INSPECTION ITEM?
NO
YES
S7
DID THE CURRENT DEFECTIVE WAFER PASS THROUGH THE SAME COATING BLOCK AS THE PREVIOUS DEFECTIVE WAFER?
NO
YES
S9
ALARM DISPLAYED
STOP WAFER TRANSPORT TO THE COATING BLOCK IN WHICH THE DEFECTIVE WAFERS WERE PROCESSED
S8
END

FIG. 11

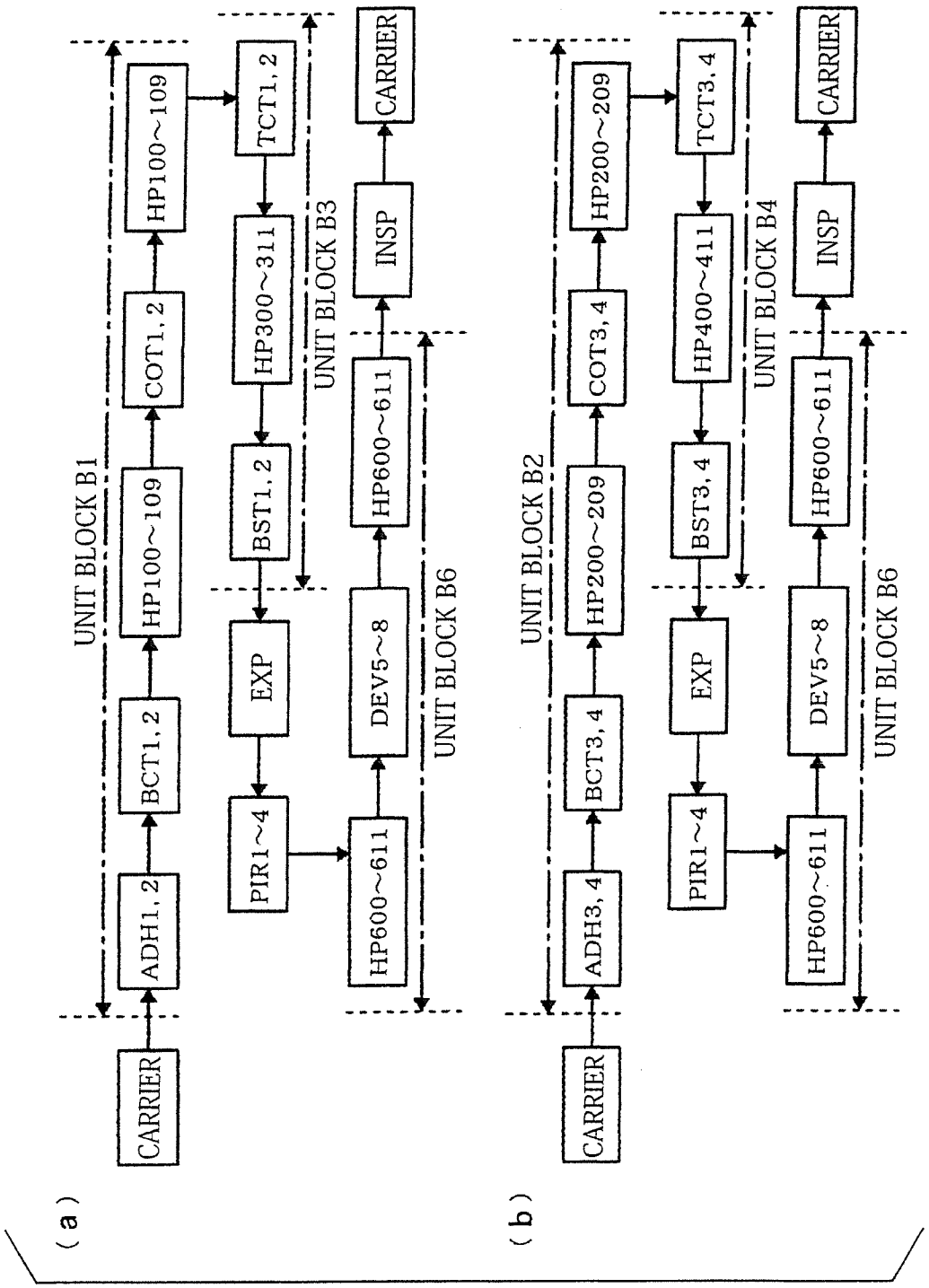

(a)
CARRIER
ADH1, 2
BCT1, 2
HP100~109
COT1, 2
HP100~109
TCT1, 2
HP300~311
BST1, 2
EXP
PIR1~4
HP600~611
DEV5~8
HP600~611
INSP
CARRIER
UNIT BLOCK B1
UNIT BLOCK B3
UNIT BLOCK B6
(b)
CARRIER
ADH3, 4
BCT3, 4
HP200~209
COT3, 4
HP200~209
TCT3, 4
HP400~411
BST3, 4
EXP
PIR1~4
HP600~611
DEV5~8
HP600~611
INSP
CARRIER
UNIT BLOCK B2
UNIT BLOCK B4
UNIT BLOCK B6

FIG. 12

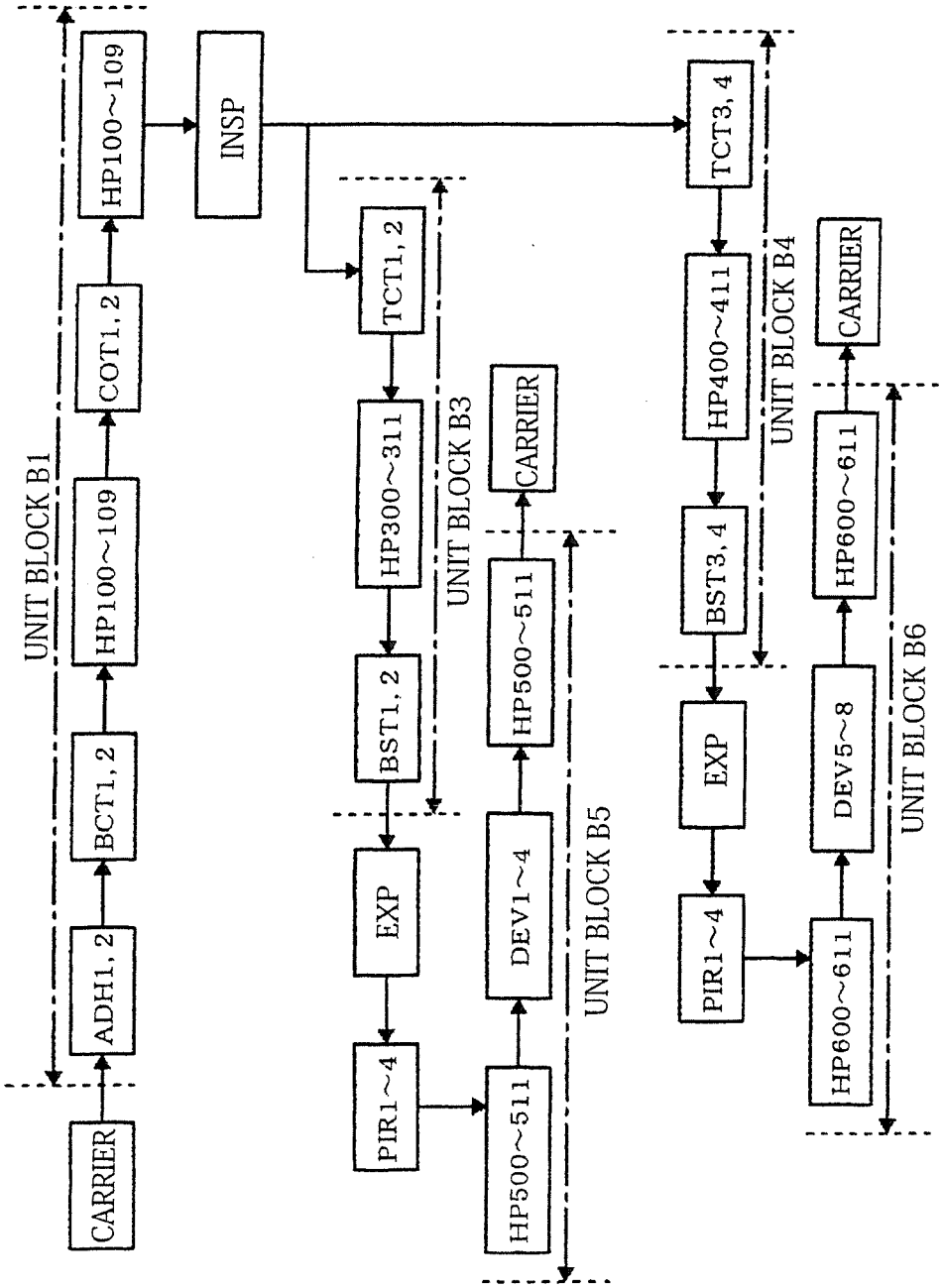

CARRIER
ADH1, 2
BCT1, 2
HP100~109
COT1, 2
HP100~109
UNIT BLOCK B1
INSP
PIR1~4
EXP
BST1, 2
HP300~311
TCT1, 2
UNIT BLOCK B3
HP500~511
DEV1~4
HP500~511
CARRIER
UNIT BLOCK B5
PIR1~4
EXP
BST3, 4
HP400~411
TCT3, 4
UNIT BLOCK B4
HP600~611
DEV5~8
HP600~611
CARRIER
UNIT BLOCK B6

FIG. 13

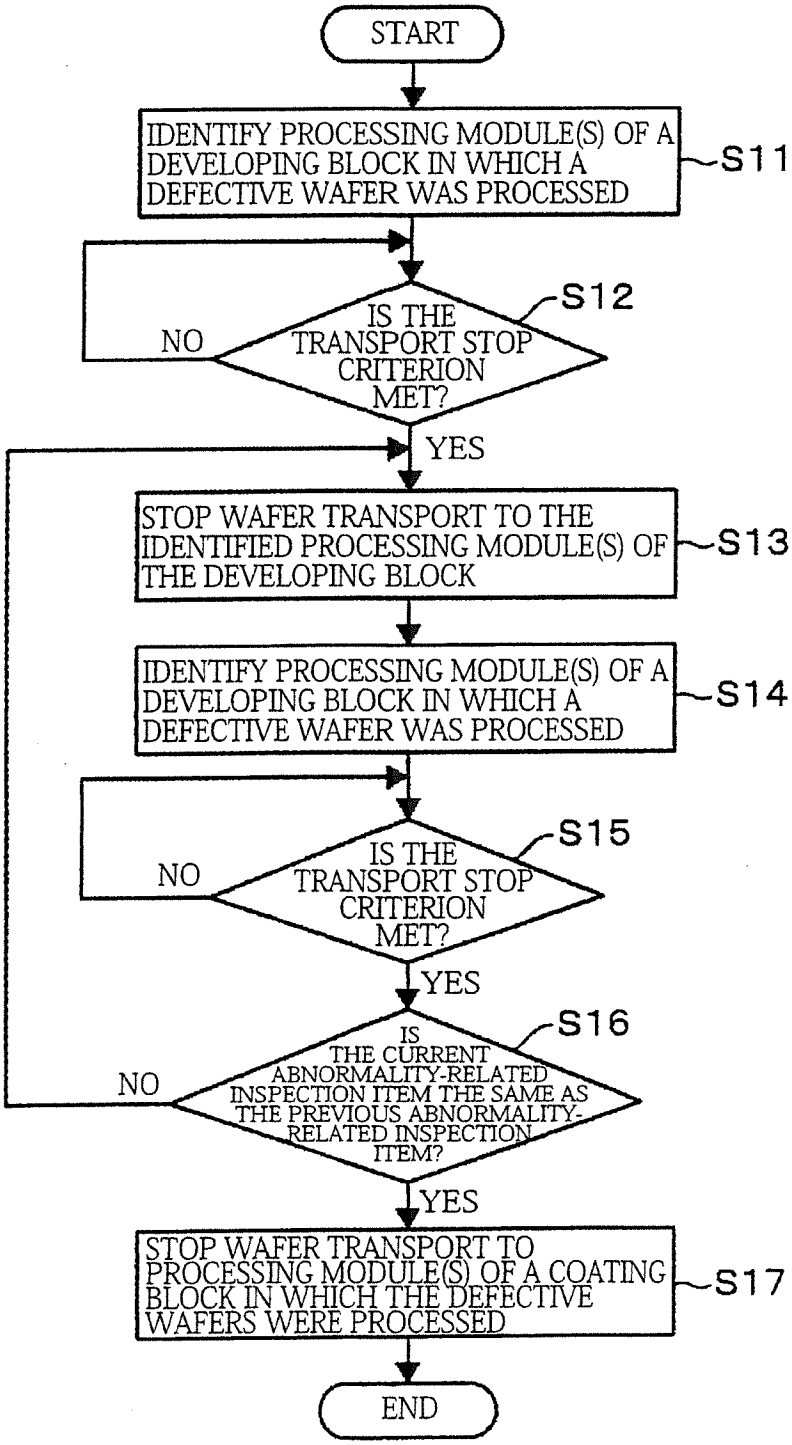

START
IDENTIFY PROCESSING MODULE(S) OF A DEVELOPING BLOCK IN WHICH A DEFECTIVE WAFER WAS PROCESSED
S11
IS THE TRANSPORT STOP CRITERION MET?
S12
NO
YES
STOP WAFER TRANSPORT TO THE IDENTIFIED PROCESSING MODULE(S) OF THE DEVELOPING BLOCK
S13
IDENTIFY PROCESSING MODULE(S) OF A DEVELOPING BLOCK IN WHICH A DEFECTIVE WAFER WAS PROCESSED
S14
IS THE TRANSPORT STOP CRITERION MET?
S15
NO
YES
IS THE CURRENT ABNORMALITY-RELATED INSPECTION ITEM THE SAME AS THE PREVIOUS ABNORMALITY-RELATED INSPECTION ITEM?
S16
NO
YES
STOP WAFER TRANSPORT TO PROCESSING MODULE(S) OF A COATING BLOCK IN WHICH THE DEFECTIVE WAFERS WERE PROCESSED
S17
END

FIG. 14

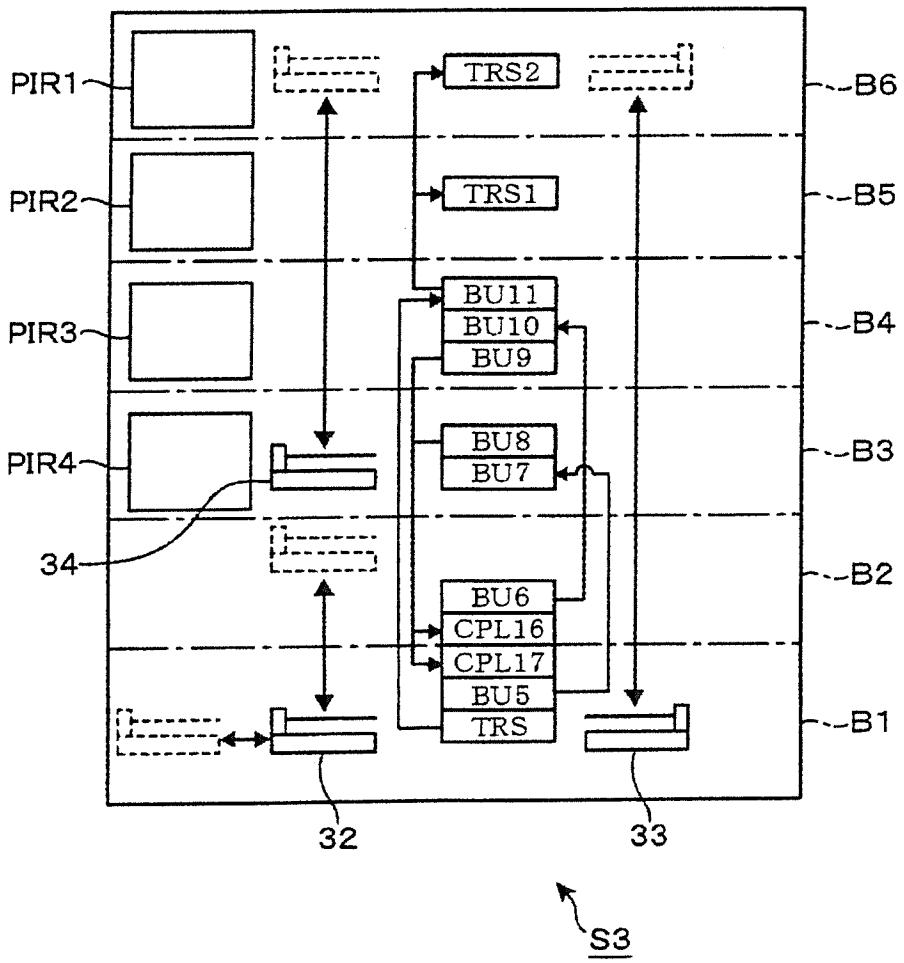

PIR1
PIR2
PIR3
PIR4
34
TRS2
TRS1
BU11
BU10
BU9
BU8
BU7
BU6
CPL16
CPL17
BU5
TRS
B6
B5
B4
B3
B2
B1
32
33
S3

FIG. 15

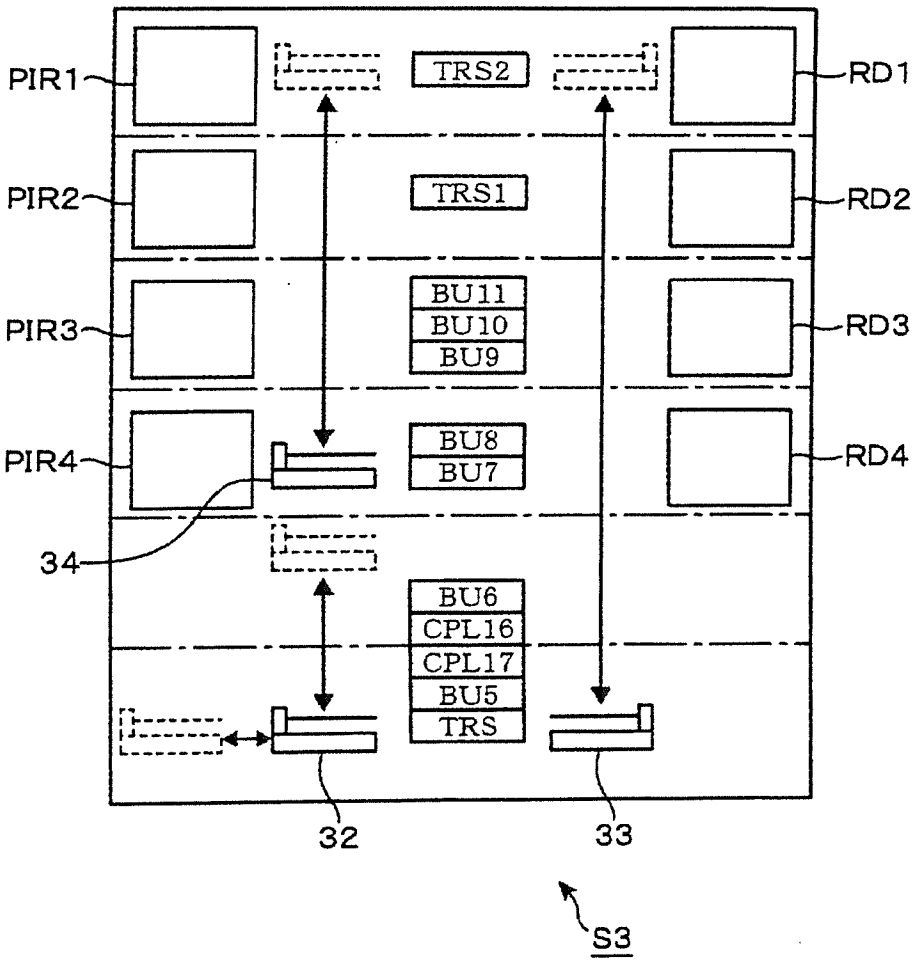

PIR1
PIR2
PIR3
PIR4
34
TRS2
TRS1
BU11
BU10
BU9
BU8
BU7
BU6
CPL16
CPL17
BU5
TRS
RD1
RD2
RD3
RD4
32
33
S3

FIG. 16

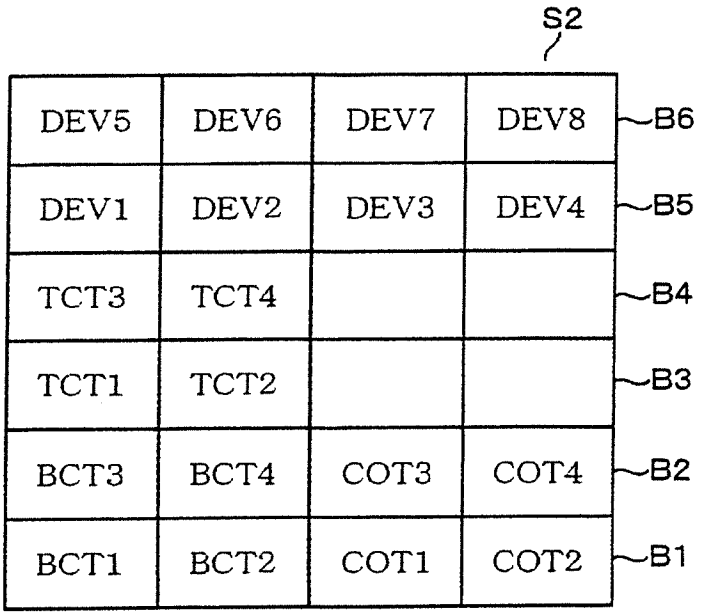

S2
DEV5
DEV6
DEV7
DEV8
B6
DEV1
DEV2
DEV3
DEV4
B5
TCT3
TCT4
B4
TCT1
TCT2
B3
BCT3
BCT4
COT3
COT4
B2
BCT1
BCT2
COT1
COT2
B1

FIG. 17

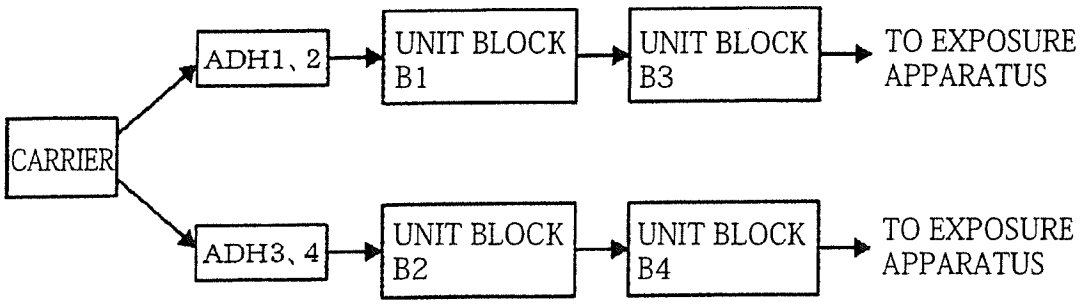

CARRIER
ADH1、2
ADH3、4
UNIT BLOCK B1
UNIT BLOCK B2
UNIT BLOCK B3
UNIT BLOCK B4
TO EXPOSURE APPARATUS
TO EXPOSURE APPARATUS

FIG. 18

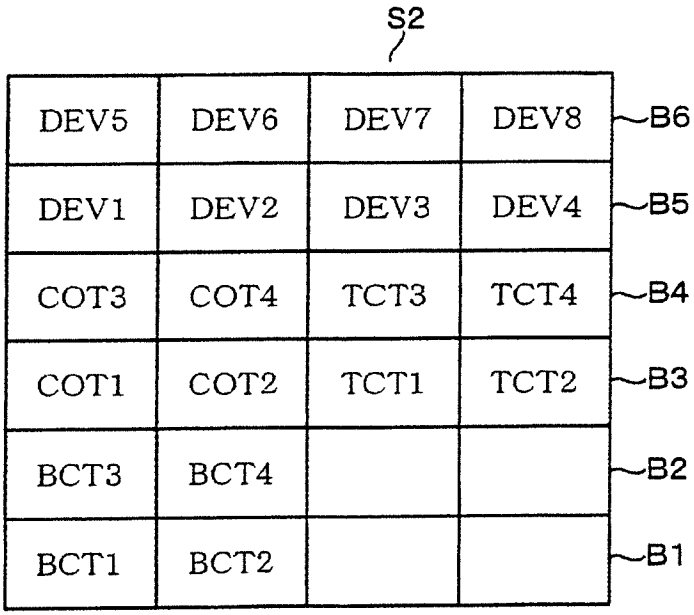

S2
DEV5
DEV6
DEV7
DEV8
B6
DEV1
DEV2
DEV3
DEV4
B5
COT3
COT4
TCT3
TCT4
B4
COT1
COT2
TCT1
TCT2
B3
BCT3
BCT4
B2
BCT1
BCT2
B1

FIG. 19

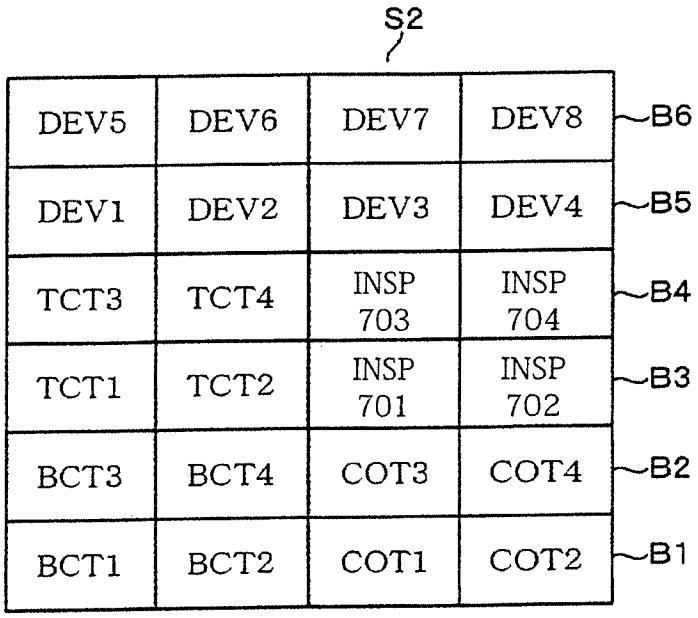

S2
DEV5
DEV6
DEV7
DEV8
B6
DEV1
DEV2
DEV3
DEV4
B5
TCT3
TCT4
INSP 703
INSP 704
B4
TCT1
TCT2
INSP 701
INSP 702
B3
BCT3
BCT4
COT3
COT4
B2
BCT1
BCT2
COT1
COT2
B1

FIG. 20

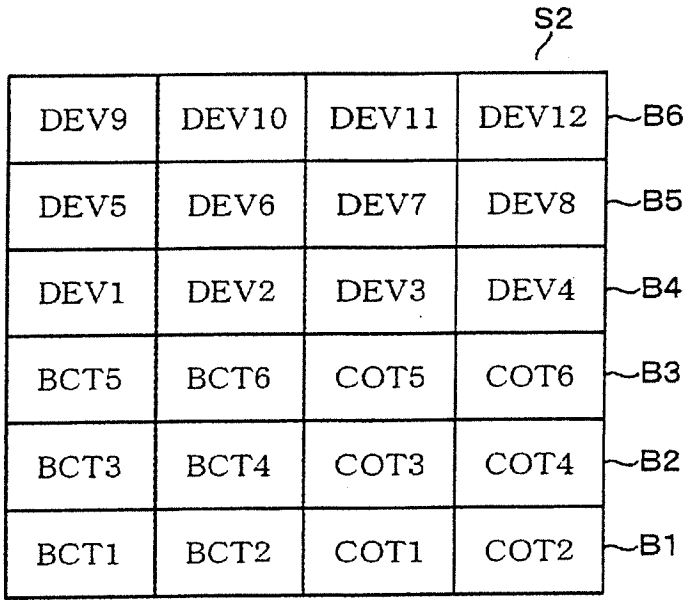

S2
DEV9
DEV10
DEV11
DEV12
B6
DEV5
DEV6
DEV7
DEV8
B5
DEV1
DEV2
DEV3
DEV4
B4
BCT5
BCT6
COT5
COT6
B3
BCT3
BCT4
COT3
COT4
B2
BCT1
BCT2
COT1
COT2
B1

FIG. 21