METHODS OF FORMING ELECTRICAL INTERCONNECT STRUCTURES USING POLYMER RESIDUES TO INCREASE ETCHING SELECTIVITY THROUGH DIELECTRIC LAYERS

Field of the Invention

The present invention relates to integrated circuit fabrication methods and, more particularly, to methods of fabricating integrated circuit devices having electrical interconnect structures therein.

Background of the Invention

Conventional methods of forming integrated circuit devices may include steps to form single and/or dual damascene structures using copper (Cu) as an electrical interconnect material. As illustrated by FIGS. 1A-1E, a conventional damascene process may utilize a multi-layered mask structure to support selective etching of one or more underlying dielectric layers. In particular, FIG. 1A illustrates steps to form a relatively porous low-k inter-layer dielectric (ILD) layer **12** on an underlying dielectric layer **10**, which may be a inter-metal dielectric (IMD) layer. This low-k ILD layer **12** may be formed of a material, such as SiCOH, which has a dielectric constant less than a dielectric constant of silicon dioxide (SiO_2). FIG. 1A also illustrates steps to form a multi-layered mask (MLM) layer on the ILD layer **12**. This multi-layered mask layer is illustrated as including a hard mask layer **14** (e.g., SiO_2 layer), an organic planarization layer (OPL) **16**, a low temperature oxide (LTO) layer **18**, an antireflective coating (ARC) **20** and a patterned photoresist (PR) layer **22**. As illustrated by FIG. 1B, a selective etching step is performed to etch through the antireflective coating **20**, the LTO layer **18** and the OPL layer **16** in sequence using the patterned photoresist layer **22** as an etching mask. The patterned photoresist layer **22** and the antireflective coating **20** are then removed.

Referring now to FIGS. 1C-1D, another selective etching step is performed to etch through and form a via opening within the hard mask layer **14** and the ILD layer **12** and define a recess within the IMD layer **10**, using the patterned OPL layer **16** as an etching mask. The patterned OPL layer **16** is then removed. This OPL layer **16** may be removed using an ashing process that is performed in an oxygen ambient. Unfortunately, this ashing process may operate to convert sidewall portions of a SiCOH-type ILD layer **12**, which are exposed to the ashing process, into silicon dioxide. This conversion process may occur in response to the removal of carbon (C) and hydrogen (H) atoms from the ILD layer **12**. Thereafter, as illustrated by FIG. 1E, a cleaning process using a diluted hydrofluoric acid (DHF) solution may cause an undercutting (i.e., recession) of the sidewalls of the ILD layer **12** relative to the hard mask layer **14** because DHF operates as an etchant to silicon dioxide. This undercutting of the sidewalls of the ILD layer **12** may result in the formation of voids within an electrically conductive via (e.g., copper plug, not shown) that is subsequently formed within the opening in the hard mask layer **14** and the ILD layer **12**. The formation of such voids may result in reduced device yield by reducing the reliability of electrical interconnects within an integrated circuit chip.

Summary of the Invention

Embodiments of the present invention include methods of forming electrical interconnect structures that are compatible with damascene fabrication techniques. These methods include forming an electrical interconnect structure by forming a first dielectric layer having a first dielectric constant on a semiconductor substrate and then forming a hard mask layer on the first dielectric layer. The hard mask layer includes a material having a second dielectric constant that is greater than the first dielectric constant. An exemplary hard mask layer may include silicon dioxide or tetraethylorthosilicate (TEOS). A photoresist layer is then patterned on an upper surface of the hard mask layer. This patterned photoresist layer is used as an etching mask during a step to selectively etch the hard mask layer and define an opening therein. This opening exposes

the first dielectric layer. The patterned photoresist layer is then stripped from the hard mask layer using an ashing process that exposes the upper surface of the hard mask layer. Following this ashing process, a portion of the first dielectric layer extending opposite the opening is selectively etched using the hard mask layer as an etching mask. During this selective etching step, polymer residues are accumulated directly on the upper surface of the hard mask layer. These polymer residues may operate to increase a degree of selectively and inhibit recession of the hard mask layer during the step of selectively etching the first dielectric layer. The etched portion of the first dielectric layer may then be exposed to a diluted hydrofluoric acid (DHF) solution.

According to further aspects of these embodiments, the step of selectively etching a portion of the first dielectric layer comprises selectively etching a portion of the first dielectric layer using a dry etching technique. This dry etching technique may include using a fluorine-based source gas. In particular, the step of selectively etching a portion of the first dielectric layer may include exposing the portion of the first dielectric layer to a first source gas including CF4 and a second source gas including H2. To achieve a desired degree of etching selectively and relatively high etch rate, a ratio of a volumetric flow rate of the second source gas relative to the first source gas is greater than about 0.25 for the case where the first source gas is CF4 and the second source gas is H2. For example, the volumetric flow rate of the second source gas may be greater than about 40 sccm and a volumetric flow rate of the first source gas may be about than about 150 sccm.

In alternative embodiments of the invention, the fluorine-based source gas includes CF4 and CHF3 and a combined volumetric flow rate of CF4 and CHF3 is in a range from about 10 sccm to about 20 sccm. This fluorine-based source gas may be used in combination with an oxygen (O_2) source gas that is supplied at a volumetric flow rate of about 10 sccm and an argon source gas that is supplied at a volumetric flow rate of about 400 sccm. In still further embodiments of the invention, the fluorine-based

source gas may include a combination of CF4 and CH2F2 or a combination of CH3F and CH2F2.

According to still further embodiments of the invention, the step of patterning a photoresist layer on the hard mask layer may be preceded by a step of depositing an antireflective coating directly on the upper surface of the hard mask layer. The stripping step may also include stripping the patterned photoresist layer and the antireflective coating from the hard mask layer. The step of selectively etching a portion of the first dielectric layer may also include etching an opening in the first dielectric layer and then forming a copper interconnect via in the etched opening.

Brief Description of the Drawings

FIGS. 1A-1E are cross-sectional views of intermediate structures that illustrate a conventional damascene process.

FIGS. 2A-2F are cross-sectional views of intermediate structures that illustrate methods of forming electrical interconnect structures according to embodiments of the present invention.

Detailed Description of Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being Aon@ another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like numbers refer to like elements throughout.

Methods of forming electrical interconnect structures according to embodiments of the present invention may include forming a single or multi-layered structure **110** on a semiconductor substrate **100**, as illustrated by FIG. 2A. This structure **110** may include, among other things, an

intermetal dielectric (IMD) layer having patterned wiring interconnects (not shown) therein. This intermetal dielectric layer may be formed using an electrically insulating material, such as a silicon dioxide layer or another dielectric having a relatively low dielectric constant, that supports a reduction in parasitic coupling capacitance between electrically conductive regions (not shown) within the intermetal dielectric layer. A first dielectric layer **120** is formed on the multi-layered structure **110**. This first dielectric layer **120** may be formed of a material having a first dielectric constant. In particular, the first dielectric layer **120** may be formed as a p-SiCOH layer having a thickness in a range from about 1000 Δ to about 3000 Δ.

Referring now to FIG. 2B, an electrically insulating hard mask layer **140** is formed directly on an upper surface of the first dielectric layer **120**. This hard mask layer **140** may be a silicon dioxide layer or other material layer (e.g., tetraethylorthosilicate (TEOS) layer) that can be selectively etched relative to the first dielectric layer **120**. Thus, the hard mask layer **140** may be formed of a material having a second dielectric constant greater than the first dielectric constant. This hard mask layer **140** may have a thickness in a range from about 150 Δ to about 600 Δ. The hard mask layer **140** is covered with an antireflective coating layer **200** that enhances accuracy of subsequently performed photolithographically-defined patterning steps. This antireflective coating layer **200** may be formed as an organic layer having a thickness in a range from about 200 Δ to about 800 Δ.

A photoresist layer is then deposited on the antireflective coating layer **200** and selectively etched (e.g., photolithographically patterned) to define a patterned photoresist layer **220**. The photoresist layer may be formed to a thickness in a range from about 1100 Δ to about 2500 Δ. As illustrated by FIGS. 2C-2D, the patterned photoresist layer **220** is used as an etching mask during a step to selectively etch the antireflective coating **200** and hard mask layer **140** in sequence to define a first opening **130** therein. This first opening exposes an upper surface of the first dielectric layer **120**. The patterned photoresist layer **220** and antireflective coating **200** are then stripped (i.e., removed) using an ashing process that exposes the upper

surface of the hard mask layer **140**. Following this ashing process, a portion of the first dielectric layer **120**, which extends opposite the first opening **130**, is selectively etched using the hard mask layer **140** as an etching mask. During this selective etching step, a layer of polymer residues **150** is accumulated directly on the upper surface of the hard mask layer **140**, as illustrated by FIG. 2E. These polymer residues within the layer **150**, which are generated as a by-product of the etching process, operate to increase a degree of etching selectively by protecting and inhibiting lateral recession of the hard mask layer **140** during the step of selectively etching the first dielectric layer **120**. As illustrated by FIG. 2F, the selective etching step may continue for a sufficient duration to define an opening (e.g., via opening) extending through the first dielectric layer **120** and possibly into the multi-layered structure **110**. The sidewalls and bottom of the opening may then be cleaned by exposing portions of the first dielectric layer **120** in the opening to a diluted hydrofluoric acid (DHF) solution. Damascene processing techniques may then be performed to form a copper interconnect via or wiring pattern **240** that fills the opening in the first dielectric layer **120**.

Referring again to FIGS. 2E-2F, the step of selectively etching the first dielectric layer **120** may include selectively etching the first dielectric layer **120** using a dry etching technique. This dry etching technique may include using a fluorine-based source gas. In particular, the step of selectively etching the first dielectric layer **120** may include exposing the first dielectric layer (in the first opening **130**) to a first source gas including CF4 and a second source gas including H2. To achieve a desired degree of etching selectively and etch rate, a ratio of a volumetric flow rate of the second source gas relative to the first source gas is greater than about 0.25 for the case where the first source gas is CF4 and the second source gas is H2. For example, the volumetric flow rate of the second source gas may be greater than about 40 sccm and a volumetric flow rate of the first source gas may be about 150 sccm.

In alternative embodiments of the invention, the fluorine-based source gas includes CF4 and CHF3 and a combined volumetric flow rate of CF4 and CHF3 is established in a range from about 10 sccm to about 20 sccm. Higher flow rates of these combined gases (CF4 and CHF3) may result in relatively low etching selectivity of the first dielectric layer **120** relative to the hard mask layer **140**. This fluorine-based source gas may also be combined with an oxygen (O_2) source gas that is supplied at a volumetric flow rate of about 10 sccm and an argon source gas that is supplied at a volumetric flow rate of about 400 sccm. In still further embodiments of the invention, the fluorine-based source gas may include a combination of CF4 and CH2F2 or a combination of CH3F and CH2F2.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A method of forming an electrical interconnect structure, comprising the steps of:

forming a first dielectric layer having a first dielectric constant on a semiconductor substrate;

forming a hard mask layer having a second dielectric constant greater than the first dielectric constant, on the first dielectric layer;

patterning a photoresist layer on an upper surface of the hard mask layer;

selectively etching the hard mask layer to define an opening therein that exposes the first dielectric layer, using the patterned photoresist layer as an etching mask;

stripping the patterned photoresist layer from the hard mask layer using an ashing process that exposes the upper surface of the hard mask layer; and

selectively etching a portion of the first dielectric layer extending opposite the opening while simultaneously accumulating polymer residues directly on the upper surface of the hard mask layer, using the hard mask layer as an etching mask.

2. The method of Claim 1, wherein said step of selectively etching a portion of the first dielectric layer comprises selectively etching a portion of the first dielectric layer using a dry etching technique.

3. The method of Claim 2, wherein the accumulated polymer residues inhibit recession of the hard mask layer during said step of selectively etching a portion of the first dielectric layer.

4. The method of Claim 2, wherein said step of selectively etching a portion of the first dielectric layer comprises exposing the portion of the first dielectric layer to a fluorine-based source gas.

5. The method of Claim 4, wherein said step of selectively etching a portion of the first dielectric layer comprises exposing the portion of the first dielectric layer to a first source gas comprising CF4 and a second source gas comprising H2.

6. The method of Claim 5, wherein the first source gas is CF4 and the second source gas is H2; and wherein a ratio of a volumetric flow rate of the second source gas relative to the first source gas is greater than about 0.25.

7. The method of Claim 6, wherein the first dielectric layer is a p-SiCOH layer.

8. The method of Claim 5, wherein a volumetric flow rate of the second source gas is greater than about 40 sccm and a volumetric flow rate of the first source gas is about 150 sccm.

9. The method of Claim 4, wherein the fluorine-based source gas comprises CF4 and CHF3.

10. The method of Claim 9, wherein a combined volumetric flow rate of CF4 and CHF3 is in a range from about 10 sccm to about 20 sccm.

11. The method of Claim 10, wherein said step of selectively etching a portion of the first dielectric layer comprises exposing the portion of the first dielectric layer to an oxygen (O_2) source gas at a volumetric flow rate of about 10 sccm and an argon source gas at a volumetric flow rate of about 400 sccm.

12. The method of Claim 4, wherein the fluorine-based source gas comprises CF4 and CH2F2.

13. The method of Claim 4, wherein the fluorine-based source gas comprises CH3F and CH2F2.

14. The method of Claim 4, wherein the fluorine-based source gas is mixed with an argon gas during said step of selectively etching a portion of the first dielectric layer.

15. The method of Claim 1, wherein the hard mask layer comprises an electrically insulating layer selected from a group consisting of silicon dioxide and tetraethylorthosilicate (TEOS).

16. The method of Claim 1, wherein said step of patterning a photoresist layer on the hard mask layer is preceded by a step of depositing an antireflective coating directly on the upper surface of the hard mask layer; and wherein said stripping step comprises stripping the patterned photoresist layer and the antireflective coating from the hard mask layer.

17. The method of Claim 1, wherein said step of selectively etching a portion of the first dielectric layer is followed by a step of exposing the etched portion of the first dielectric layer to a diluted hydrofluoric acid (DHF) solution.

18. The method of Claim 1, wherein said step of selectively etching a portion of the first dielectric layer comprises etching an opening in the first dielectric layer; and wherein said step of selectively etching a portion of the first dielectric layer is followed by a step of forming a copper interconnect via in the etched opening.

19. A method of forming an electrical interconnect structure, comprising the steps of:

forming a dielectric layer on a semiconductor substrate;

forming a hard mask layer on the dielectric layer;

patterning a photoresist layer on an upper surface of the hard mask layer;

selectively etching the hard mask layer to define an opening therein that exposes the dielectric layer, using the patterned photoresist layer as an etching mask; then

stripping the patterned photoresist layer from the hard mask layer using an ashing process; and then

selectively dry etching a portion of the dielectric layer extending opposite the opening by exposing the portion of the dielectric layer to a CF4 source gas and an H2 source gas at respective rates that establish a volumetric flow rate ratio of H2/CF4 at greater than about 0.25.

20. A method of forming an electrical interconnect structure, comprising the steps of:

forming a dielectric layer on a semiconductor substrate;

forming a hard mask layer on the dielectric layer;

patterning a photoresist layer on an upper surface of the hard mask layer;

selectively etching the hard mask layer to define an opening therein that exposes the dielectric layer, using the patterned photoresist layer as an etching mask; then

stripping the patterned photoresist layer from the hard mask layer using an ashing process; and then

selectively dry etching a portion of the dielectric layer extending opposite the opening by exposing the portion of the dielectric layer to CF4 and CHF3 source gases at a combined volumetric flow rate in a range from about 10 sccm to about 20 sccm.