METHODS AND APPARATUS FOR PROCESSING A SUBSTRATE

FIELD

[0001] Embodiments of the present disclosure generally relate to method and apparatus for processing a substrate, and more particularly, methods and apparatus for reducing overhang and improve opening width for physical vapor deposition (PVD) films deposited within a feature.

BACKGROUND

[0002] The miniaturization of semiconductor circuit elements has reached a point where feature sizes of 45 nm, 32 nm, 28 nm, 20 nm and even less are fabricated on a commercial scale. As the dimensions of features continue to get smaller, new challenges arise for process steps like filling a gap between circuit elements. As the width between the elements continues to shrink, the gap between the elements often gets taller and narrower, making the gap more difficult to fill without the gapfill material creating voids and weak seams.

[0003] Sputtering, alternatively called PVD, is used for the deposition of metals and other materials in the fabrication of semiconductor integrated circuits. Use of sputtering has been extended to depositing material layers onto the sidewalls of high aspect-ratio (HAR) holes or gaps such as vias or other vertical interconnect structures.

[0004] PVD techniques often experience an overgrowth or overhang of material at the top of the gap before the gap has been completely filled. The overhang can create a void or seam in the gap where the deposited material has been cut off by the overhang, a problem sometimes referred to as breadloafing.

[0005] Current methods of reducing overhang utilize a continuous wave (CW) bias applied to the substrate, but such methods have a limited power range. Further, CW bias can cause damage to the underlying substrate when operated at high-power levels.

SUMMARY

[0006] Methods and apparatus for processing a substrate are provided herein. In some embodiments, a method of physical vapor deposition on a substrate includes sputtering a material from a target in a physical vapor deposition (PVD) chamber to

form a material layer on a layer comprising a feature extending a depth from a top surface of the layer to a top surface of a base layer on which the layer is deposited, the feature having an opening width defined by a first sidewall and a second sidewall, the material layer having a greater lateral thickness at the top surface of the layer than a thickness on the first sidewall or the second sidewall within the feature, depositing additional material on the layer by biasing the layer with an RF bias at a low power, etching the material layer from the layer by biasing the layer with an RF bias at a high-power, and repeatedly alternating between the low power and the high-power at a predetermined frequency to reduce a difference between the lateral thickness at the top surface of the layer and the lateral thickness on the first sidewall or the second sidewall within the feature.

[0007] In accordance with at least some embodiments, a non-transitory computer readable storage medium has stored thereon instructions that when executed by a processor perform a method of physical vapor deposition on a substrate. The method includes sputtering a material from a target in a physical vapor deposition (PVD) chamber to form a material layer on a layer comprising a feature extending a depth from a top surface of the layer to a top surface of a base layer on which the layer is deposited, the feature having an opening width defined by a first sidewall and a second sidewall, the material layer having a greater lateral thickness at the top surface of the layer than a thickness on the first sidewall or the second sidewall within the feature, depositing additional material on the layer by biasing the layer with an RF bias at a low power, etching the material layer from the layer by biasing the layer with an RF bias at a high-power, and repeatedly alternating between the low power and the high-power at a predetermined frequency to reduce a difference between the lateral thickness at the top surface of the layer and the lateral thickness on the first sidewall or the second sidewall within the feature.

[0008] In accordance with at least some embodiments, a method of physical vapor deposition on a substrate includes sputtering a material from a target in a physical vapor deposition (PVD) chamber to form a material layer on a layer comprising a feature extending a depth from a top surface of the layer to a top surface of a base layer on which the layer is deposited, the feature having an opening width defined by a first sidewall and a second sidewall, the material layer having a greater lateral thickness at the top surface of the layer than a thickness on the first sidewall or the

second sidewall within the feature, depositing additional material on the layer by biasing the layer with an RF bias at a low power and at a dual frequency from about 2 MHz to about 60 MHz, etching the material layer from the layer by biasing the layer with an RF bias at a high-power and at the dual frequency from about 2 MHz to about 60 MHz, and repeatedly alternating between the low power and the high-power at a predetermined frequency within the dual frequency to reduce a difference between the lateral thickness at the top surface of the layer and the lateral thickness on the first sidewall or the second sidewall within the feature.

[0009] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0011] Figure 1 is a schematic cross-sectional view of a processing chamber, in accordance with at least some embodiments of the present disclosure.

[0012] Figures 2A-2C are diagrams of a substrate with a material layer thereon having a reduced overhang, in accordance with at least some embodiments of the present disclosure.

[0013] Figure 3 is a flowchart of a method for processing a substrate, in accordance with at least some embodiments of the present disclosure.

[0014] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0015] Embodiments of methods and apparatus for processing a substrate are provided herein. For examples, methods of physical vapor deposition on a substrate can include sputtering a material from a target in a PVD chamber to form a material layer on a layer comprising a feature extending a depth from a top surface of the layer to a top surface of a base layer on which the layer is deposited. In at least some embodiments, the feature has an opening width defined by a first sidewall and a second sidewall. The material layer can have a greater lateral thickness at the top surface of the layer than a thickness on the first sidewall or the second sidewall within the feature. Next, additional material can be deposited on the layer by biasing the layer with an RF bias at a low power. Next, the material layer can be etched from the layer by biasing the layer with an RF bias at a high-power. Next, the method can include repeatedly alternating between the low power and the high-power at a predetermined frequency to reduce a difference between the lateral thickness at the top surface of the layer and the lateral thickness on the first sidewall or the second sidewall within the feature. The methods and apparatus described herein mitigate/minimize overhang issues related to PVD processes and make subsequent metallization steps easier to achieve by providing larger top feature openings.

[0016] Figure 1 depicts a schematic side view of a processing chamber 100 (e.g., a plasma processing chamber), in accordance with at least some embodiments of the present disclosure. In some embodiments, the processing chamber 100 is a PVD processing chamber suitable for sputter depositing materials on a substrate having a given diameter. Illustrative examples of suitable PVD chambers that may be adapted to benefit from the present disclosure include those commercially available from Applied Materials, Inc., of Santa Clara, California. Other processing chambers available from Applied Materials, Inc. as well as other manufacturers may also be adapted in accordance with the embodiments described herein.

[0017] The processing chamber 100 generally includes an upper sidewall 102, a lower sidewall 103, a ground adapter 104, and a lid assembly 111 defining a body 105 that encloses an interior volume 106. An adapter plate 107 may be disposed between the upper sidewall 102 and the lower sidewall 103.

[0018] A substrate support 108 is disposed in the interior volume 106 of the processing chamber 100. The substrate support 108 is configured to support a substrate having a given diameter (e.g., 150 mm, 200 mm, 300 mm, 450 mm, or the like). A substrate transfer port 109 is formed in the lower sidewall 103 for transferring substrates into and out of the interior volume 106.

[0019] A gas source 110 is coupled to the processing chamber 100 to supply process gases into the interior volume 106. In some embodiments, process gases may include inert gases, non-reactive gases, and reactive gases, if necessary. Examples of process gases that may be provided by the gas source 110 include, but are not limited to, argon gas (Ar), helium (He), neon gas (Ne), nitrogen gas (N_2), oxygen gas (O_2), and water (H_2O) vapor, among others.

[0020] A pumping device 112 is coupled to the processing chamber 100 in communication with the interior volume 106 to control the pressure of the interior volume 106. In some embodiments, during deposition the pressure level of the processing chamber 100 may be maintained from about 0.001 mTorr to about 1 Torr.

[0021] The ground adapter 104 may support a target, such as target 114. The target 114 is fabricated from a material to be deposited on the substrate. In some embodiments, the target 114 may be fabricated from aluminum (Al), cobalt (Co), copper (Cu), indium (In), molybdenum (Mo), nickel (Ni), rhodium (Rh), ruthenium (Ru), tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, combinations thereof, or the like. In some embodiments, the processing chamber 100 is configured to deposit, for example, aluminum (Al), cobalt (Co), copper (Cu), indium (In), molybdenum (Mo), nickel (Ni), rhodium (Rh), ruthenium (Ru), tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, combinations thereof, or the like, In some embodiments, the processing chamber 100 is configured to deposit, for example, aluminum oxide (AlO_2), aluminum oxynitride (such as ALON), tantalum nitride (TaN), tantalum oxynitride (TaOxNy), Ti oxynitride (TiOxNy), or tungsten nitride (WN) on a substrate. The shape of a front surface of the target 114 can be planar or generally concave with thicker outer peripheral edges than inner diameter portions.

[0022] The target 114 may be coupled to a source assembly comprising a power supply 117 for the target 114. In some embodiments, the power supply 117 may be

an RF power supply, which may be coupled to the target 114 via a matching network 116. In some embodiments, the power supply 117 may alternatively be a DC power supply, in which case the matching network 116 is omitted. In some embodiments, the power supply 117 may include both DC and RF power sources. The power supply 117 negatively biases the target 114 with respect to the ground adapter 104 or a grounded shield to excite a plasma gas into a plasma 165. For example, regardless of the type of power supply 117, the power supplied to the target 114 excites the plasma processing gas into a plasma and positively charged ions of the plasma are accelerated towards the target 114 and sputter material from the target 114.

[0023] Additionally, in some embodiments, the target 114 may include a backing plate (not shown in Figure 1), which can be provided to improve structural stability of the target 114. The backing plate may comprise a conductive material, such as copper-zinc, copper-chrome, or the same material as the target 114, such that RF, and optionally DC, power can be coupled to the target 114 via the backing plate. Alternatively, the backing plate may be non-conductive and may include conductive elements (not shown) such as electrical feedthroughs or the like.

[0024] A magnetron 170 is positioned above the target 114 and may include a one or more magnets 172, which are rotatable along a pathway, supported by a base plate 174 connected to a shaft 176, which may be axially aligned with the central axis of the processing chamber 100 and the substrate 101. The one or more magnets 172 produce a magnetic field within the processing chamber 100 near the front face of the target 114 to generate plasma so a significant flux of ions strike the target 114, causing sputter emission of target material. The one or more magnets 172 may be rotated about the shaft 176 to increase uniformity of the magnetic field across the surface of the target 114. In general, the one or more magnets 172 may be rotated such that the innermost magnet position during rotation of the one or more magnets 172 is disposed above or outside of the diameter of the substrate being processed (e.g., the distance from the axis of rotation to the innermost position of the one or more magnets 172 is equal to or greater than the diameter of the substrate being processed).

[0025] A collimator 118 can be positioned in the interior volume 106 between the target 114 and the substrate support 108. A central region 135 of the collimator 118

generally corresponds to the diameter of the substrate being processed (e.g., is equal to or substantially equal to the diameter of the substrate). Thus, a peripheral region 133 of the collimator 118 generally corresponds to an annular region radially outward of the substrate being processed (e.g., the inner diameter of the peripheral region 133 is substantially equal to or greater than the diameter of the substrate). In some embodiments, the collimator 118 may be electrically biased to control ion flux to the substrate and neutral angular distribution at the substrate, as well as to increase the deposition rate due to the added DC bias.

[0026] The collimator 118 is coupled to an upper shield 113, which in turn is coupled to the process tool adapter 138. The process tool adapter 138 may be made from suitable conductive materials compatible with processing conditions in the processing chamber 100. An insulator ring 156 and an insulator ring 157 are disposed on either side of the process tool adapter 138 to electrically isolate the process tool adapter 138 from the ground adapter 104. The insulator rings 156, 157 may be made from suitable process compatible dielectric materials.

[0027] In some embodiments, a first set of magnets 196 may be disposed adjacent to the ground adapter 104 to assist with generating the magnetic field to guide dislodged ions from the target 114 through the peripheral region 133. In some embodiments, a second set of magnets 194 may be disposed in a position to form a magnetic field between the bottom of the collimator 118 and the substrate to guide the metallic ions dislodged from the target 114 and distribute the ions more uniformly over the substrate 101. In some embodiments, a third set of magnets 154 may be disposed between the first and second set of magnets 196, 194 and about centered with or below a substrate-facing surface of the central region 135 of the collimator 118 to further guide the metallic ions towards the center of the substrate 101.

[0028] The process tool adapter 138 includes one or more features to facilitate supporting a process tool within the interior volume 106, such as the collimator 118. For example, as shown in Figure 1, the process tool adapter 138 includes a mounting ring, or shelf 164 that extends in a radially inward direction to support the upper shield 113.

[0029] In some embodiments, a coolant channel 166 may be provided in the process tool adapter 138 to facilitate flowing a coolant through the process tool

adapter 138 to remove heat generated during processing. For example, the coolant channel 166 may be coupled to a cooling apparatus 153 (coolant source) to provide a suitable coolant, such as water (deionized water), nitrogen, argon, or other noble gas, clean dry air (CDA), or corrosive gas, etc. The coolant channel 166 advantageously removes heat from the process tool (e.g., collimator 118) that is not readily transferred to other cooled chamber components, such as the ground adapter 104.

[0030] A radially inwardly extending ledge (e.g., the mounting ring, or shelf 164) is provided to support the upper shield 113 within the central opening within the interior volume 106 of the processing chamber 100. In some embodiments the shelf 164 is disposed in a location proximate the coolant channel 166 to facilitate maximizing the heat transfer from the collimator 118 to the coolant flowing in the coolant channel 166 during use.

[0031] In some embodiments, a lower shield 120 may be provided in proximity to the collimator 118 and interior of the ground adapter 104 or the upper sidewall 102. The lower shield 120 may include a tubular body 121 having a radially outwardly extending flange 122 disposed in an upper surface of the tubular body 121. The flange 122 provides a mating interface with an upper surface of the upper sidewall 102. In some embodiments, the tubular body 121 of the lower shield 120 may include a shoulder region 123 having an inner diameter that is less than the inner diameter of the remainder of the tubular body 121. In some embodiments, the inner surface of the tubular body 121 transitions radially inward along a tapered surface 124 to an inner surface of the shoulder region 123. A shield ring 126 may be disposed in the processing chamber 100 adjacent to the lower shield 120 and intermediate of the lower shield 120 and the adapter plate 107. The shield ring 126 may be at least partially disposed in a recess 128 formed by an opposing side of the shoulder region 123 of the lower shield 120 and an interior sidewall of the adapter plate 107.

[0032] In some embodiments, the shield ring 126 may include an axially projecting annular sidewall 127 that has an inner diameter that is greater than an outer diameter of the shoulder region 123 of the lower shield 120. A radial flange 130 extends from the annular sidewall 127. The radial flange 130 includes a protrusion

132 formed on a lower surface of the radial flange 130. The protrusion 132 may be a circular ridge extending from the surface of the radial flange 130 in an orientation that is substantially parallel to the inside diameter surface of the annular sidewall 127 of the shield ring 126. The protrusion 132 is generally adapted to mate with a recess 134 formed in an edge ring 136 disposed on the substrate support 108. The recess 134 may be a circular groove formed in the edge ring 136. The engagement of the protrusion 132 and the recess 134 centers the shield ring 126 with respect to the longitudinal axis of the substrate support 108. The substrate 101 (shown supported on lift pins 140) is centered relative to the longitudinal axis of the substrate support 108 by coordinated positioning calibration between the substrate support 108 and a robot blade (not shown).

[0033] One or more additional RF power sources (e.g., bias power source) can be coupled to the processing chamber 100. For example, one or more RF power sources 180 may be coupled to the processing chamber 100 through the substrate support 108 to provide a bias power between the target 114 and the substrate support 108, which is conductive to act as an electrode. For example, a bias in the presence of a plasma within processing chamber 100 causes a negative self-bias to develop on the substrate support 108 so that sputtered material (e.g., metal ions) can be accelerated towards the substrate 101 and enter deep within any high aspect-ratio holes or features formed in the substrate 101. In some embodiments, a match network (e.g., the matching network 116) can be coupled between the RF power source 180 and the substrate support 108. In some embodiments, the RF power source 180 may have a frequency between about 400 Hz and about 60 MHz, such as about 13.56 MHz. In at least some embodiments, the RF power source can be configured to provide RF power at two or more frequencies. For example, in at least some embodiments, the RF power source can be dual frequency (e.g., from about 2 MHz to about 60 MHz, such as about 13.56 MHz to about 40 MHz) capable of providing RF power at different frequencies. In at least some embodiments, two or more RF power sources each operable to provide RF power at different frequencies can be used. For example, a first RF power source can be operable to provide RF power at a frequency of about 13.56 MHz and a second power source can be operable to provide RF power at a frequency of about 40 MHz. In at least some embodiments, an inductively coupled plasma (ICP) coil 155 (shown in

phantom) can be used to provide RF power at about 2 MHz separately. In some embodiments, the RF power source 180 provides an amplitude pulsing modulated phase-shift keying signal and provide RF power at the same frequency that the matching network 116 operates at, as will be described in greater detail below.

[0034] In operation, a robot blade (not shown) having the substrate 101 disposed thereon is extended through the substrate transfer port 109. The substrate support 108 may be lowered to allow the substrate 101 to be transferred to the lift pins 140 extending from the substrate support 108. Lifting and lowering of the substrate support 108 and/or the lift pins 140 may be controlled by a drive 142 coupled to the substrate support 108. The substrate 101 may be lowered onto a substrate receiving surface 144 of the substrate support 108. With the substrate 101 positioned on the substrate receiving surface 144 of the substrate support 108, sputter deposition may be performed on the substrate 101. The edge ring 136 may be electrically insulated from the substrate 101 during processing.

[0035] After sputter deposition, the substrate 101 may be elevated utilizing the lift pins 140 to a position that is spaced away from the substrate support 108. The elevated location may be proximate one or both of the shield ring 126 and a reflector ring 148 adjacent to the adapter plate 107. The adapter plate 107 includes one or more lamps 150 coupled to the adapter plate 107 at a position intermediate of a lower surface of the reflector ring 148 and a concave surface 152 of the adapter plate 107. The lamps 150 provide optical and/or radiant energy in the visible or near visible wavelengths, such as in the infra-red (IR) and/or ultraviolet (UV) spectrum. The energy from the lamps 150 is focused radially inward toward the backside (i.e., lower surface) of the substrate 101 to heat the substrate 101 and the material deposited thereon.

[0036] After controlling the substrate 101 to a predetermined temperature, the substrate 101 is lowered to a position on the substrate receiving surface 144 of the substrate support 108. The substrate 101 may be rapidly cooled utilizing thermal control channels 146 in the substrate support 108 via conduction. For example, the cooling apparatus 153 can be connected to the substrate support 108 and be configured to provide one or more coolants to the substrate support. The substrate

101 may be removed from the processing chamber 100 through the substrate transfer port 109 for further processing.

[0037] A controller 198 is coupled to the processing chamber 100. The controller 198 includes a central processing unit 160, a memory 158, and support circuits 162. The controller 198 is utilized to control the process sequence, regulating the gas flows from the gas source 110 into the processing chamber 100 and controlling ion bombardment of the target 114. The central processing unit 160 may be of any form of a general-purpose computer processor that can be used in an industrial setting. The software routines (e.g., instructions) can be stored in the memory 158 (e.g., non-transitory computer readable storage medium), such as random-access memory, read only memory, floppy or hard disk drive, or other form of digital storage. The support circuits 162 are conventionally coupled to the central processing unit 160 and may comprise cache, clock circuits, input/output subsystems, power supplies, and the like. The software routines, when executed by the central processing unit 160, transform the central processing unit into a specific purpose computer that controls the processing chamber 100 such that the processes disclosed below, are performed in accordance with embodiments of the present disclosure. The software routines may also be stored and/or executed by a second controller (not shown) that is located remotely from the processing chamber 100.

[0038] During processing, material is sputtered from the target 114 and deposited on the surface of the substrate 101. The target 114 and the substrate support 108 are biased relative to each other by the power supply 117 or the RF power source 180 to maintain a plasma formed from the process gases (e.g., at least one of argon (Ar), helium (He), krypton (Kr), neon (Ne), or xenon (Xe)) supplied by the gas source 110. The DC pulsed bias power applied to the collimator 118 also assists controlling ratio of the ions and neutrals passing through the collimator 118, advantageously enhancing the trench sidewall and bottom fill-up capability. The ions from the plasma are accelerated toward and strike the target 114, causing target material to be dislodged from the target 114. The dislodged target material and process gases forms a layer on the substrate 101 with desired compositions.

[0039] Figures 2A-2C are diagrams of a substrate 200 (e.g., the substrate 101) with a material layer thereon having a reduced overhang, in accordance with at least some embodiments of the present disclosure.

[0040] The substrate 200 comprises a base layer 202 and a layer 204 comprising a feature 206 (e.g., via, trench, dual damascene, etc.) extending a depth from a top surface 208 of the layer 204 to an exposed top surface 210 of the base layer 202 (Figure 2A). In at least some embodiments, the depth of the feature 206 can extend to a bottom surface of the layer 204, e.g., the top surface 210 of the base layer 202 is covered by some of the layer 204 and is not exposed. The feature 206 has an opening width W_O defined by a first sidewall 212 and a second sidewall 214. In some embodiments, the first sidewall 212 and the second sidewall 214 are opposite faces of a continuous sidewall (e.g., a circular via). The opening width W_O is about 3 nm to about 40 nm, e.g., about 10 nm, 14 nm, 16 nm, 20 nm, 22 nm, 26 nm, or 28 nm.

[0041] The base layer 202 comprises a dielectric. For example, in at least some embodiments, the base layer 302 comprises or consists essentially of silicon carbide (SiC), silicon carbonitride (SiCN), silicon nitride (SiN), silicon oxide (SiO_2), silicon oxycarbide (SiOC), silicon oxynitride (SiON). As defined herein, a material which consists essentially of a stated material comprises greater than or equal to about 95%, greater than or equal to about 98%, greater than or equal to about 99% or greater than or equal to about 99.5% of the stated material on a molar basis.

[0042] Figure 3 is a flowchart of a method 300 for processing a substrate (e.g., the substrate 200), in accordance with at least some embodiments of the present disclosure. The method 300 and processes associated therewith are controlled by the controller 198.

[0043] For example, with reference again to Figures 2A and 2B, at 302, the method 300 comprises sputtering a material (e.g., from the target 114) to form a material layer (e.g., material layer 216) on a layer comprising a feature (e.g., the feature 206) extending a depth from a top surface of the layer (e.g., the top surface 208 of the layer 204) to a top surface of a layer on which the layer is deposited (e.g., the top surface 210 of the base layer 202) in a PVD chamber (e.g., the processing chamber 100). As noted above, the material can be a conductive material

comprising at least one of aluminum (Al), cobalt (Co), copper (Cu), indium (In), molybdenum (Mo), nickel (Ni), rhodium (Rh), ruthenium (Ru), tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, combinations thereof, or the like, or a dielectric material comprising at least one of aluminum oxide (AlO_2), aluminum oxynitride (such as ALON), aluminum nitride (AlN), rhodium nitride (RhN), ruthenium nitride (RuN), silicon oxide (SiO), tantalum nitride (TaN), tantalum oxynitride (TaOxNy), titanium oxynitride (TiOxNy), or tungsten nitride (WN). As also noted above, the feature can have an opening width (e.g., W_O) defined by the first sidewall 212 and the second sidewall 214. The material layer can have a greater lateral thickness (T_L) at the top surface than a thickness (T_S) on the first sidewall or the second sidewall within the feature (see Figure 2B). In at least some embodiments, at 302, the material layer 216 can have a lateral thickness T_L at the top surface outside of the feature of about 3 nm to about 40 nm, e.g., about 10 nm, 14 nm, 16 nm, 20 nm, 22 nm, 26 nm, or 28 nm. In at least some embodiments, at 302, the material layer 216 can have a lateral thickness T_L of about 15 nm.

[0044] The difference between T_L and T_S is, typically, referred to as an overhang. The opening width W_O of the feature at the top of the feature is less than the width of the feature between the first sidewall 212 and the second sidewall 214 with the material layer 216 deposited thereon.

[0045] The method 300 continues by reducing the overhang by a deposition-etch cycle, which comprises a deposition phase and an etch phase. In at least some embodiments, during the deposition-etch cycle the deposition phase can be performed prior to the etch phase, or vice versa.

[0046] For example, next, at 304, the method 300 comprises depositing additional material on the layer 204 (e.g., over the material layer 216) by biasing the layer with an RF bias at a low power. For example, the deposition phase deposits an additional material layer on the top surface 208 (e.g., on the material layer 216) by biasing the top surface 208 with an RF bias at low power bias. For example, the low power bias can be about 5 W to about 300 W (e.g., about 70 W to about 100 W). Additionally, the low power bias can be provided at a dual frequency, e.g., 2 MHz to about 60 MHz. In at least some embodiments, as described above, the low power bias can be provided at about 13.56 MHz to about 40 MHz.

[0047] Next, at 306, the method 300 comprises etching the material layer 216 from the layer by biasing the layer with an RF bias at a high-power. For example, the etch phase etches the material layer 216 from the top surface 208 by biasing the top surface 208 with RF bias at a high-power bias. For example, the high-power bias can be about 200 W to about 3000 W (e.g., about 1000 W, about 1400 W, or about 2000 W). The inventors have found that the high-power bias cannot be applied to the top surface 208 for an extended period of time. For example, if the high-power bias is applied for too long, the base layer 302 may be damaged by the high-power bias (e.g., arcing from the substrate to other portions of the processing chamber). Accordingly, the inventors have found that by using short bursts of high-power bias and low power bias the material layer 216 may be etched without damage to the underlying base layer 302. Additionally, the high-power bias can be provided at a dual frequency, e.g., 2 MHz to about 60 MHz. In at least some embodiments, the low power bias can be provided at about 13.56 MHz to about 40 MHz. In at least some embodiments, the low power bias and the high-power bias can be provided at the same frequency or a different frequency. In some embodiments, the substrate (e.g., including the base layer 302 and the layer 204) is substantially undamaged.

[0048] Next, at 308, the method 300 comprises repeatedly alternating between the low power bias and the high-power bias (between 304 and 306) at a predetermined frequency to reduce a difference between the lateral thickness at the top surface and the lateral thickness on the first sidewall or the second sidewall within the feature. For example, during the dep-etch cycle, the deposition phase and the etch phase are repeated in an alternating fashion. In at least some embodiments, the time between the deposition phase and the etch phase is minimized. For example, in at least some embodiments, the predetermined frequency at the low power bias and the high-power bias can be about 1 Hz to about 100 kHz, e.g., about 10 kHz.

[0049] Similarly, a duty cycle, which is a time percentage of a cycle spent applying the RF bias at the high-power to the substrate surface, can be about 1% to about 99%, e.g., about 30%, about 40%, about 45%, about 50%, about 55%, about 60%, or about 70%.

[0050] During 308, a determination is made to see if the opening width W_O of the feature 206 is sufficient. For example, if the opening width W_O is not sufficient,

additional dep-etch cycles are performed at 308. For example, 308 (e.g., the dep-etch cycle) is repeated until a sufficient thickness of the overhang has been removed. For example, as illustrated in Figure 2C, after a plurality of dep-etch cycles, a substrate has a material layer 216 with a reduced overhang. That is, the difference between the reduced lateral thickness T_L at the top surface of the feature 206 and thickness T_S on the first sidewall 212 and the second sidewall 214 within the featured 206 is reduced, cf. Figure 2B with 2C, for example. In some embodiments, the thickness T_S within the feature 206 is substantially unchanged by the dep-etch cycle. Alternatively, in some embodiments, the thickness T_S within the feature 206 is increased by the dep-etch cycle.

[0051] The dep-etch cycle can deposit an additional material layer on the top surface 208 outside of the feature 206. For example, the dep-etch cycle deposits about 2 nm to about 8 nm of additional material layer on the top surface 208 outside of the feature 206. In at least some embodiments, the dep-etch cycle deposits about 4 nm to about 6 nm of an additional material layer on the top surface 208 outside of the feature 206.

[0052] After 308, if the opening width W_O is sufficient, the substrate 200 may undergo further processing. For example, in at least some embodiments, the method 300 further comprises depositing a conductive fill material within the feature 206. The conductive fill material comprises a same or different material than the material layer 216. In at least some embodiments, the conductive fill material comprises a metal (e.g., comprises at least one of cobalt (Co), copper (Cu), indium (In), iridium (Ir), molybdenum (Mo), rhodium (Rh), ruthenium (Ru), or tungsten (W) or metal alloy (e.g., CuMn, CuAl, etc.)).

[0053] In at least some embodiments, the opening width W_O of the feature 206 is about 3 nm to about 40 nm before sputtering the material, sputtering the material forms a material layer 216 with a thickness of about 15 nm on the top surface 208 outside of the feature 206, and repeatedly alternating between the low power bias and the high-power bias forms an additional material layer with a thickness of about 6 nm on the top surface 208 outside of the feature 206. In such embodiments, the opening width W_O of the feature 206 is greater than or equal to about 3 nm after sputtering the material and repeatedly alternating between the low power bias and the high-power bias.

[0054] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.