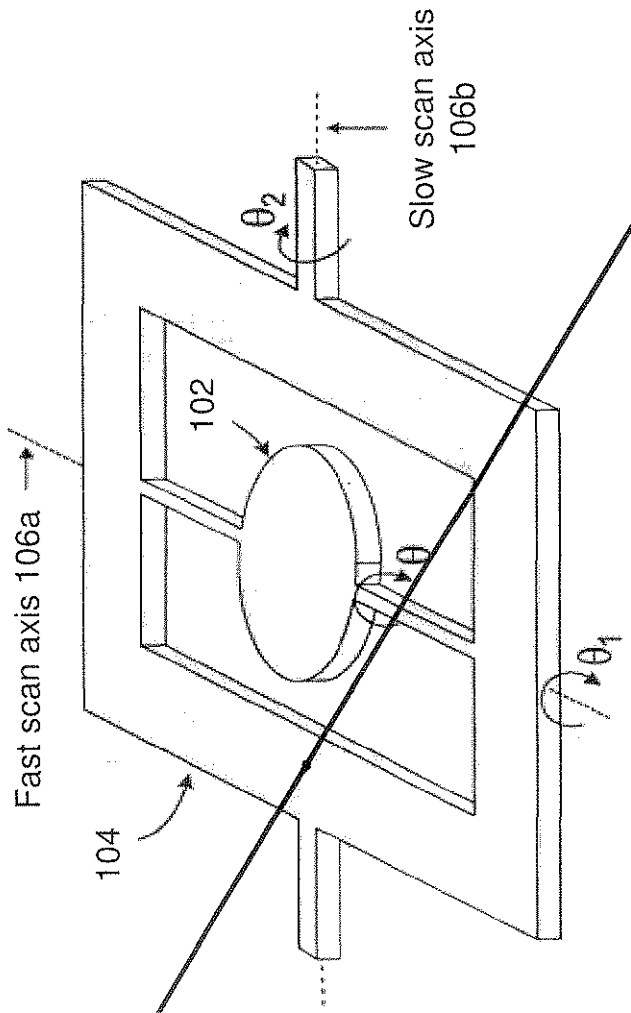

Slow scan axis
106b
θ_2
102
Fast scan axis 106a
θ
θ_1
104

FIG. 1
100

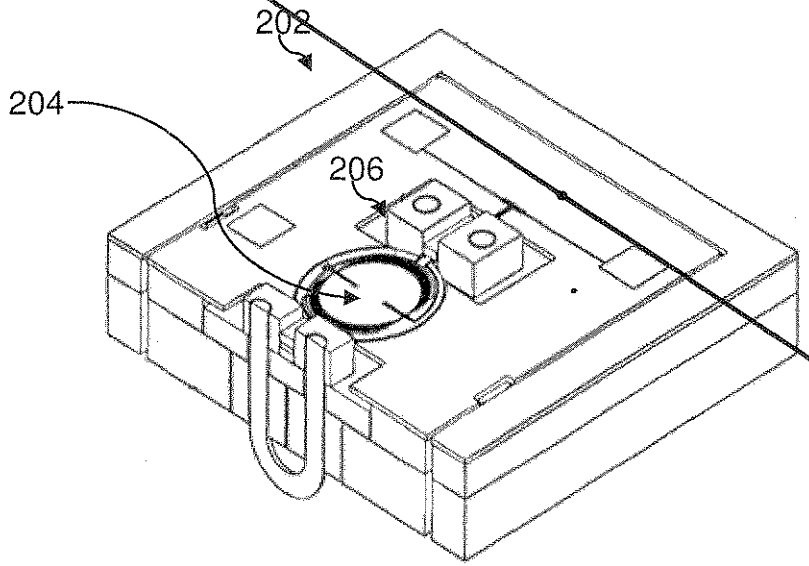


FIG. 2A
200

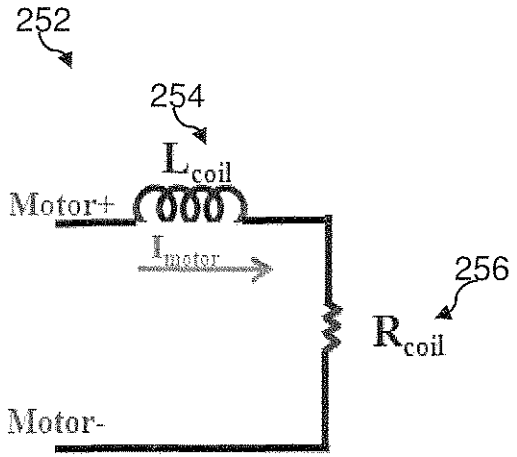


FIG. 2B
250

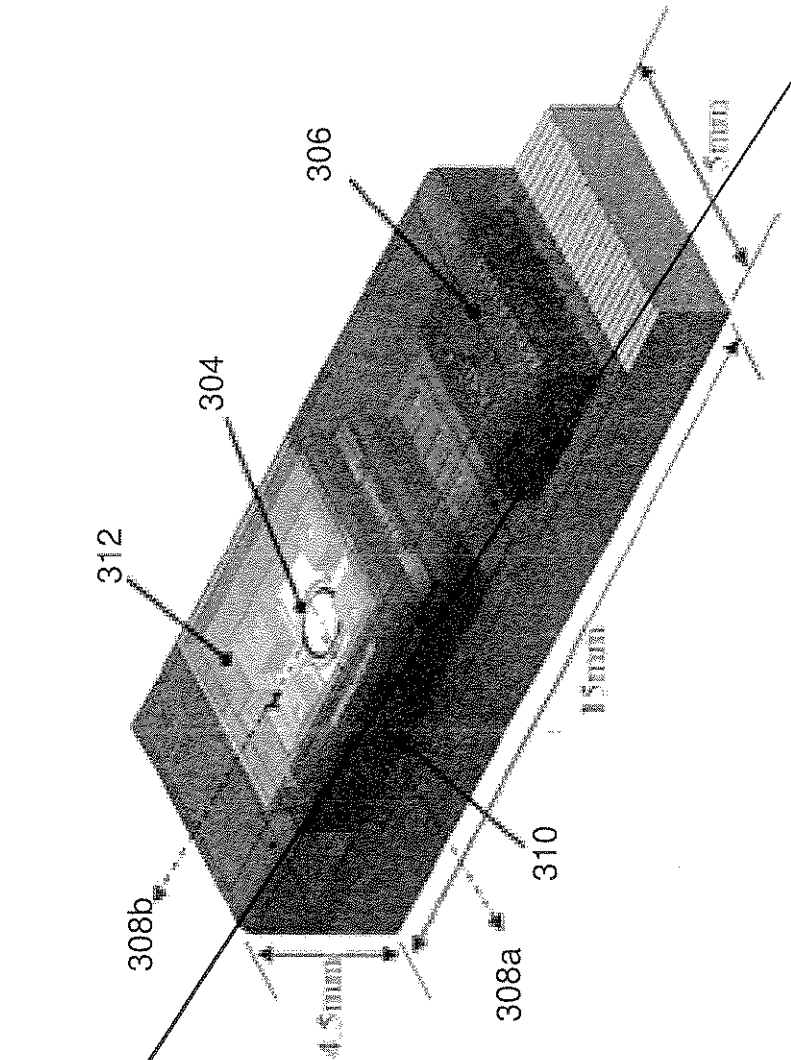


FIG. 3
300

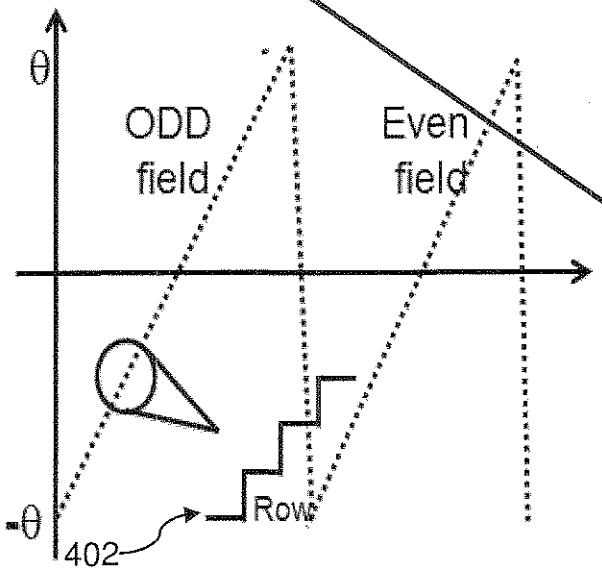


FIG. 4A
400

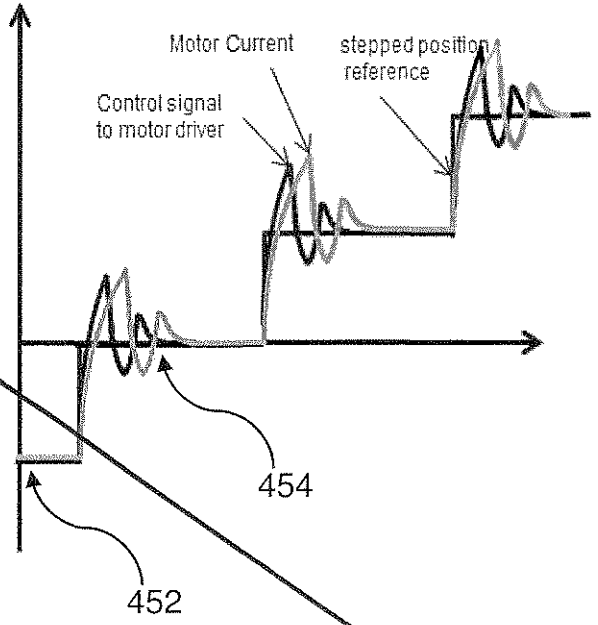


FIG. 4B
450

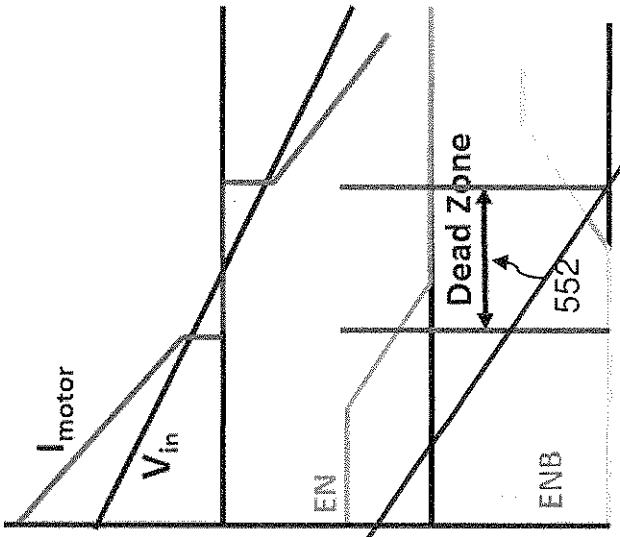


FIG. 5B
550

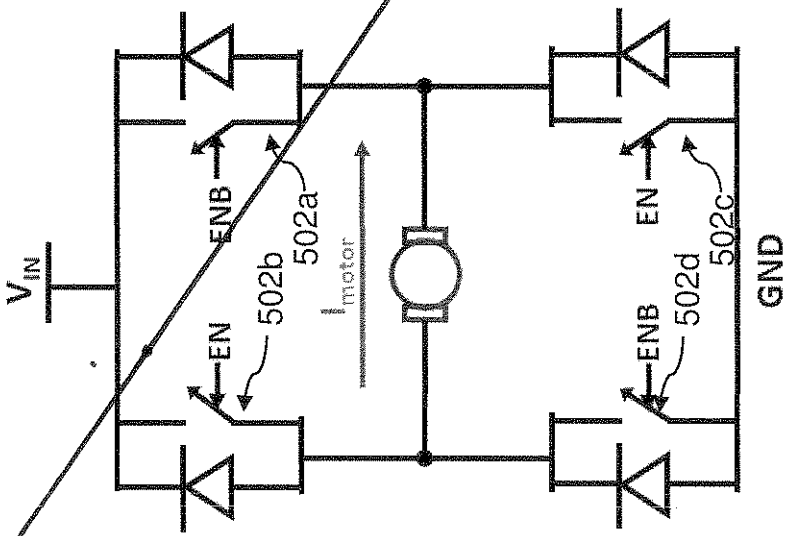


FIG. 5A
500

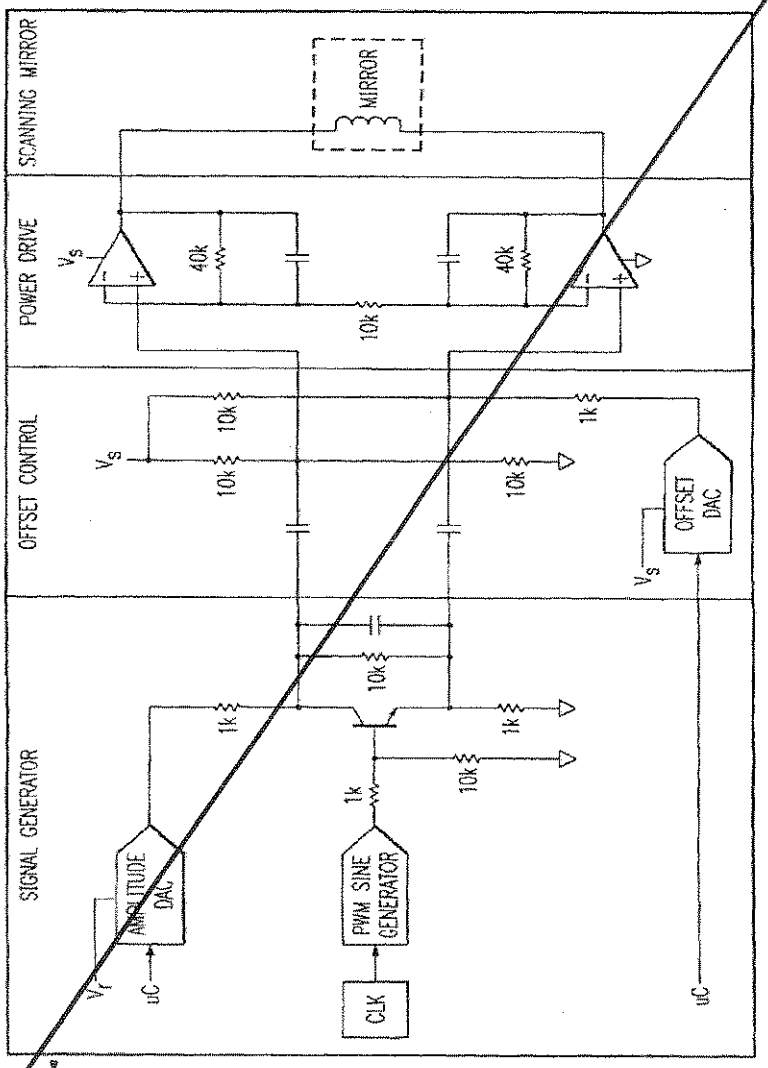

SCANNING MIRROR
MIRROR
POWER DRIVE
V_S
40k
40k
10k
OFFSET CONTROL
V_S
10k
10k
10k
1k
V_S
OFFSET DAC
SIGNAL GENERATOR
10k
1k
1k
10k
1k
AMPLITUDE DAC
PWM SINE GENERATOR
CLK
V_f
uC
uC

FIG. 6
600

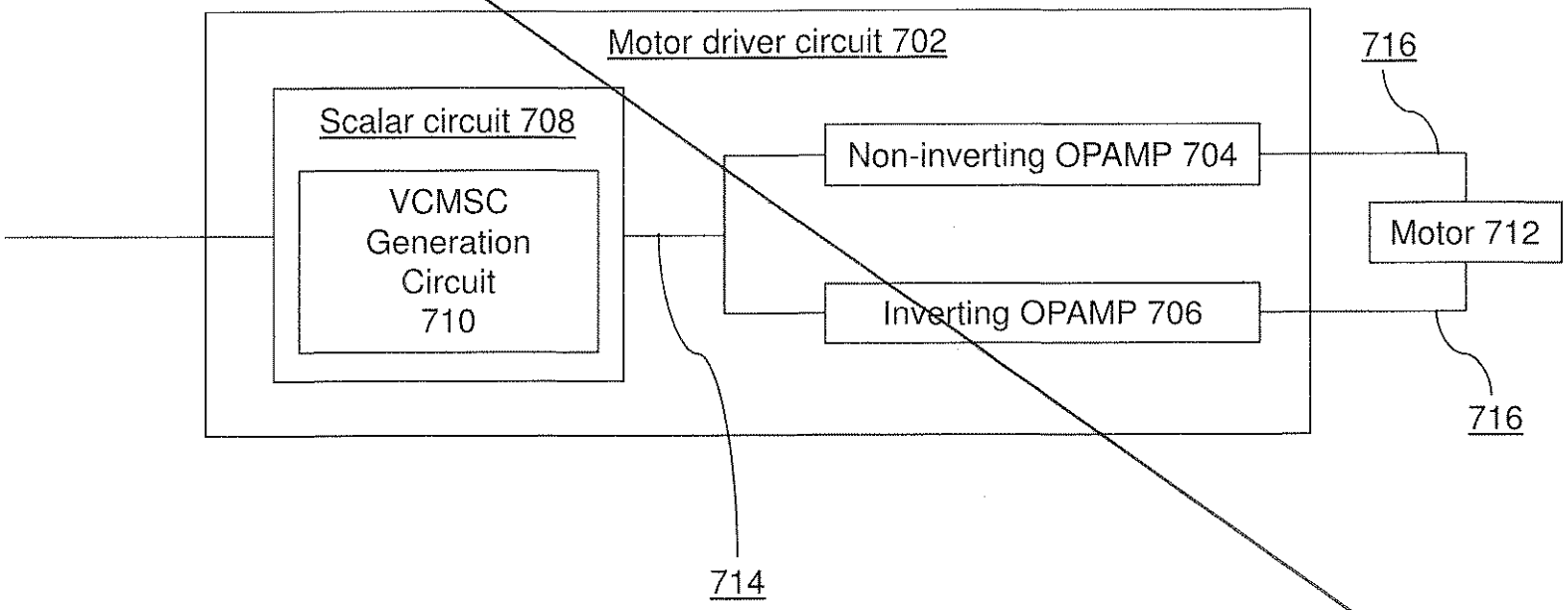

Motor driver circuit 702
Scalar circuit 708
VCMSC Generation Circuit 710
Non-inverting OPAMP 704
Inverting OPAMP 706
716
Motor 712
716
714

FIG. 7
700

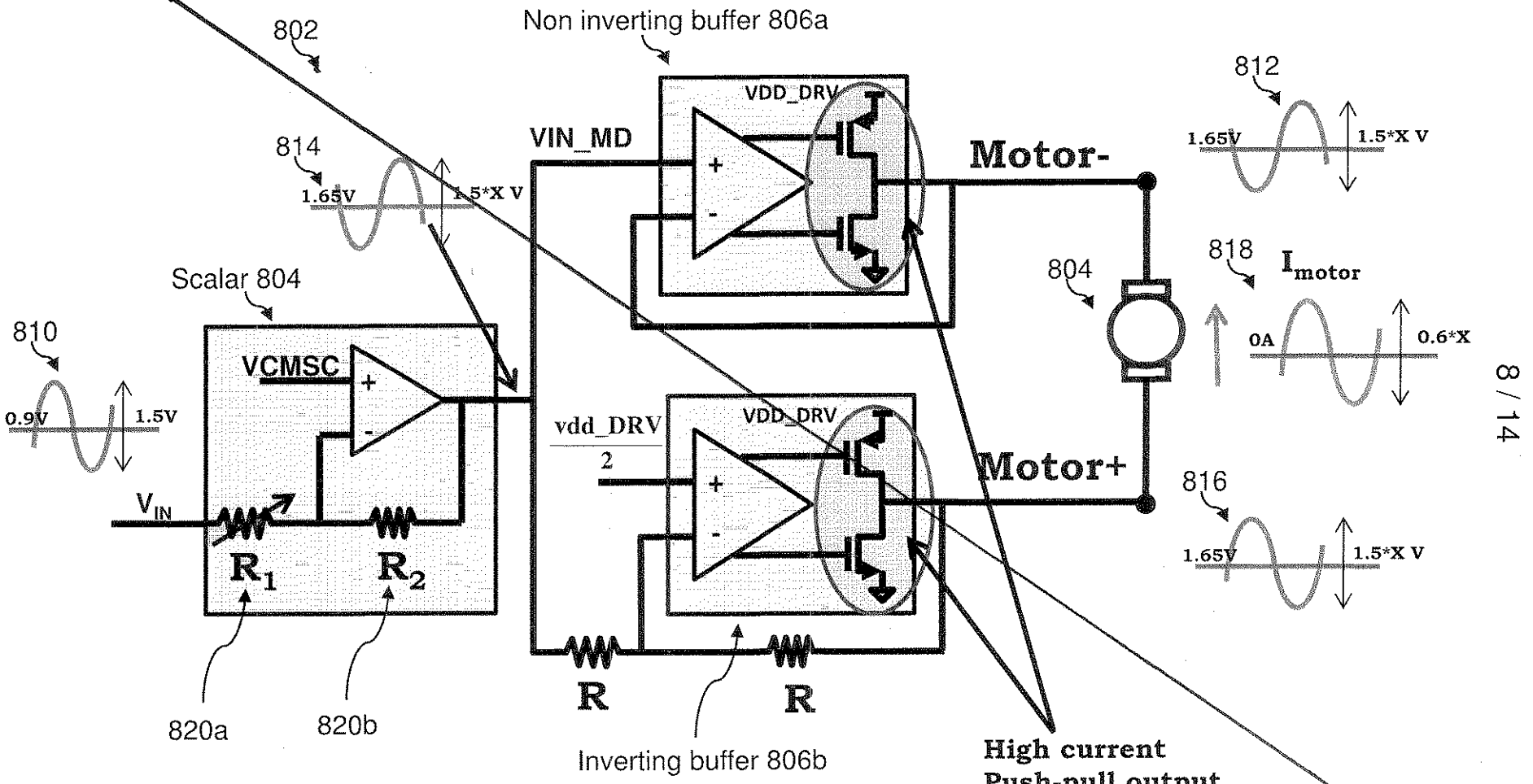

802
Non inverting buffer 806a
VDD_DRV
VIN_MD
814
1.65V
1.5*X V
Motor-
812
1.65V
1.5*X V
Scalar 804
804
818
I_{motor}
0A
0.6*X
810
0.9V
1.5V
VCMSC
vdd_DRV
2
VDD_DRV
Motor+
816
1.65V
1.5*X V
V_{IN}
R_1
R_2
R
R
820a
820b
Inverting buffer 806b
High current
Push-pull output
stage

FIG. 8
800

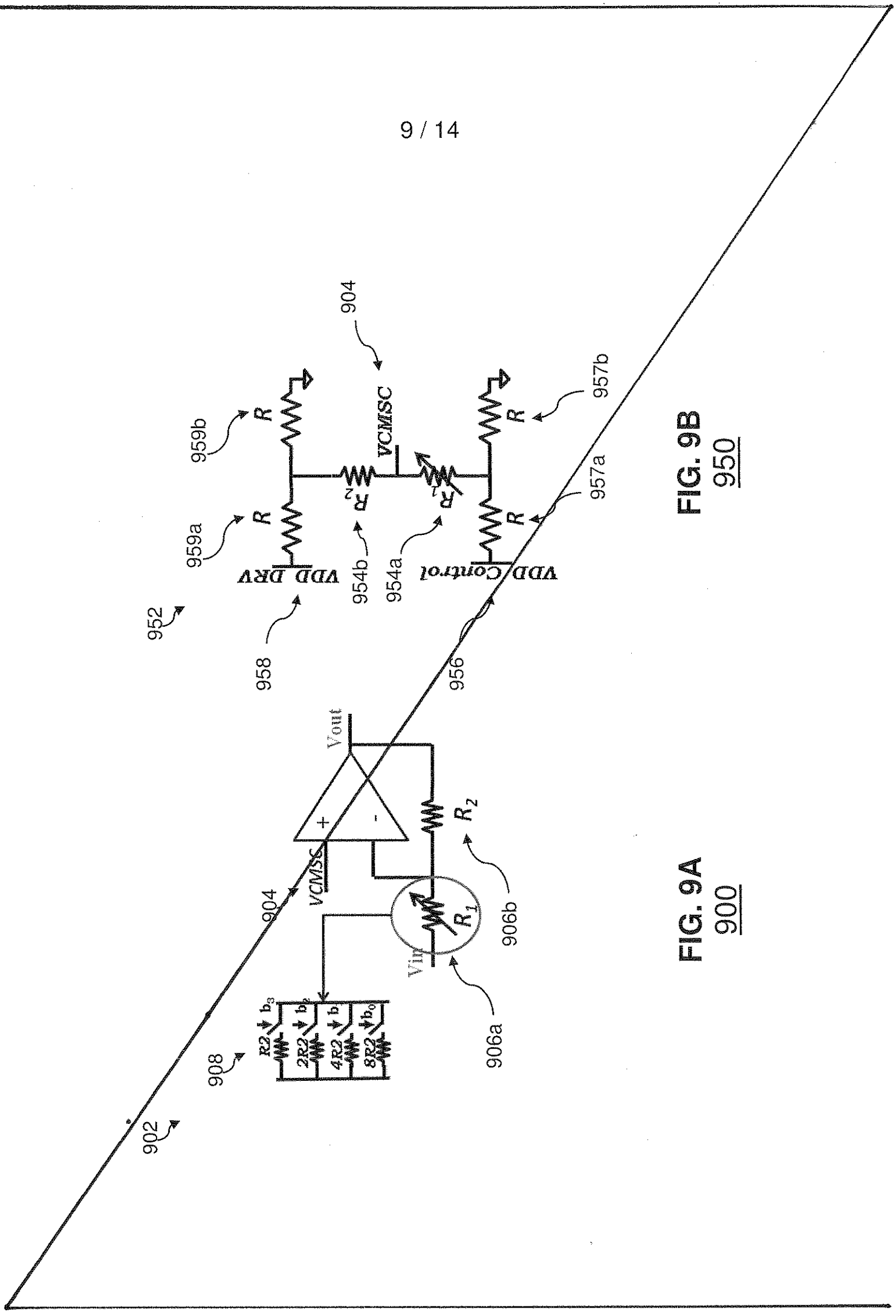
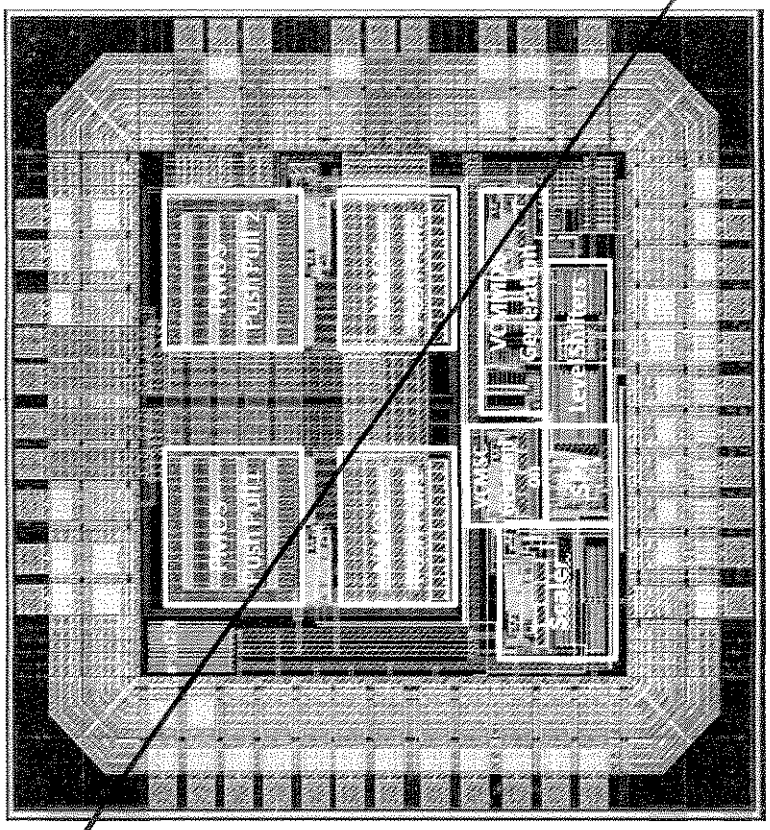


FIG. 9A
900

FIG. 9B
950



1002

FIG. 10
1000

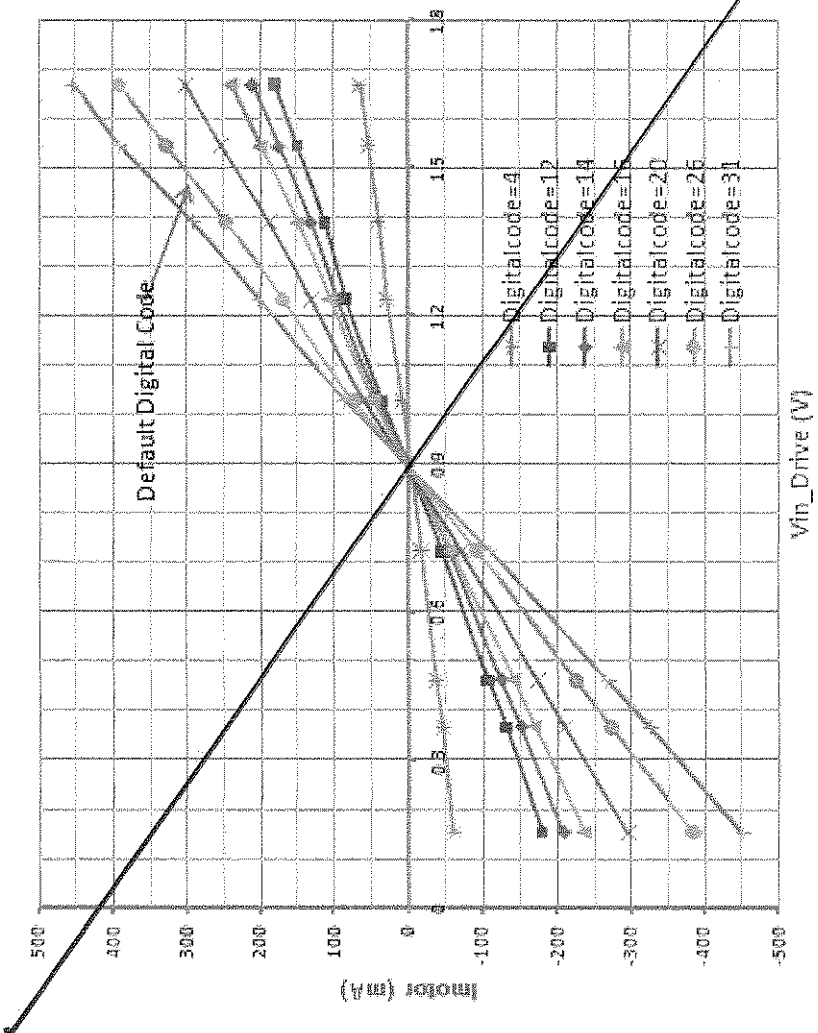

Default Digital Code
DigitalCode=4
DigitalCode=12
DigitalCode=14
DigitalCode=16
DigitalCode=20
DigitalCode=26
DigitalCode=31
Imotor (mA)
Vin_Drive (V)
500
400
300
200
100
0
-100
-200
-300
-400
-500
0
0.3
0.6
0.9
1.2
1.5
1.8

FIG. 11
1100

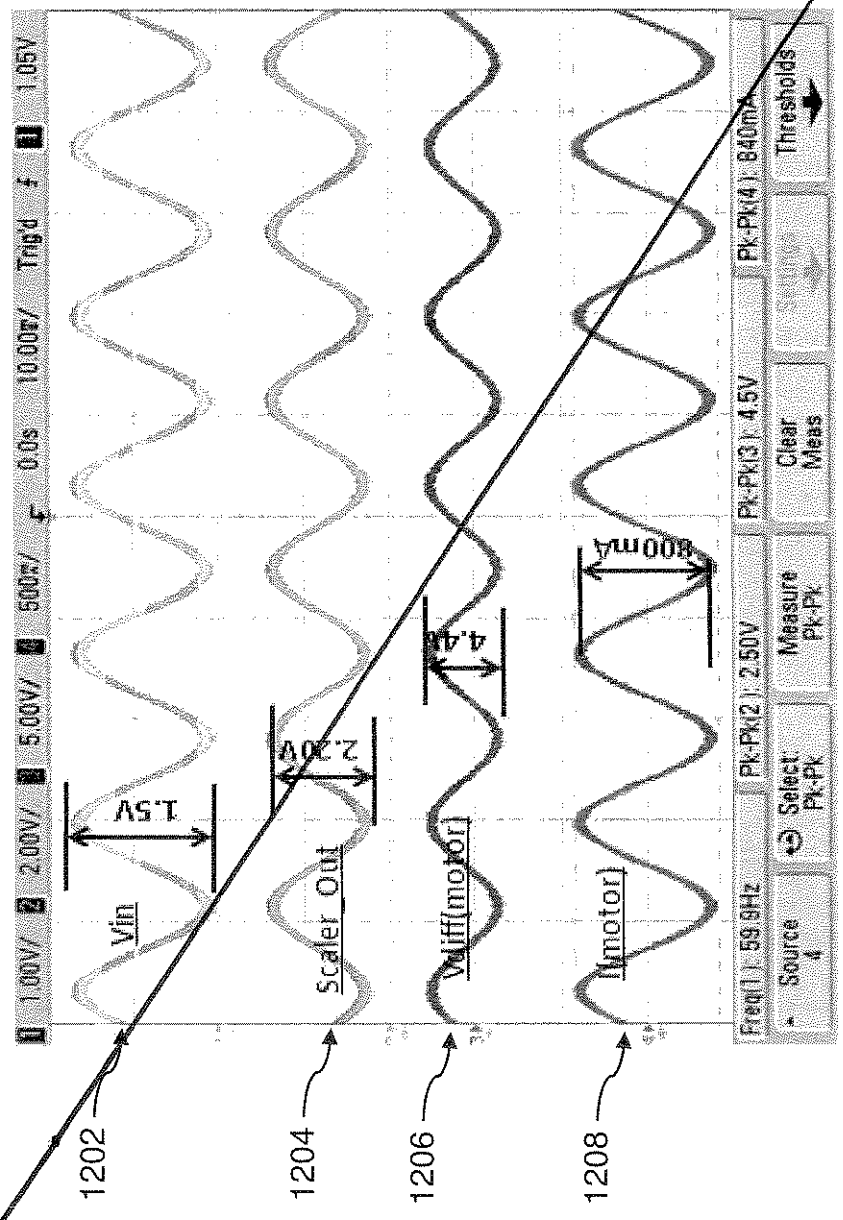

1.00V/
2.00V/
5.00V/
500s/
0.0s
10.00s/
Trig'd
1.05V
Vin
1.5V
Scaler Out
2.30V
Vdiff(motor)
4.4A
Imotor
800mA
Freq(1) 59.9Hz
Pk-Pk(2) 2.50V
Pk-Pk(3) 4.5V
Pk-Pk(4) 840mA
Source 4
Select Pk-Pk
Measure Pk-Pk
Clear Meas
Thresholds
1202
1204
1206
1208

FIG. 12
1200

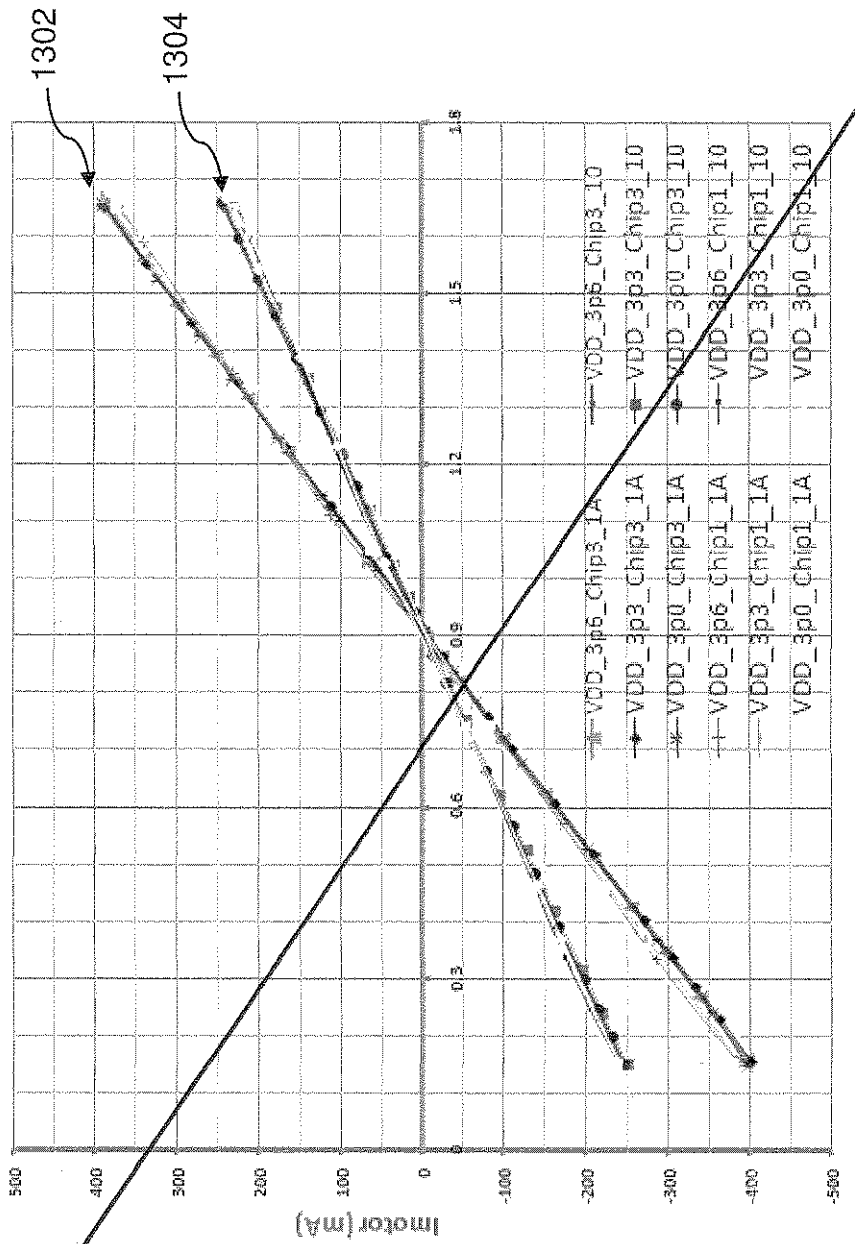

1302
1304
Imotor (mA)
Vin_Drive (V)
VDD_3p6_Chip3_1A
VDD_3p3_Chip3_1A
VDD_3p0_Chip3_1A
VDD_3p6_Chip1_1A
VDD_3p3_Chip1_1A
VDD_3p0_Chip1_1A
VDD_3p6_Chip3_10
VDD_3p3_Chip3_10
VDD_3p0_Chip3_10
VDD_3p6_Chip1_10
VDD_3p3_Chip1_10
VDD_3p0_Chip1_10

FIG. 13
1300

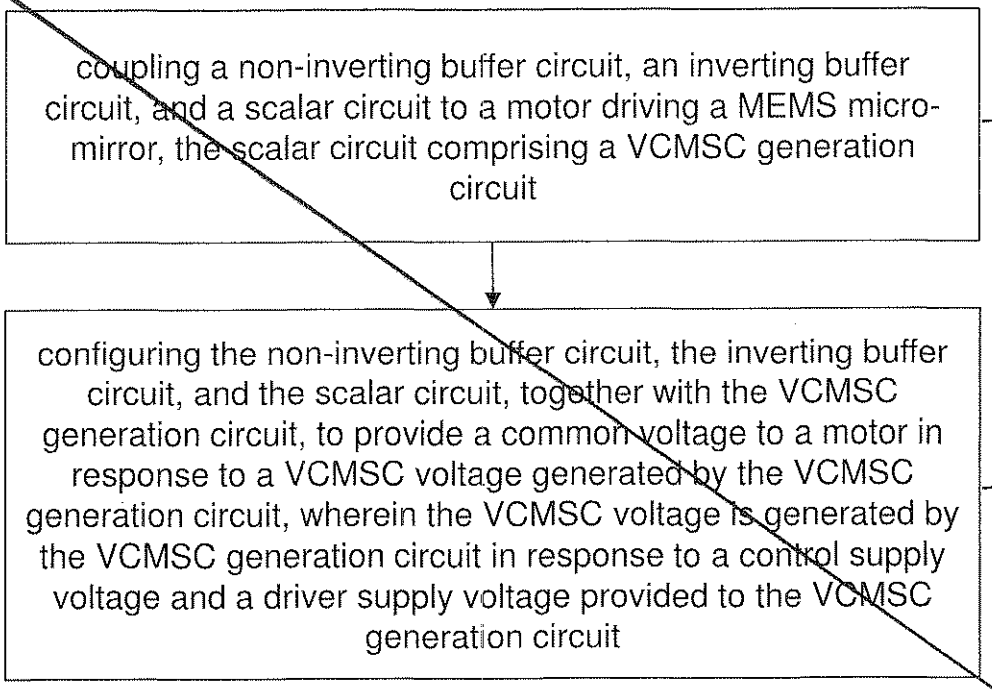

coupling a non-inverting buffer circuit, an inverting buffer circuit, and a scalar circuit to a motor driving a MEMS micro-mirror, the scalar circuit comprising a VCMSC generation circuit
1402
configuring the non-inverting buffer circuit, the inverting buffer circuit, and the scalar circuit, together with the VCMSC generation circuit, to provide a common voltage to a motor in response to a VCMSC voltage generated by the VCMSC generation circuit, wherein the VCMSC voltage is generated by the VCMSC generation circuit in response to a control supply voltage and a driver supply voltage provided to the VCMSC generation circuit
1404

FIG. 14

1400

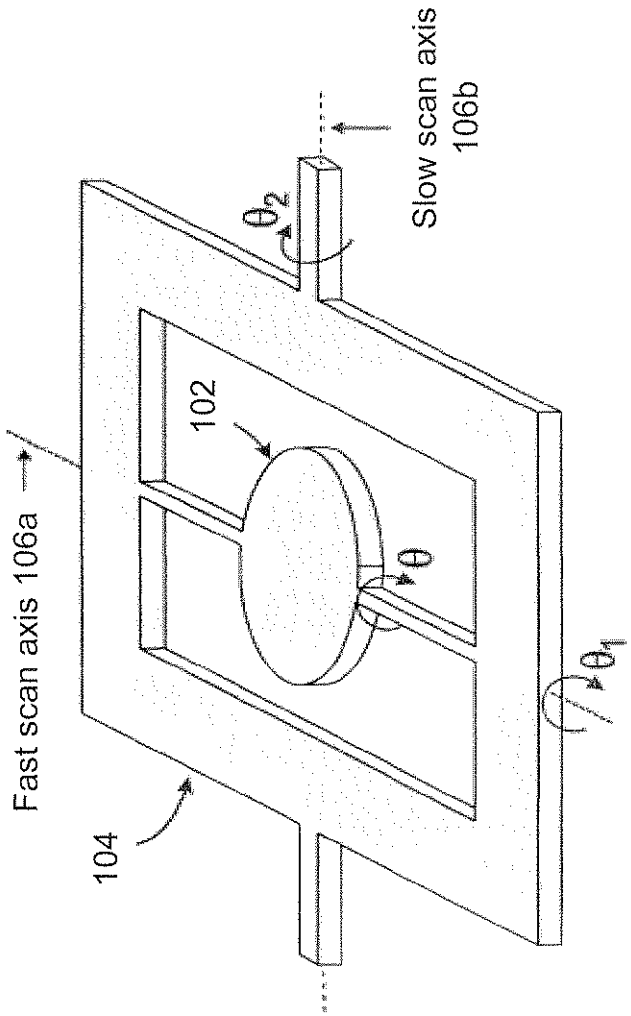


FIG. 1
100

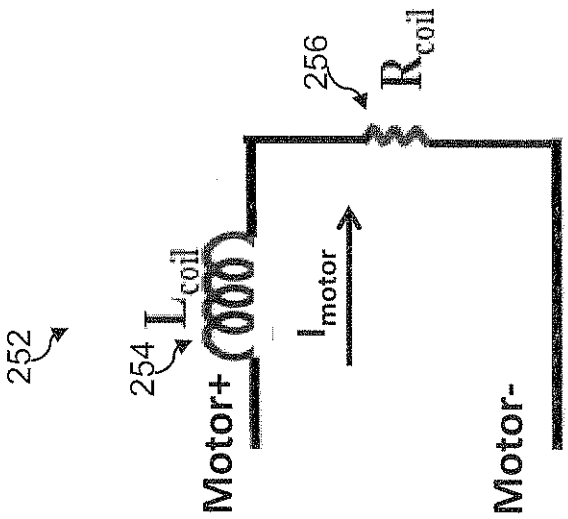


FIG. 2B
250

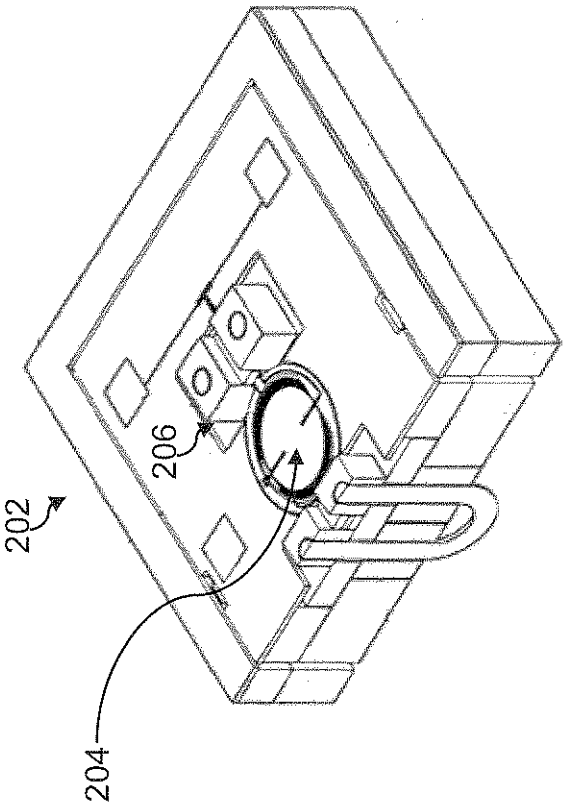


FIG. 2A
200

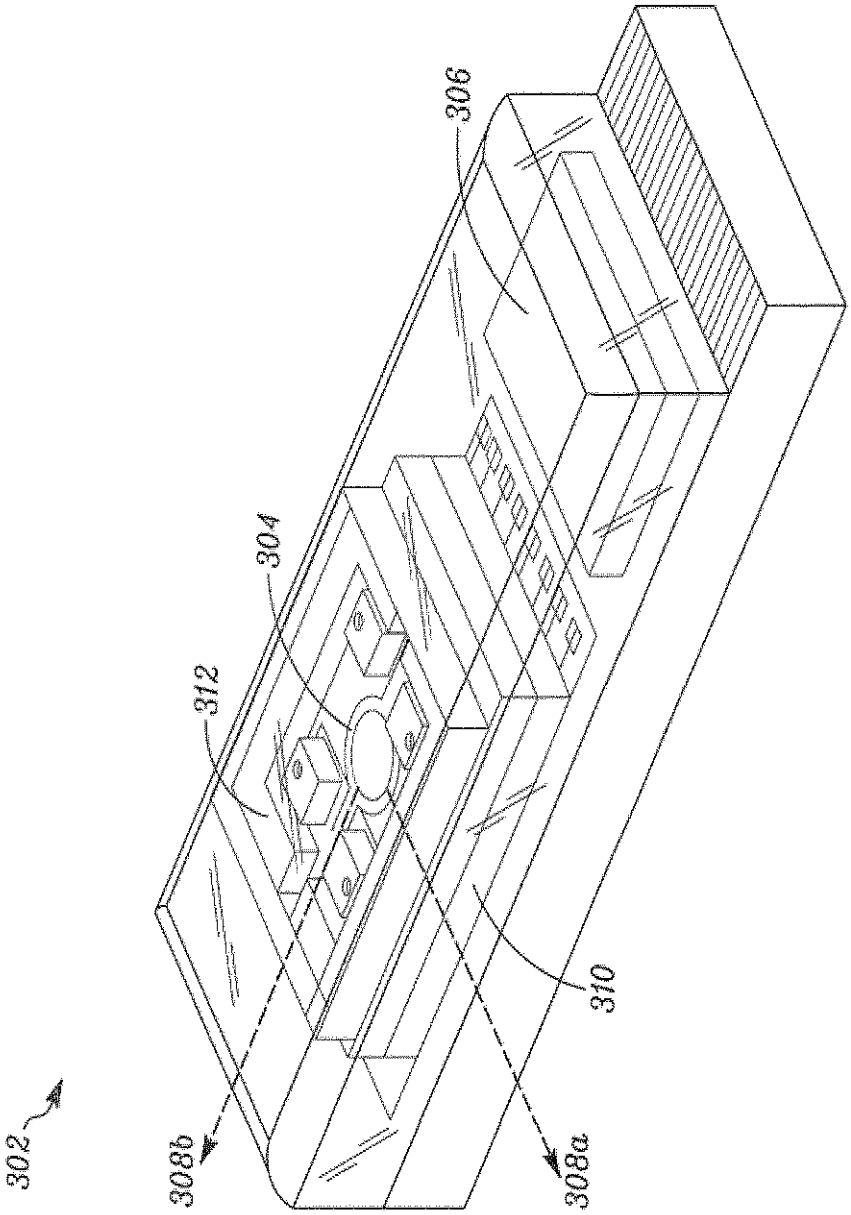


FIG. 3
300

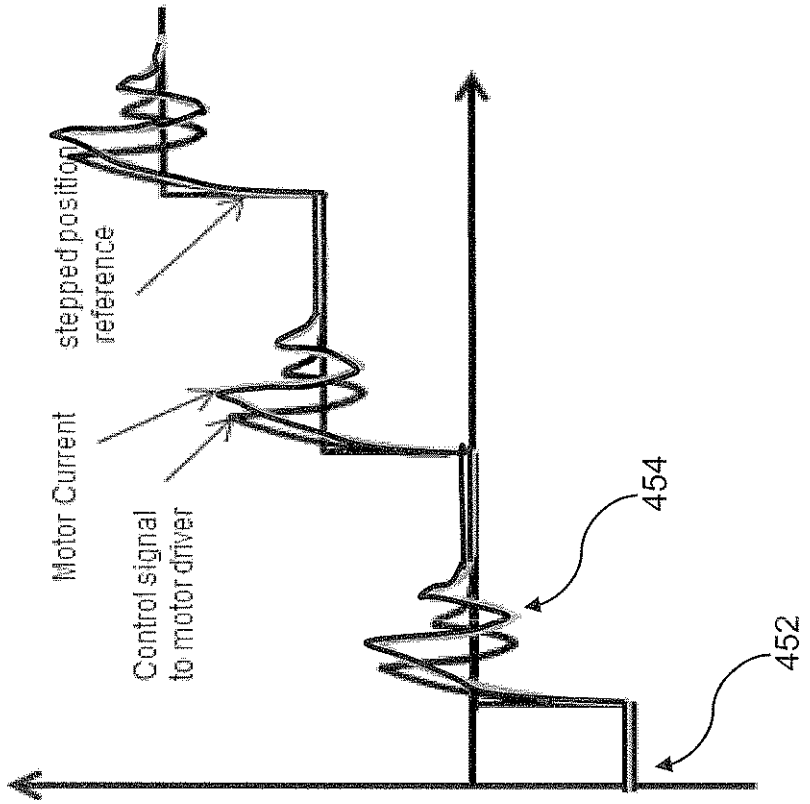


FIG. 4B
450

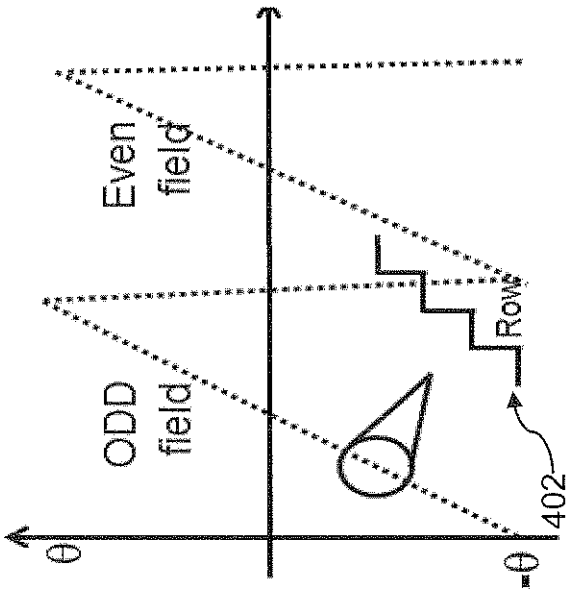


FIG. 4A
400

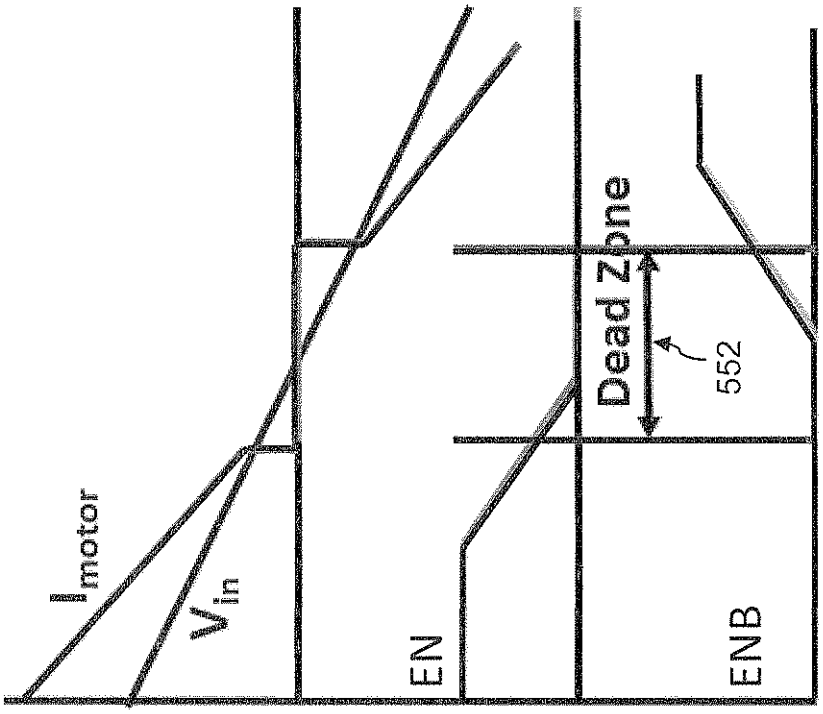


FIG. 5B
550

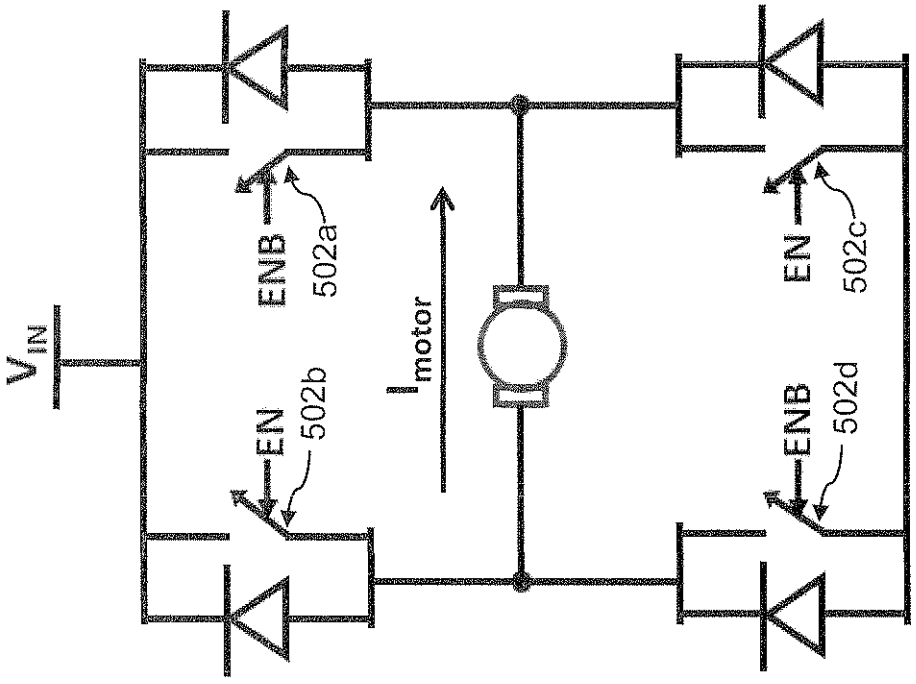


FIG. 5A
500

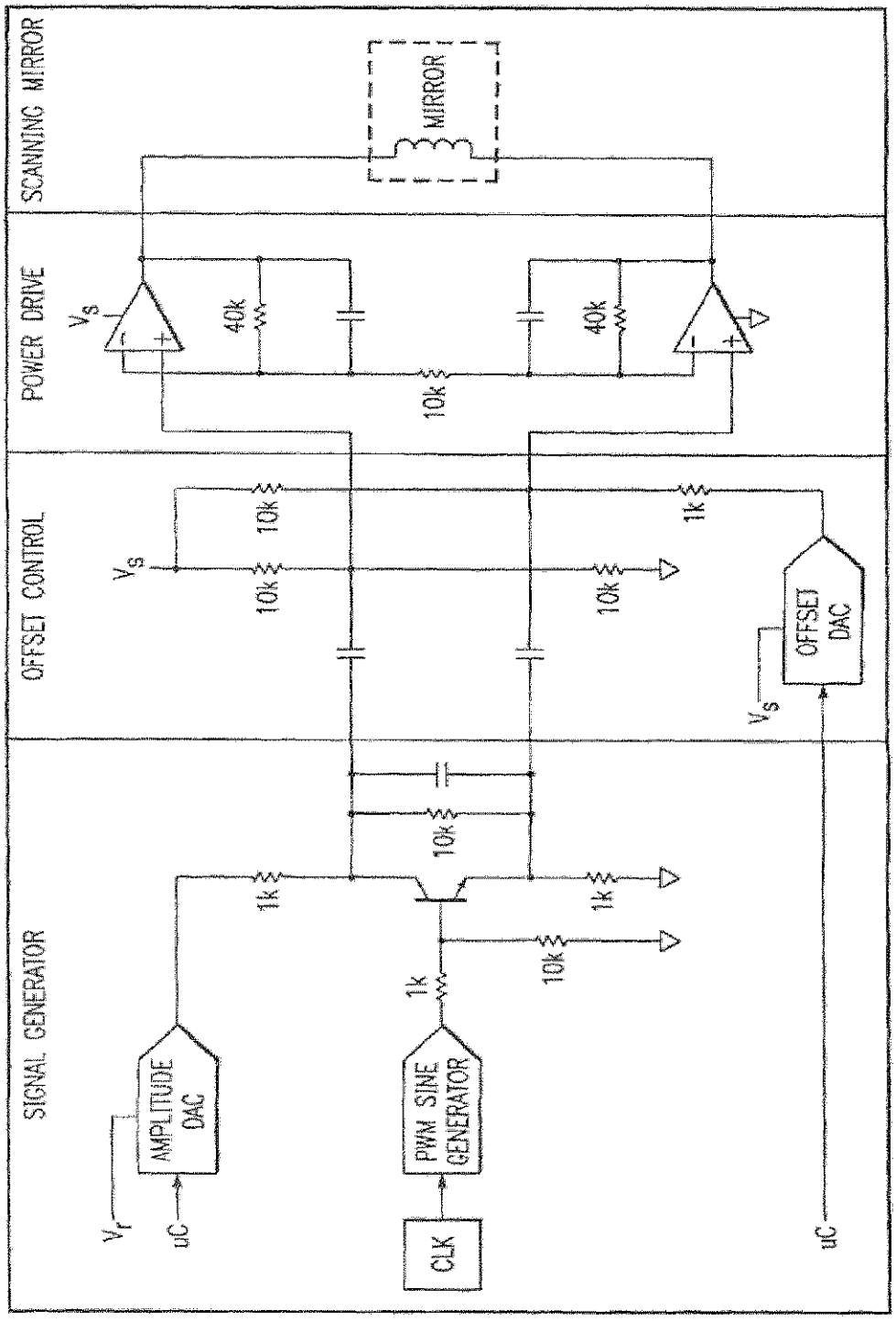

SCANNING MIRROR
MIRROR
POWER DRIVE
V_S
40k
40k
10k
OFFSET CONTROL
V_S
10k
10k
10k
1k
V_S
OFFSET DAC
SIGNAL GENERATOR
10k
1k
1k
10k
1k
AMPLITUDE DAC
PWM SINE GENERATOR
CLK
V_r
uC
uC

FIG. 6
600

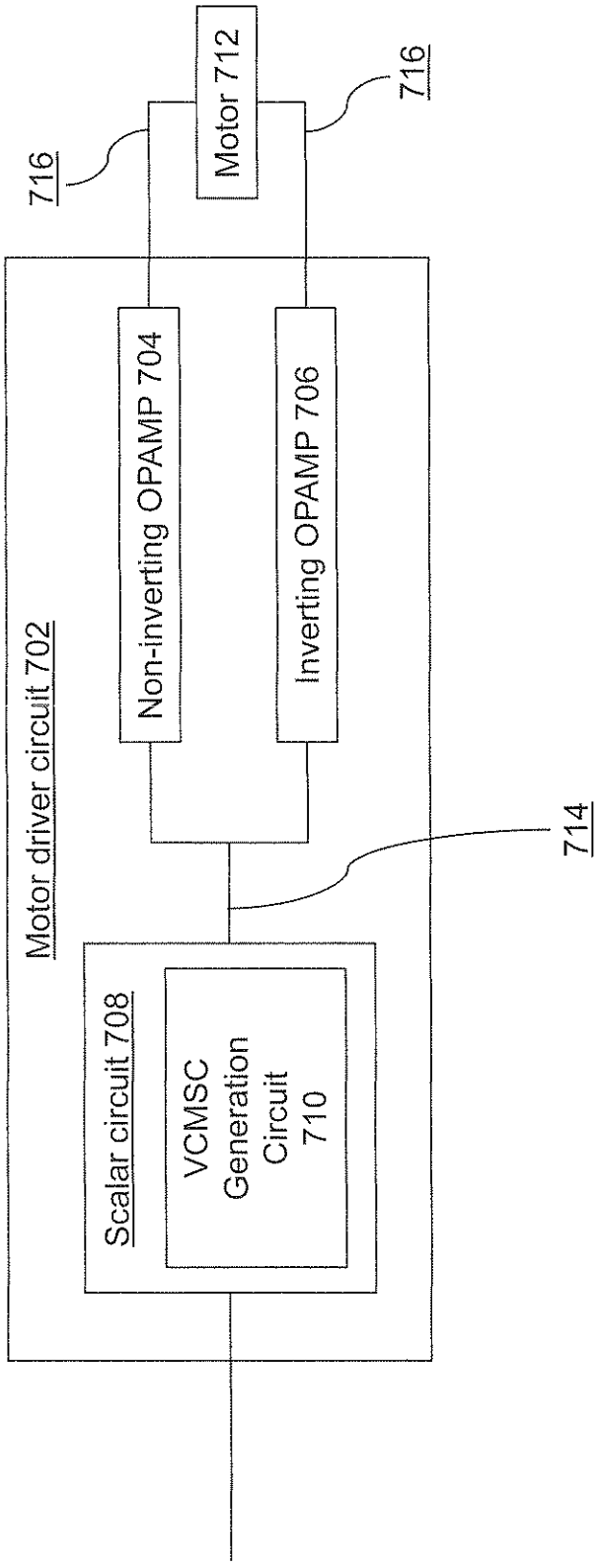

Motor driver circuit 702
Scalar circuit 708
VCMSC Generation Circuit 710
Non-inverting OPAMP 704
Inverting OPAMP 706
Motor 712
716
716
714

FIG. 7
700

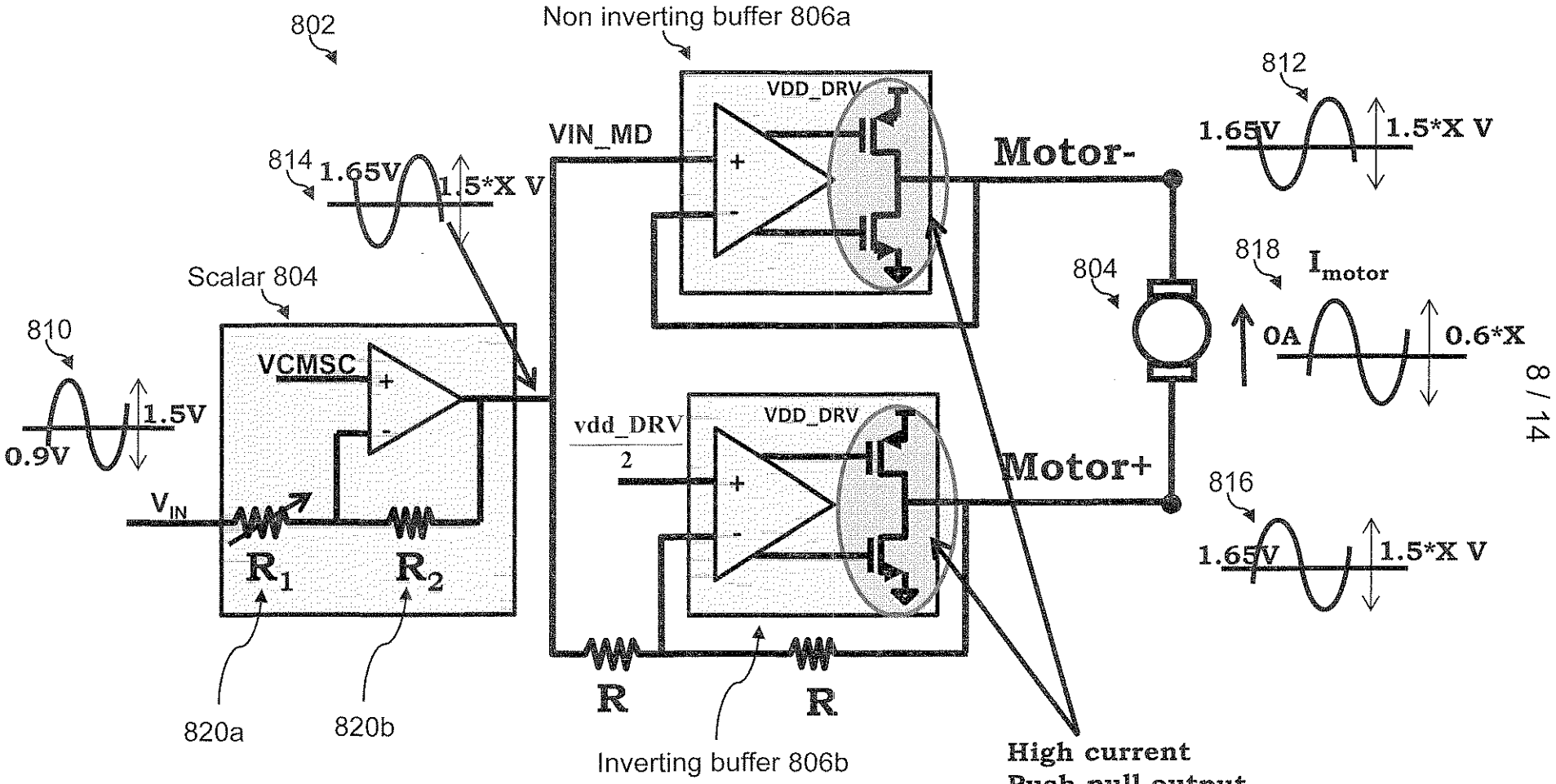

802
Non inverting buffer 806a
VDD_DRV
VIN_MD
814
1.65V
1.5*X V
Motor-
812
1.65V
1.5*X V
Scalar 804
804
818
I_{motor}
0A
0.6*X
810
VCMSC
1.5V
0.9V
vdd_DRV
2
VDD_DRV
Motor+
816
1.65V
1.5*X V
V_{IN}
R_1
R_2
R
R
820a
820b
Inverting buffer 806b
High current
Push-pull output
stage

FIG. 8
800

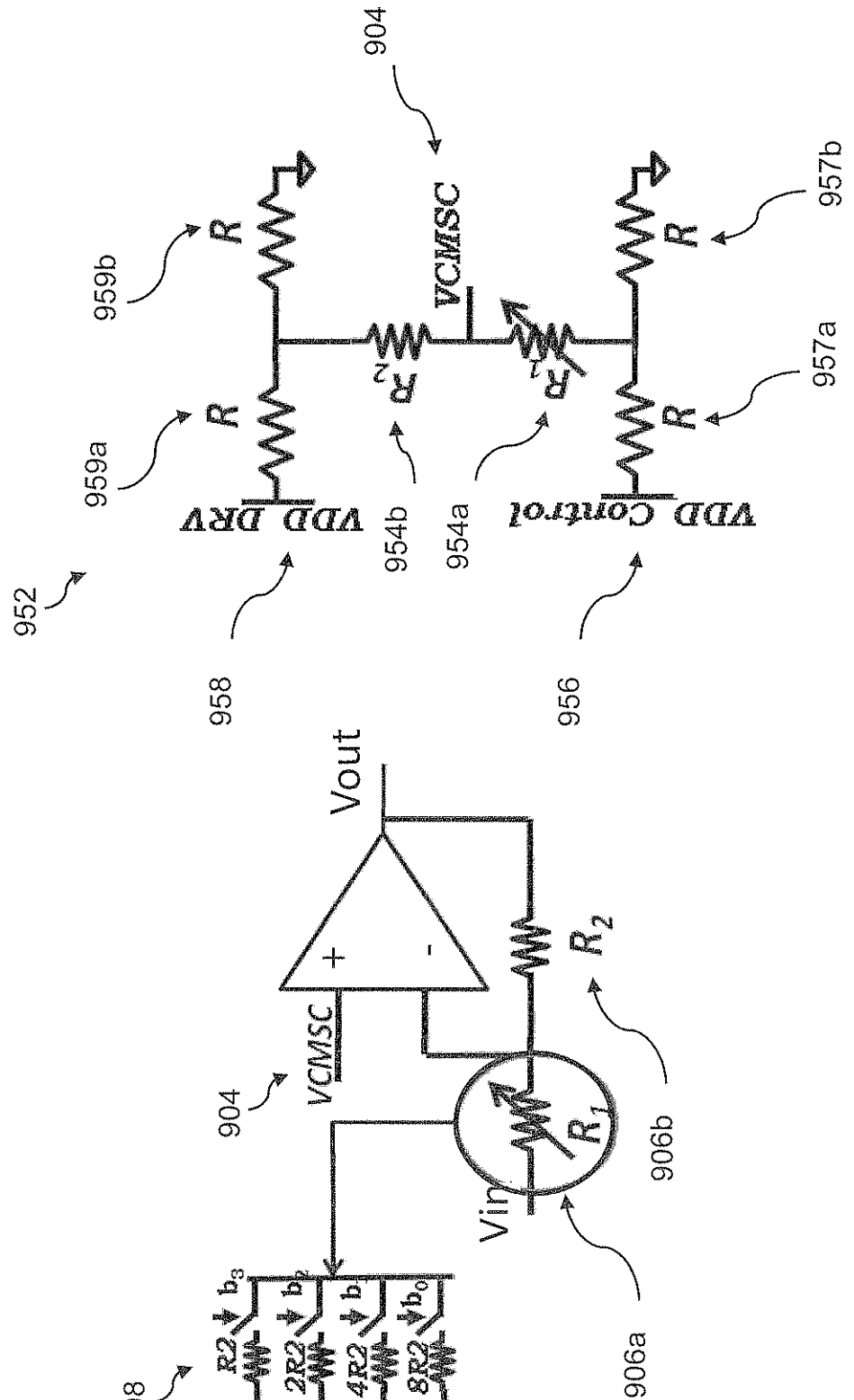


FIG. 9A
900

FIG. 9B
950

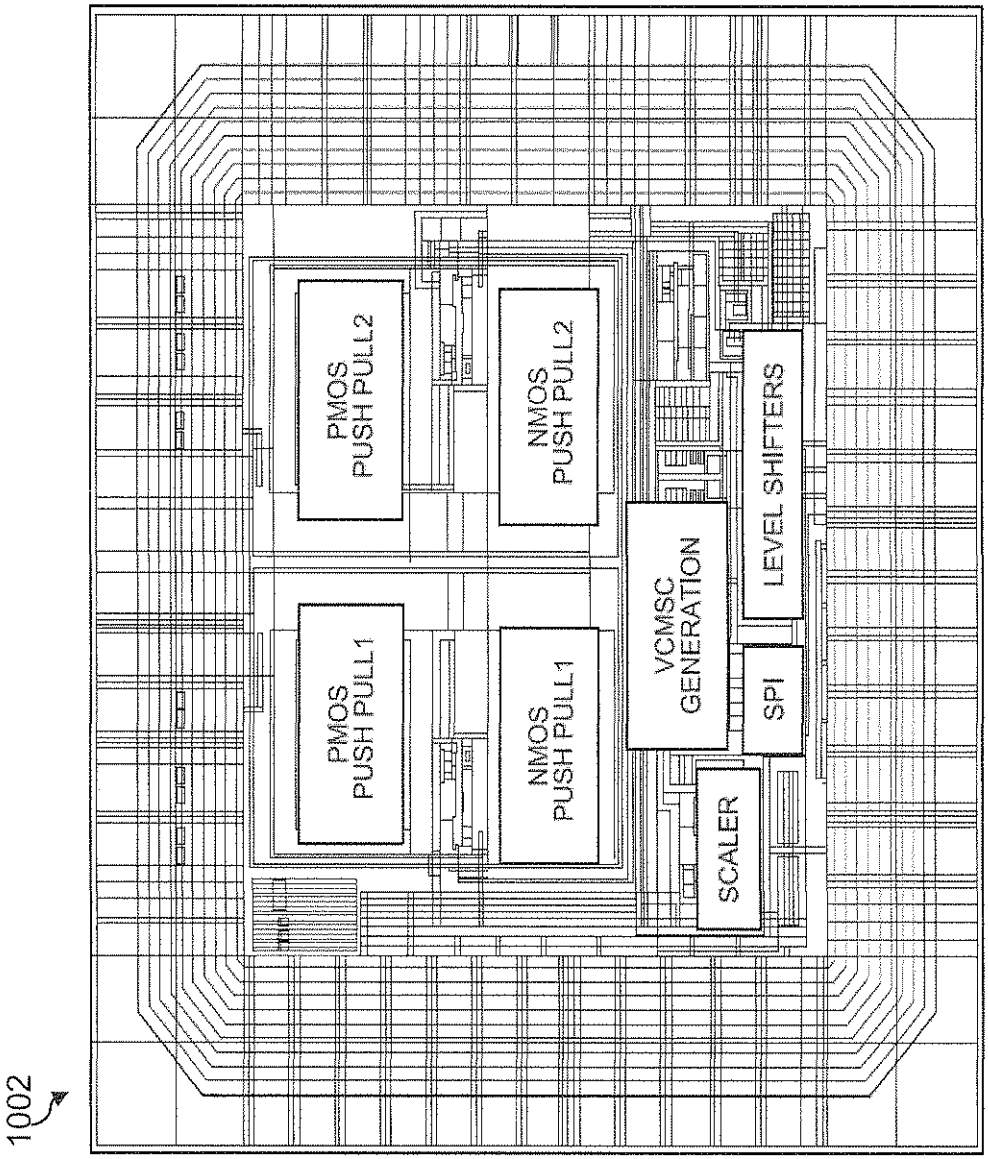

1002
PMOS PUSH PULL2
NMOS PUSH PULL2
PMOS PUSH PULL1
NMOS PUSH PULL1
VCMSC GENERATION
LEVEL SHIFTERS
SPI
SCALER

FIG. 10
1000

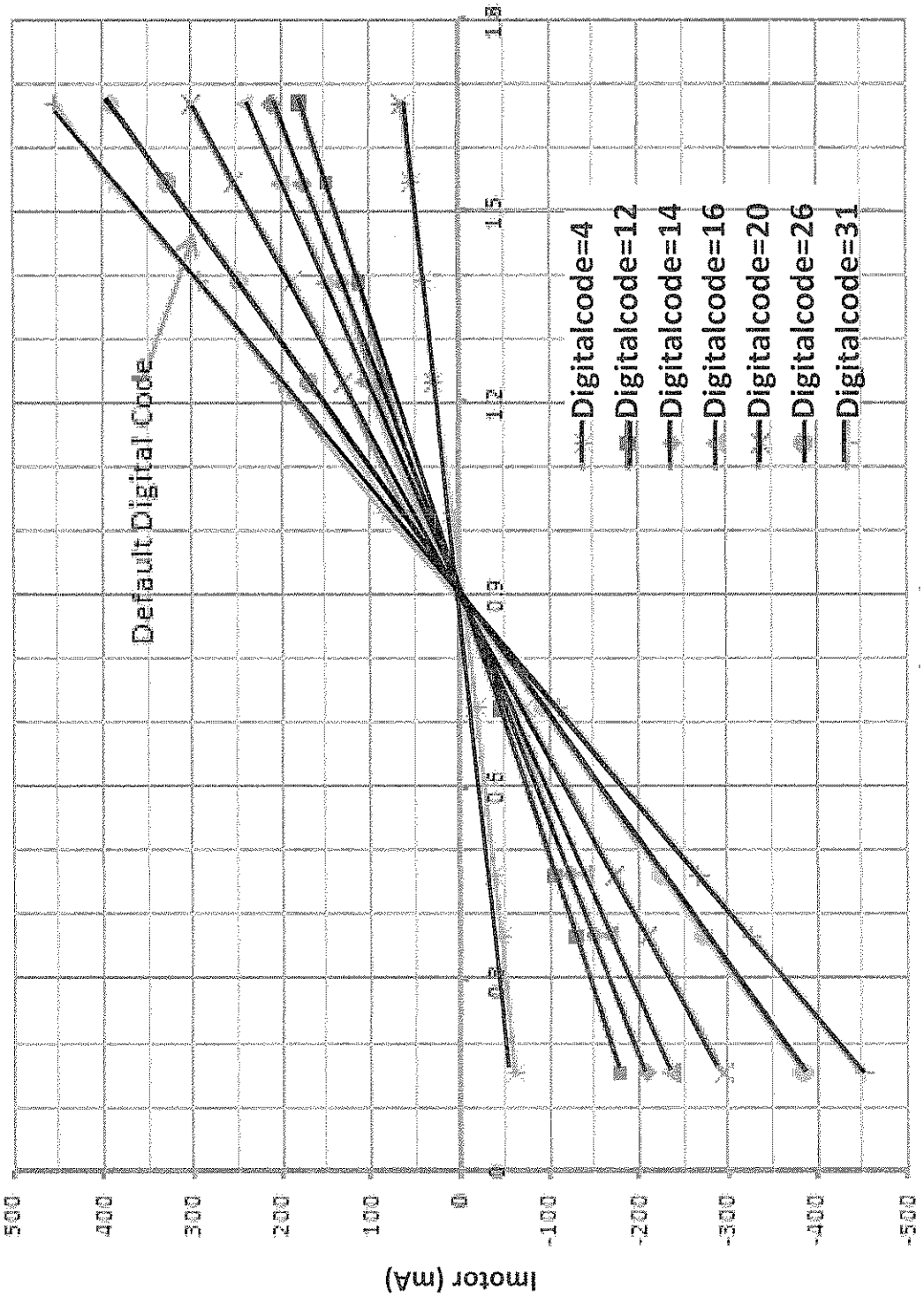

Imotor (mA)
500
400
300
200
100
0
-100
-200
-300
-400
-500
0
0.3
0.6
0.9
1.2
1.5
1.8
Vin_Drive (V)
Default Digital Code
Digitalcode=4
Digitalcode=12
Digitalcode=14
Digitalcode=16
Digitalcode=20
Digitalcode=26
Digitalcode=31

FIG. 11
1100

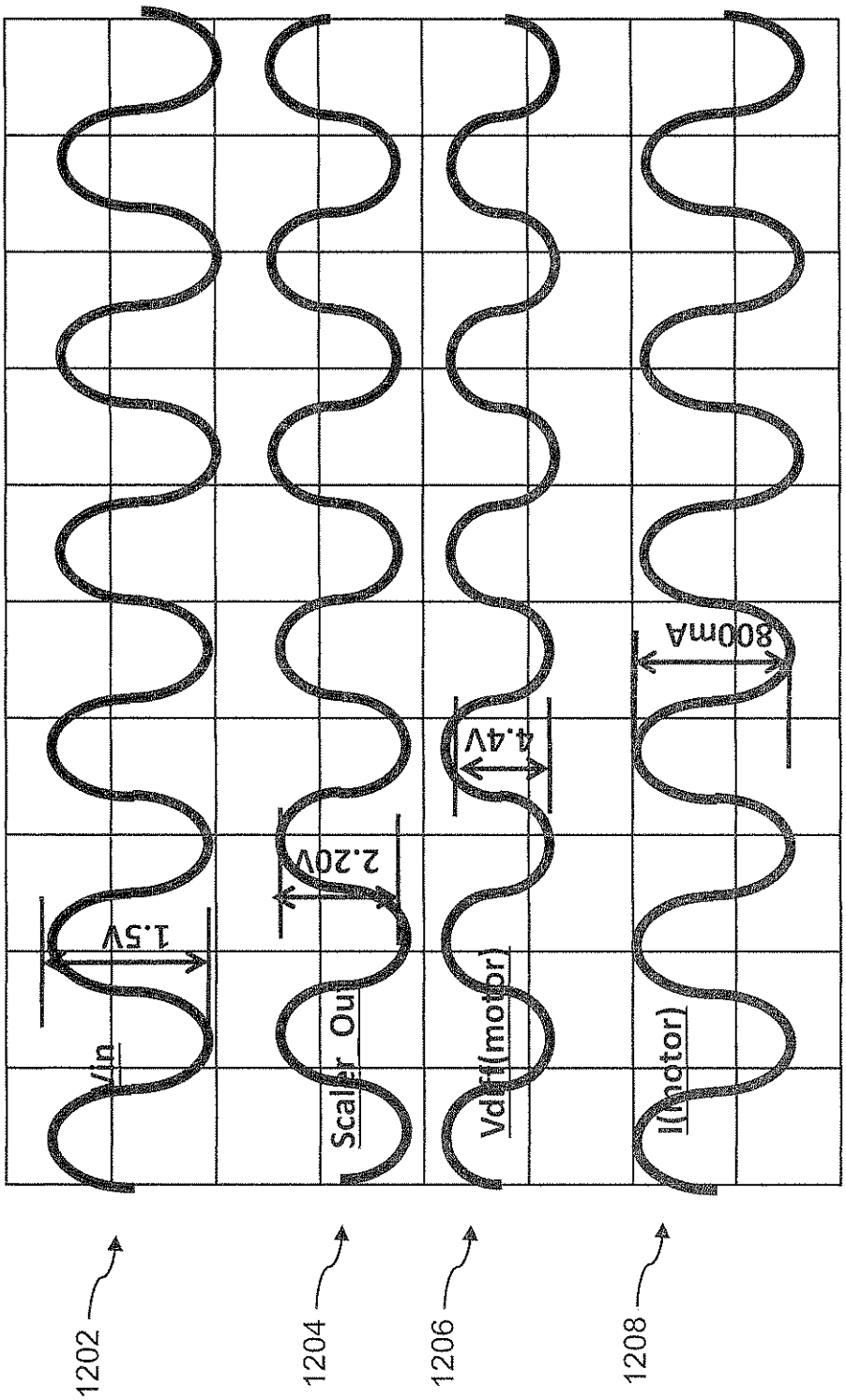

1202
1204
1206
1208
Vin
1.5V
Scaler Ou
2.20V
Vdrf(motor)
4.4V
I(motor)
800mA

FIG. 12
1200

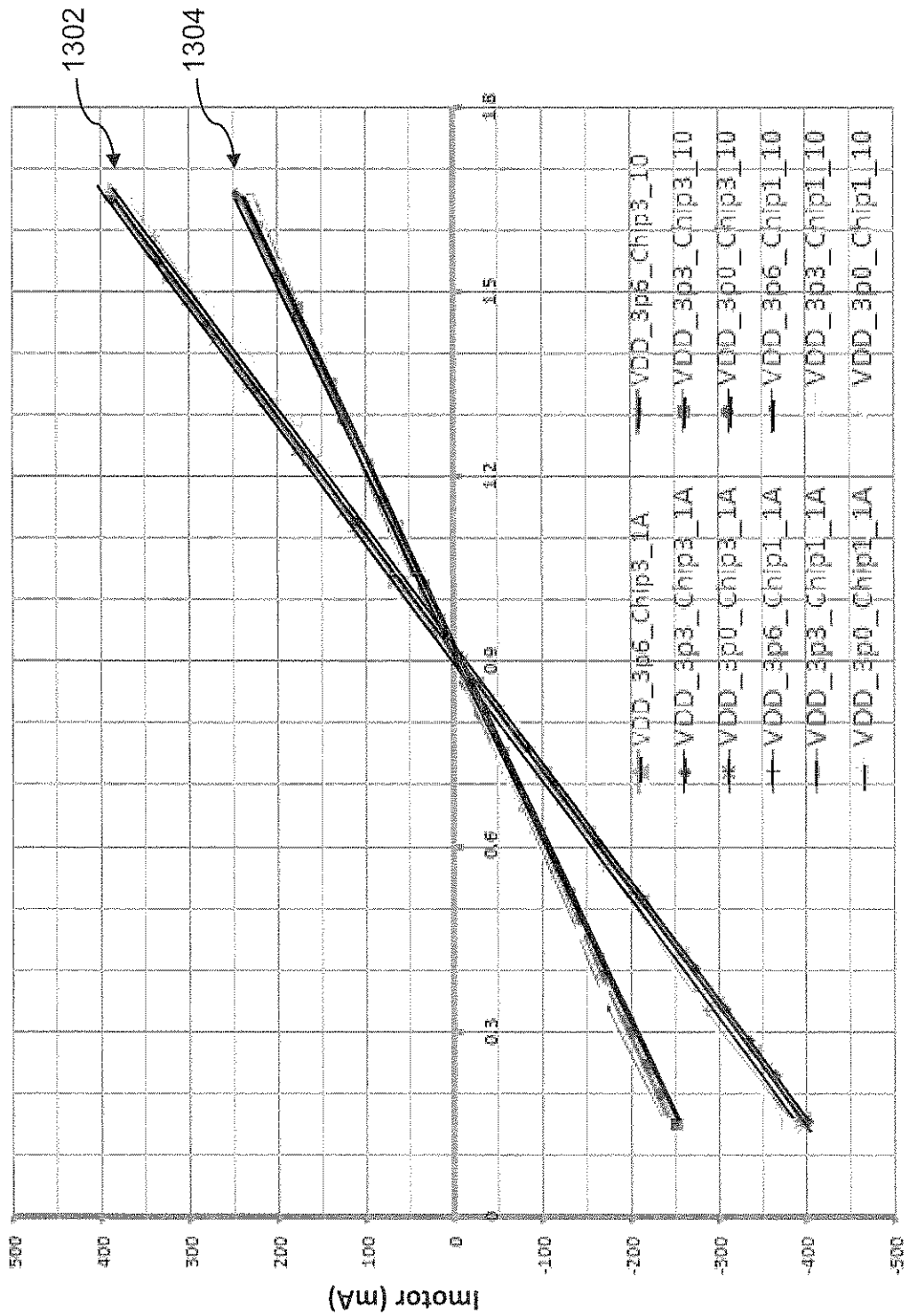

1302
1304
Imotor (mA)
Vin_Drive (V)
VDD_3p6_Chip3_1A
VDD_3p3_Chip3_1A
VDD_3p0_Chip3_1A
VDD_3p6_Chip1_1A
VDD_3p3_Chip1_1A
VDD_3p0_Chip1_1A
VDD_3p6_Chip3_10
VDD_3p3_Chip3_10
VDD_3p0_Chip3_10
VDD_3p6_Chip1_10
VDD_3p3_Chip1_10
VDD_3p0_Chip1_10

FIG. 13
1300

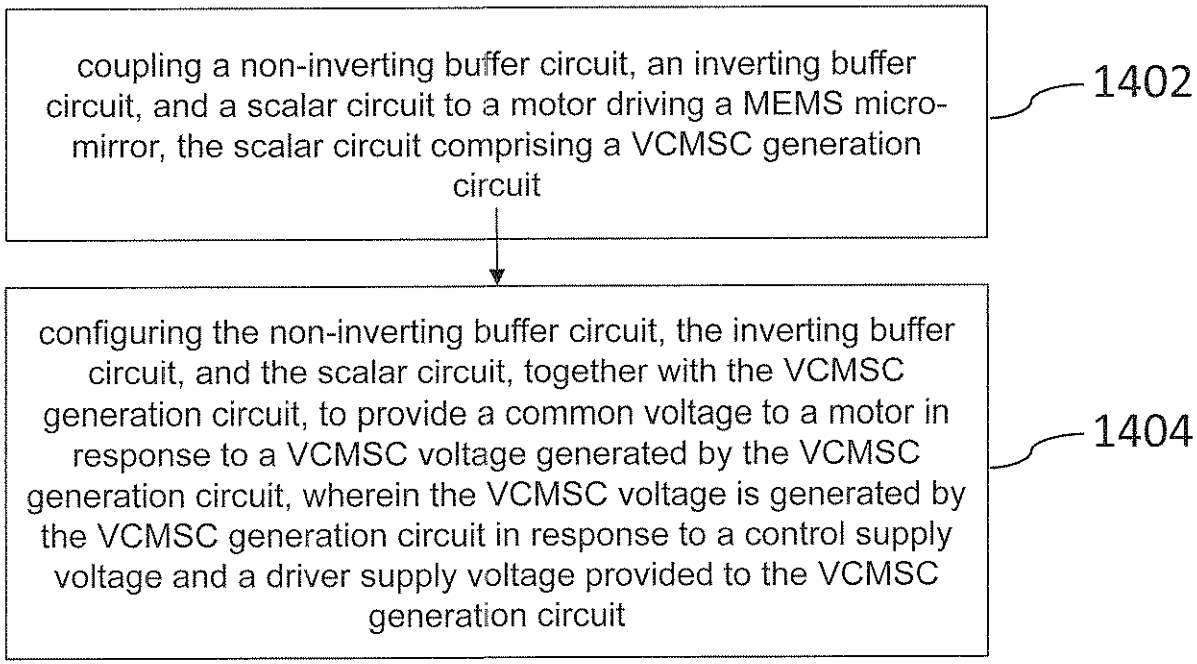

coupling a non-inverting buffer circuit, an inverting buffer circuit, and a scalar circuit to a motor driving a MEMS micro-mirror, the scalar circuit comprising a VCMSC generation circuit
1402
configuring the non-inverting buffer circuit, the inverting buffer circuit, and the scalar circuit, together with the VCMSC generation circuit, to provide a common voltage to a motor in response to a VCMSC voltage generated by the VCMSC generation circuit, wherein the VCMSC voltage is generated by the VCMSC generation circuit in response to a control supply voltage and a driver supply voltage provided to the VCMSC generation circuit
1404

FIG. 14
1400