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FIG. 1

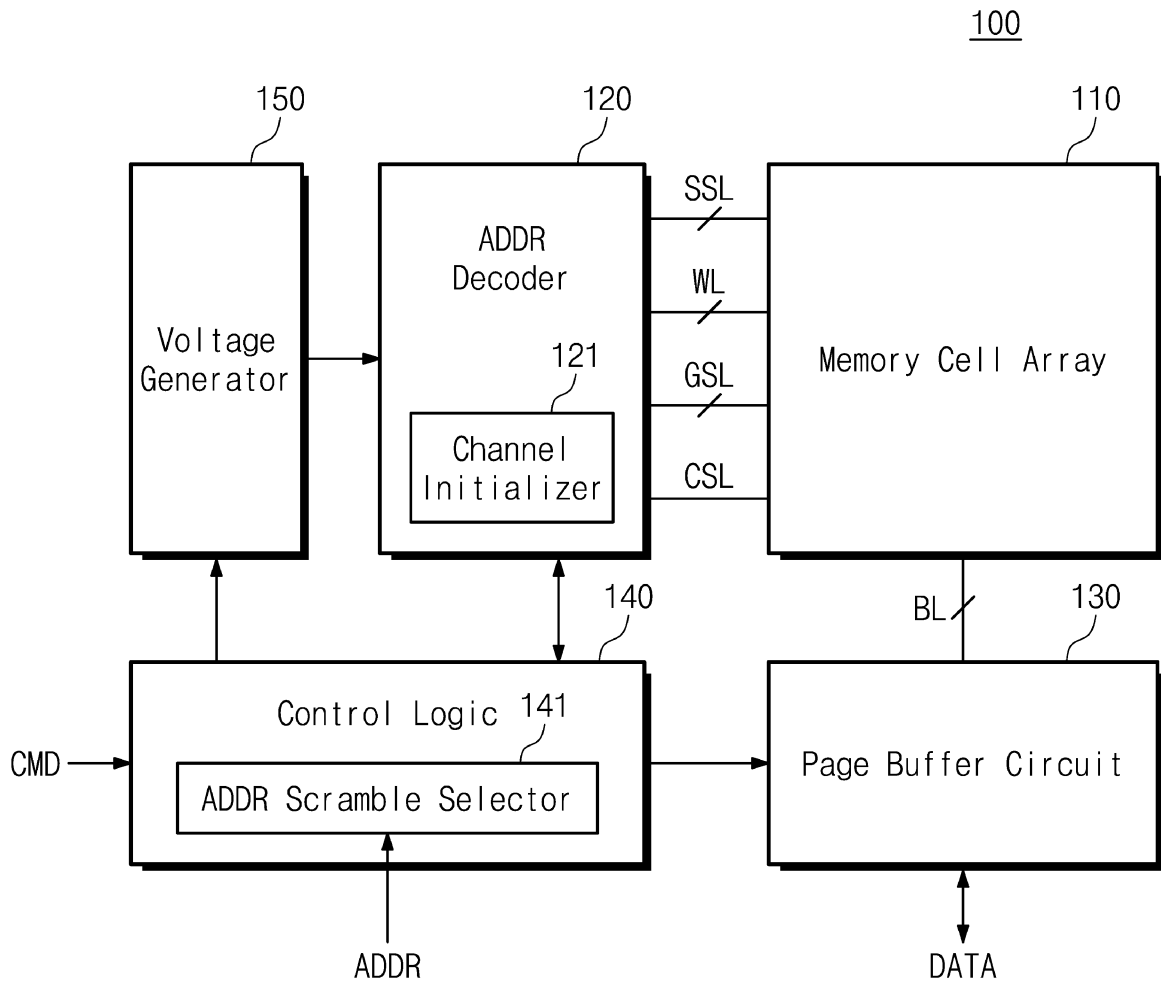
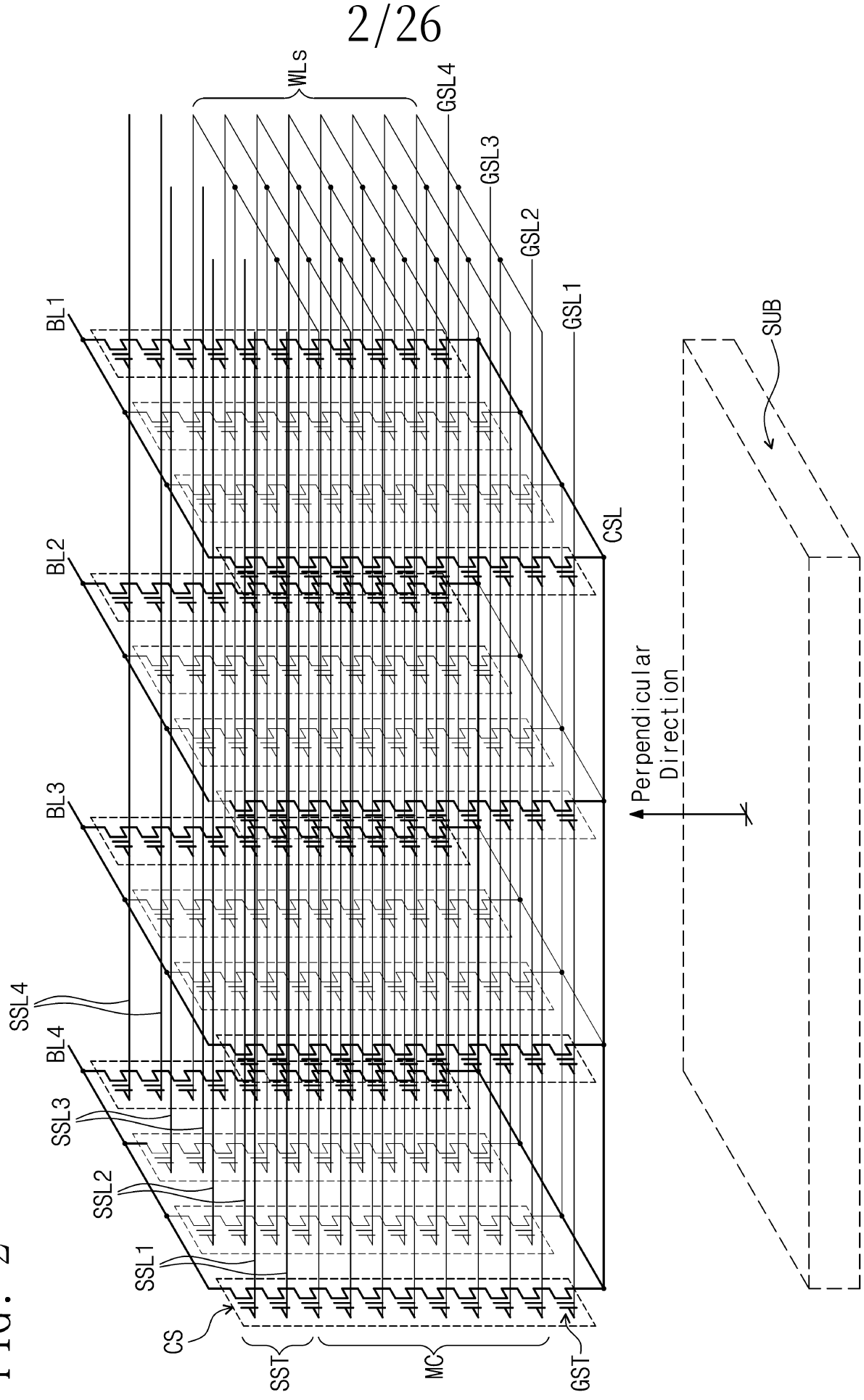
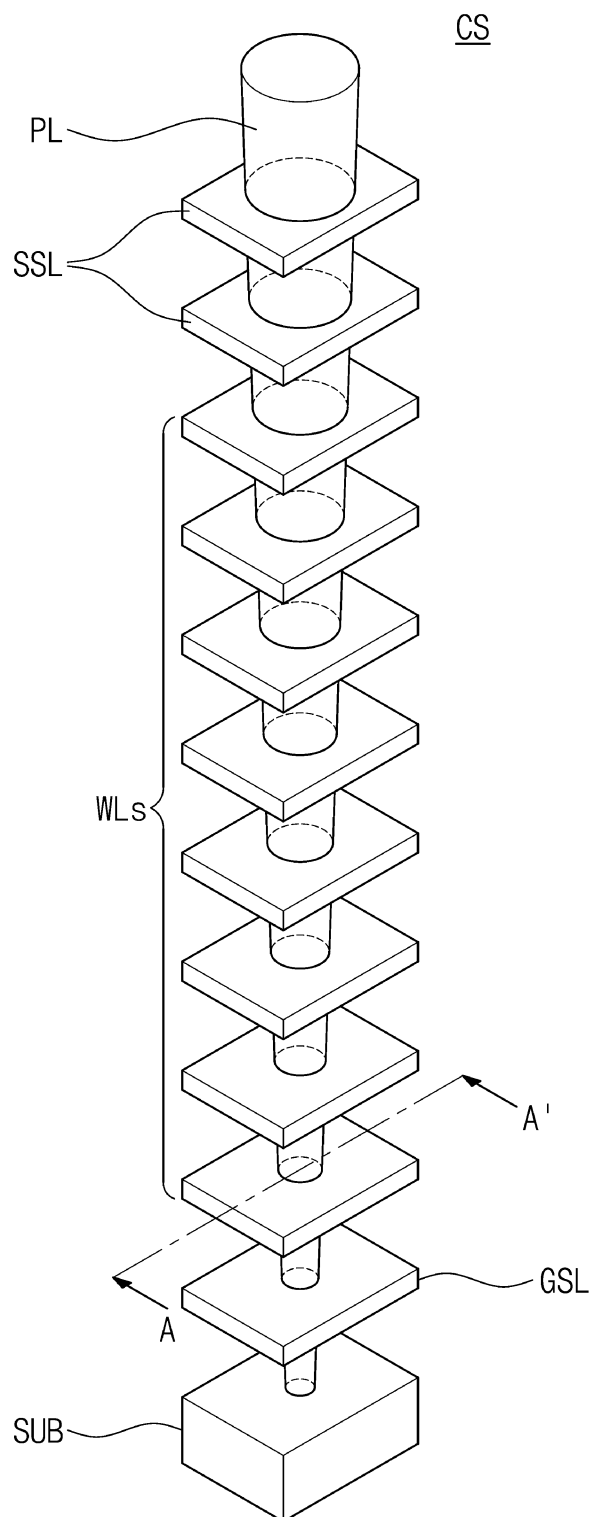


FIG. 2

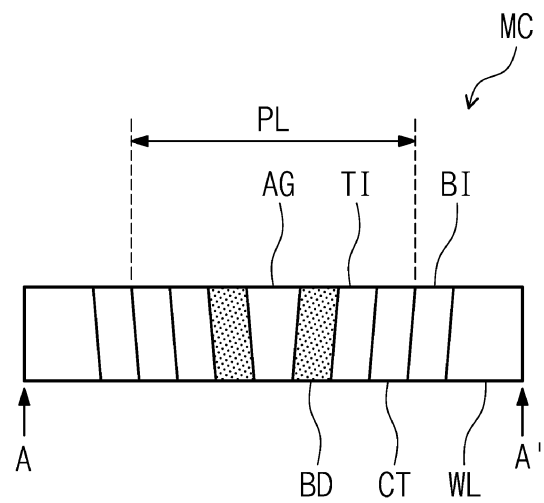
BLKa



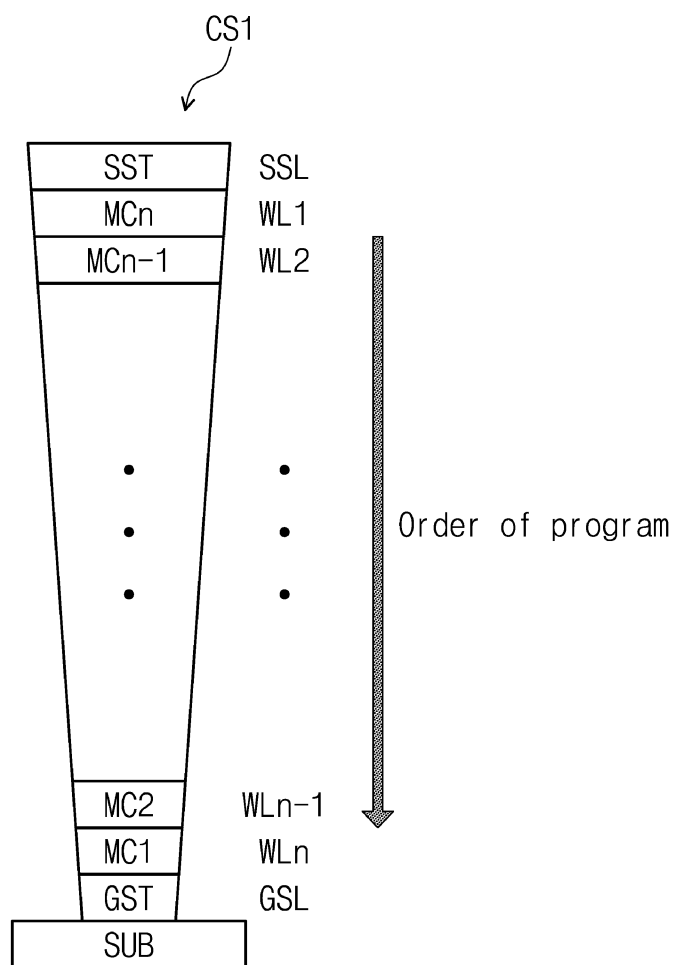
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FIG. 3A



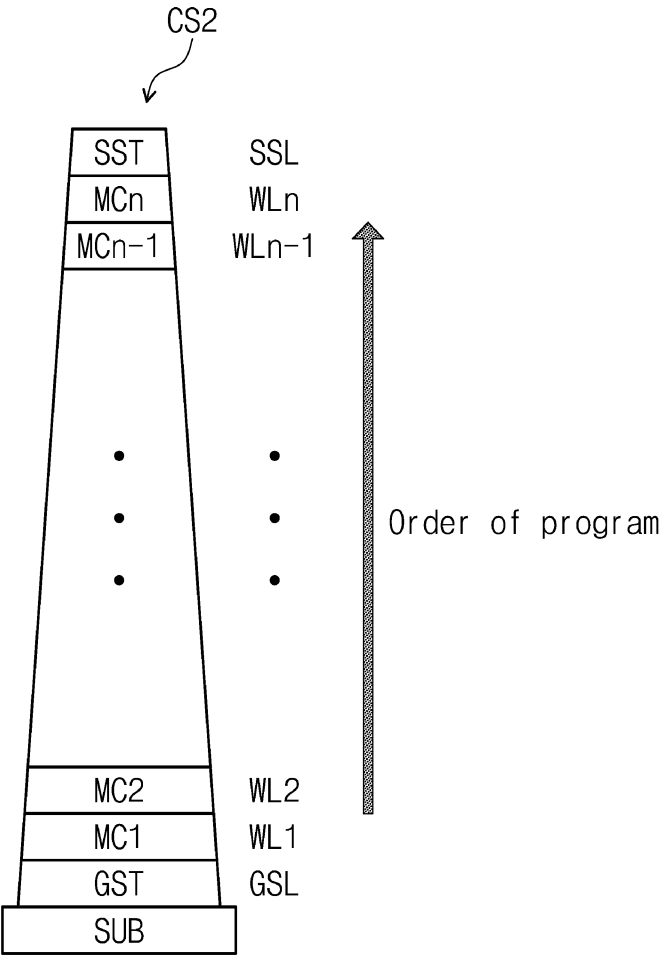
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FIG. 3B



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FIG. 4A

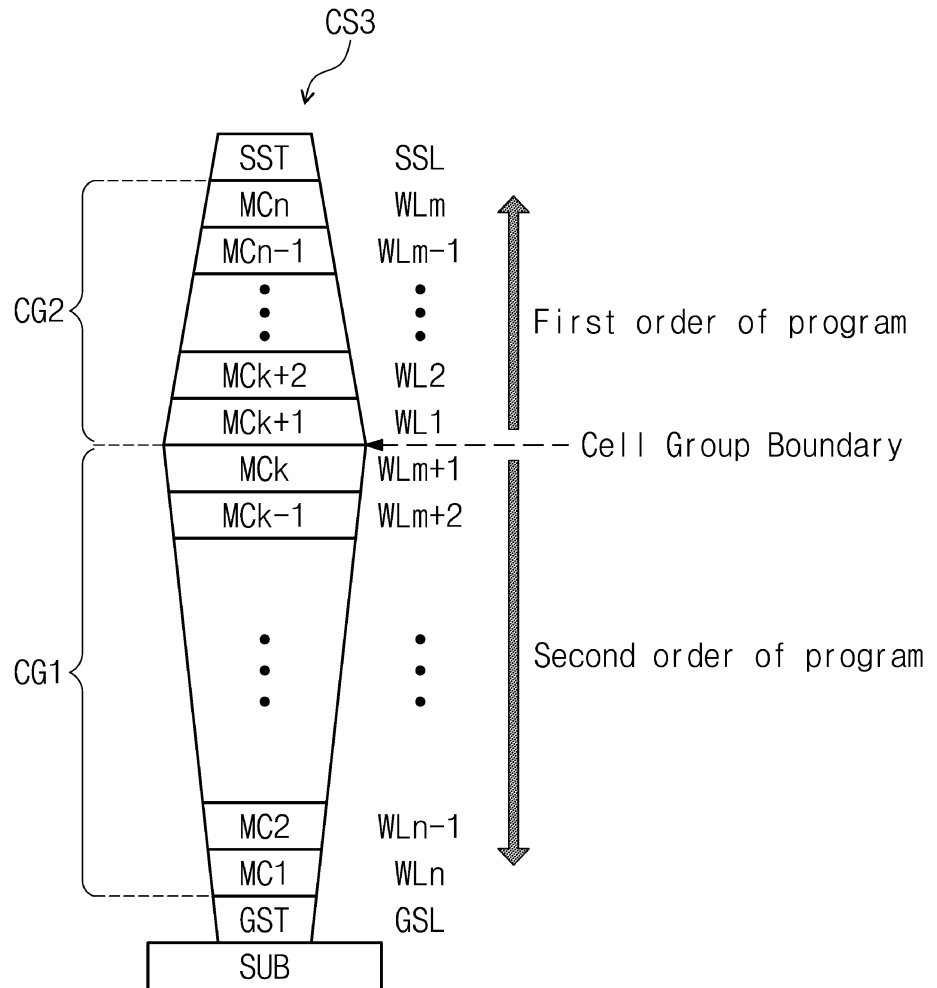


< ADDR Scramble 1 >



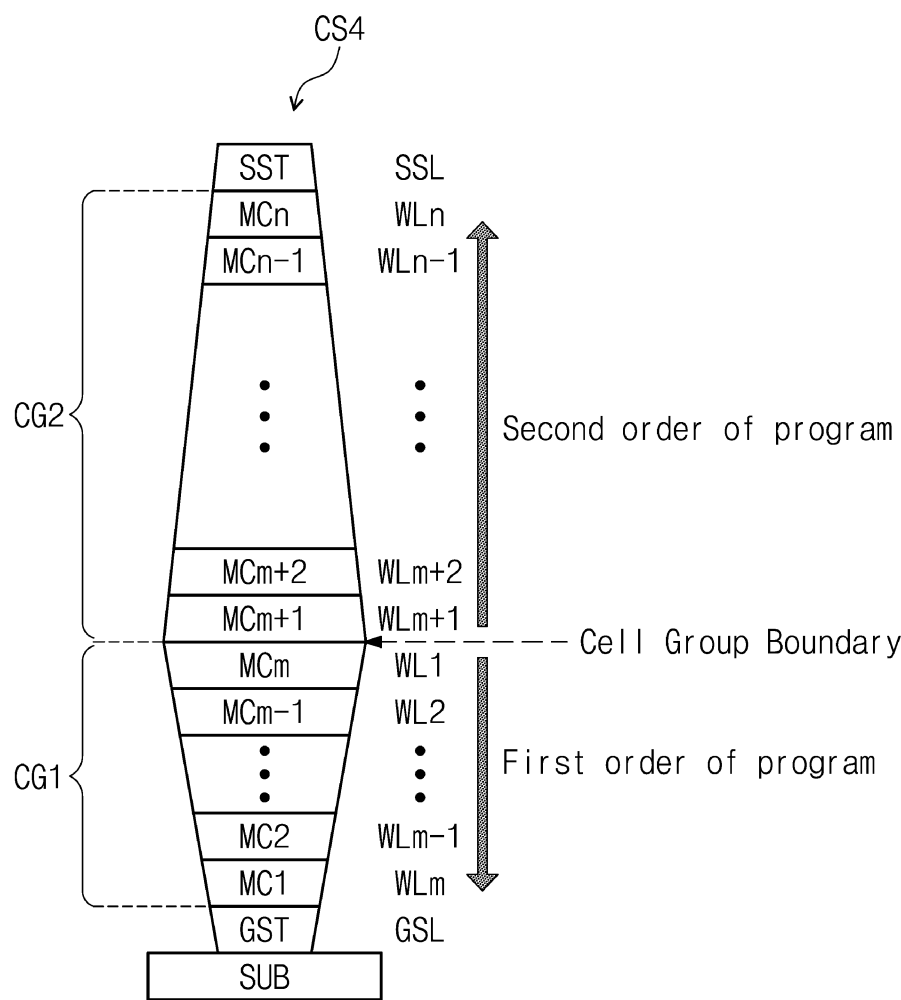
< ADDR Scramble 2 >

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FIG. 4C



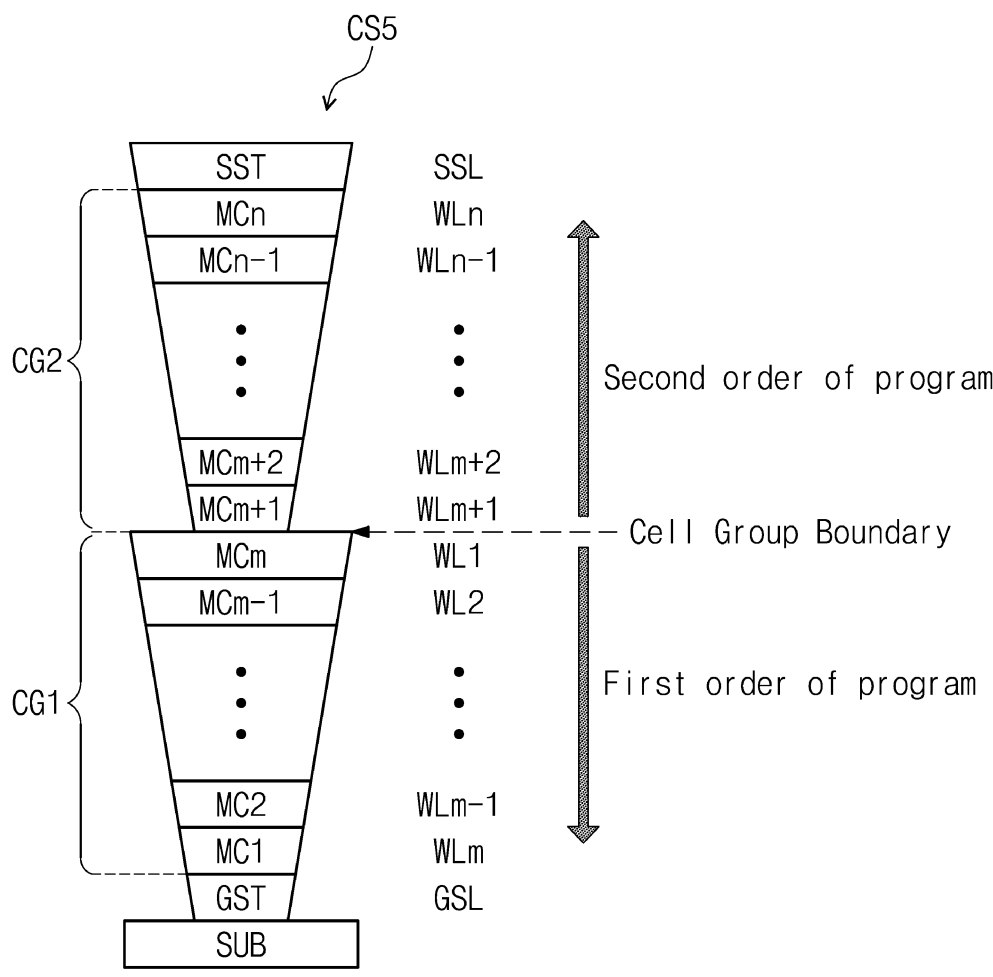
< ADDR Scramble 3 >

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FIG. 4D



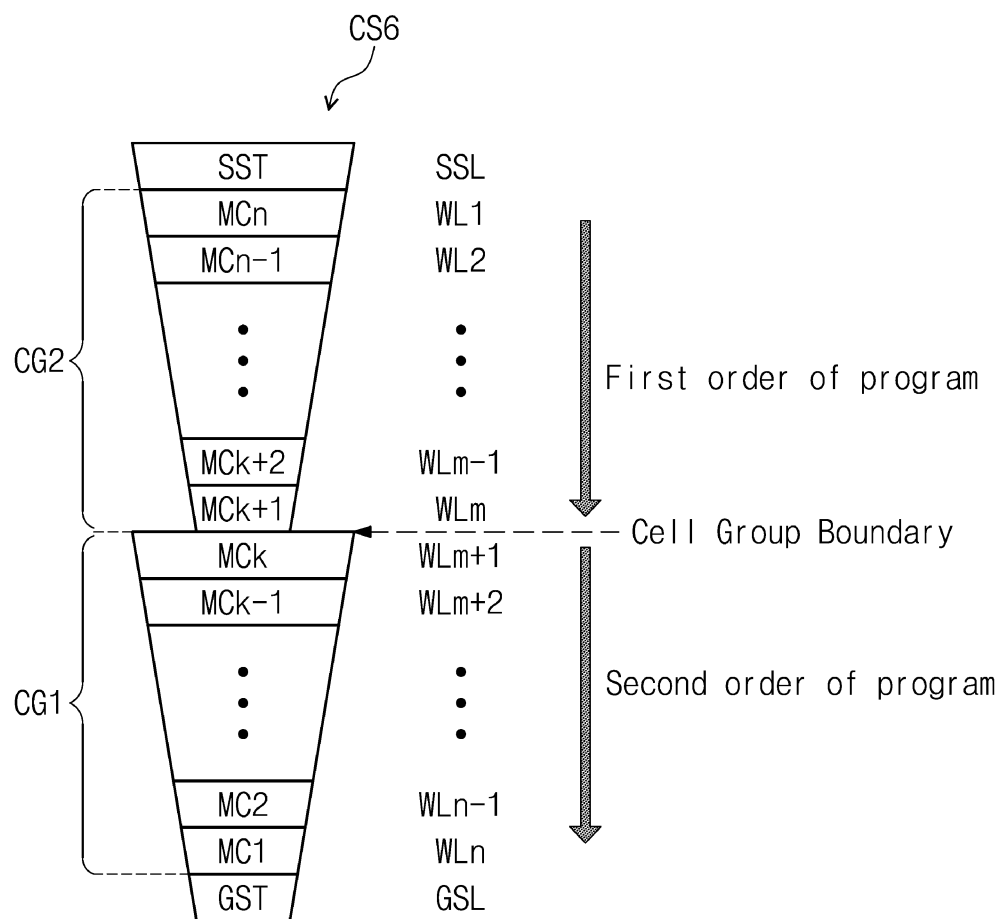
< ADDR Scramble 4 >

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FIG. 4E



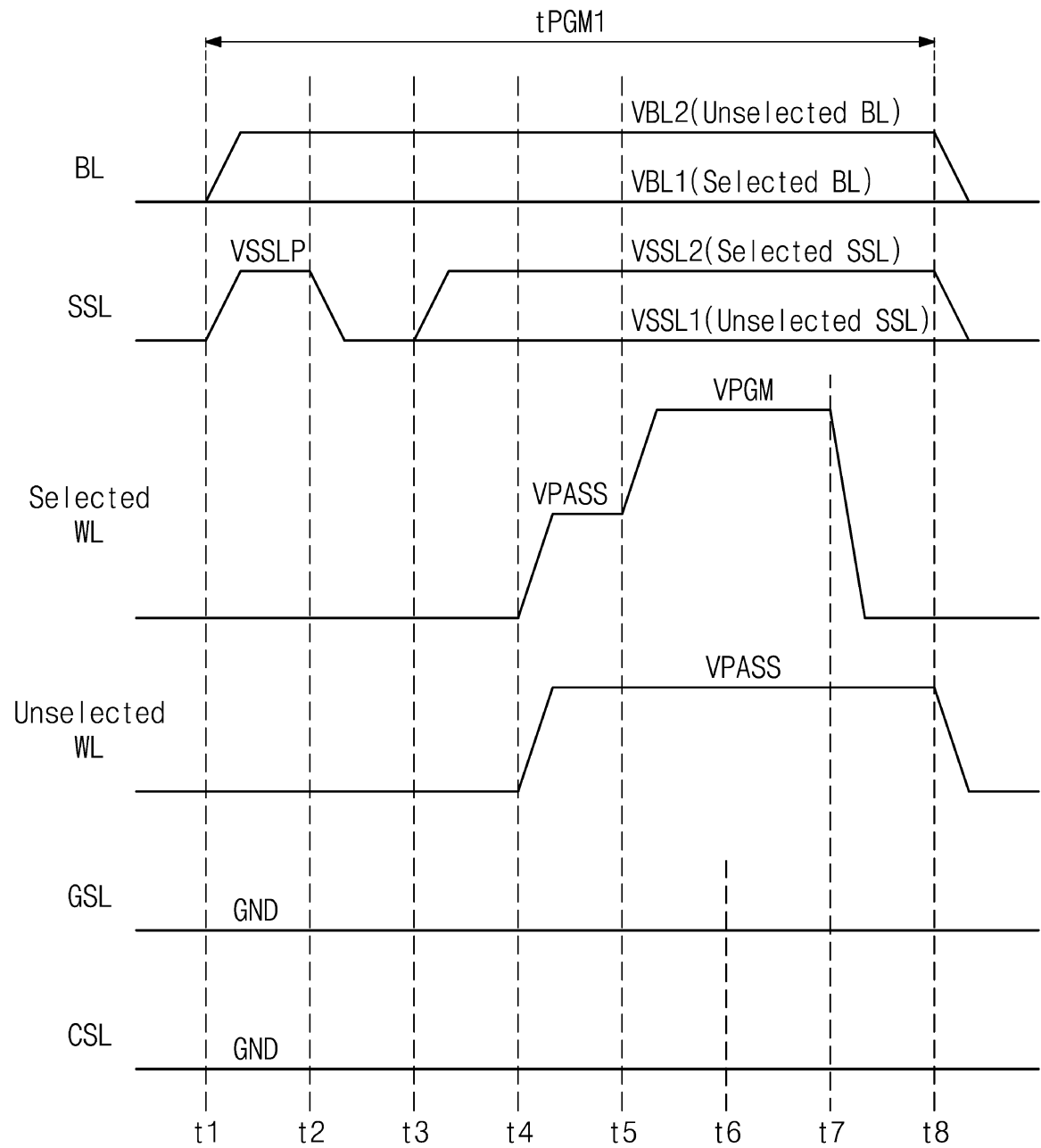
< ADDR Scramble 5 >

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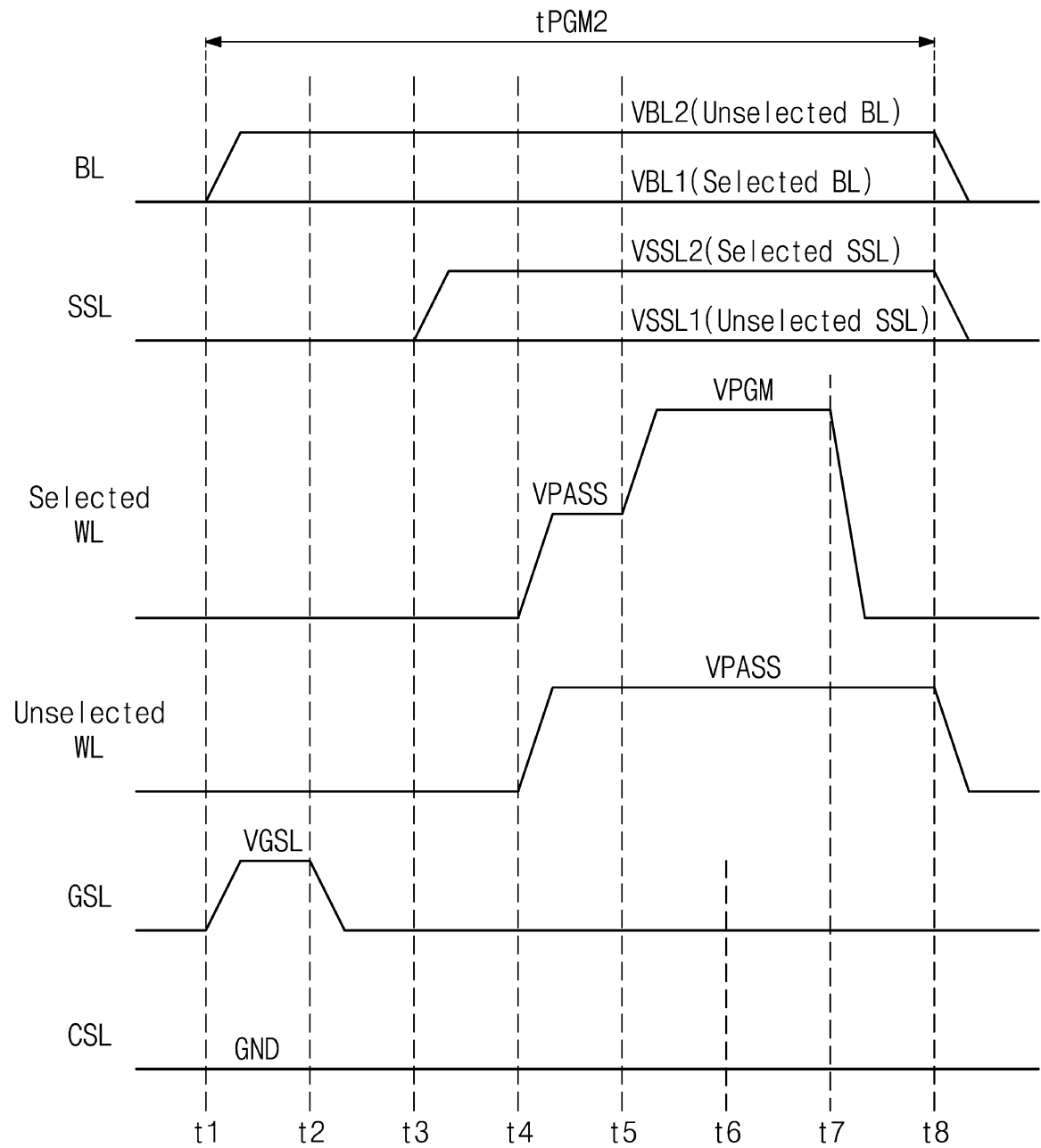
< ADDR Scramble 6 >

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FIG. 5



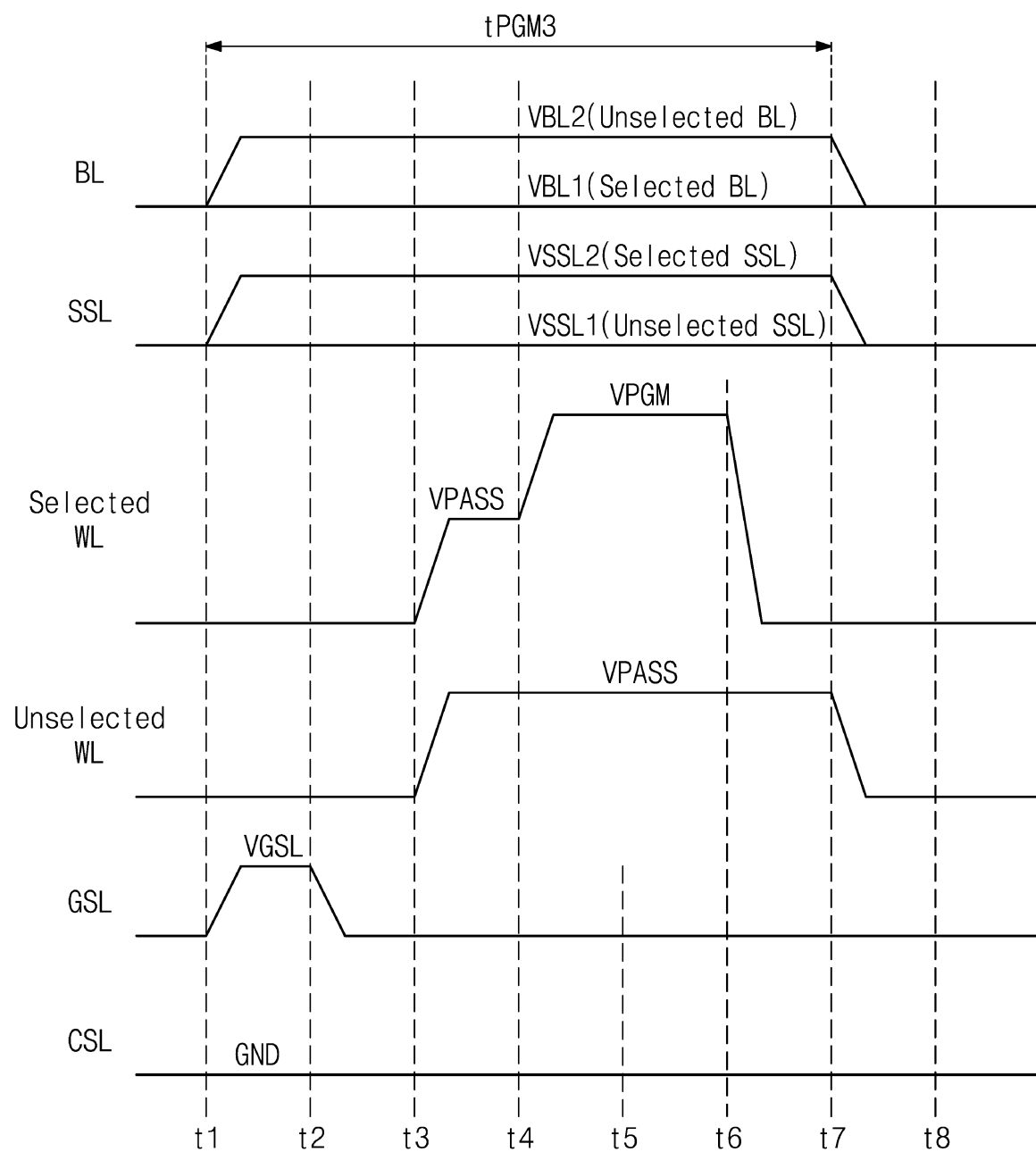
< Program Operation 1 >

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FIG. 6



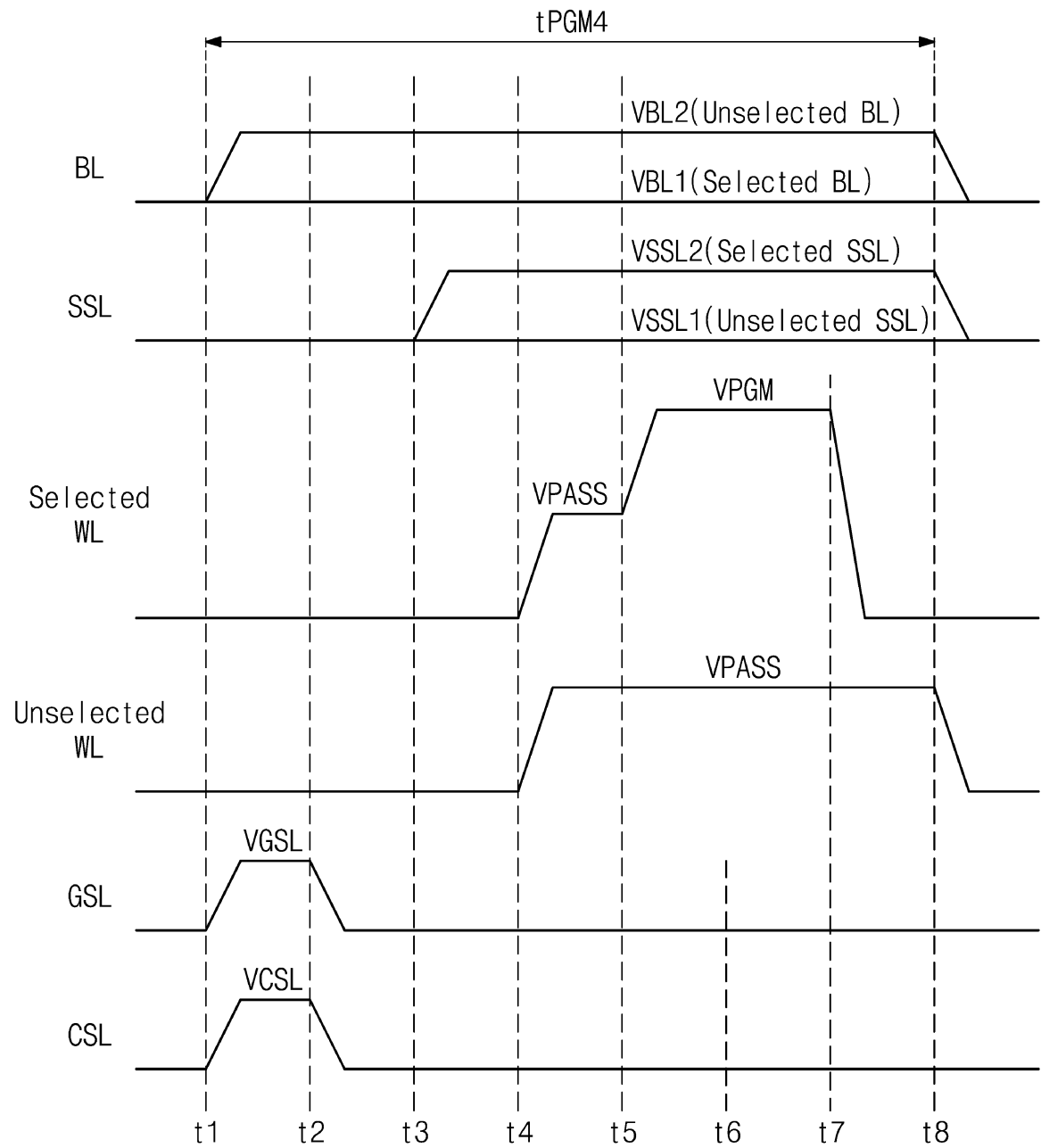
< Program Operation 2 >

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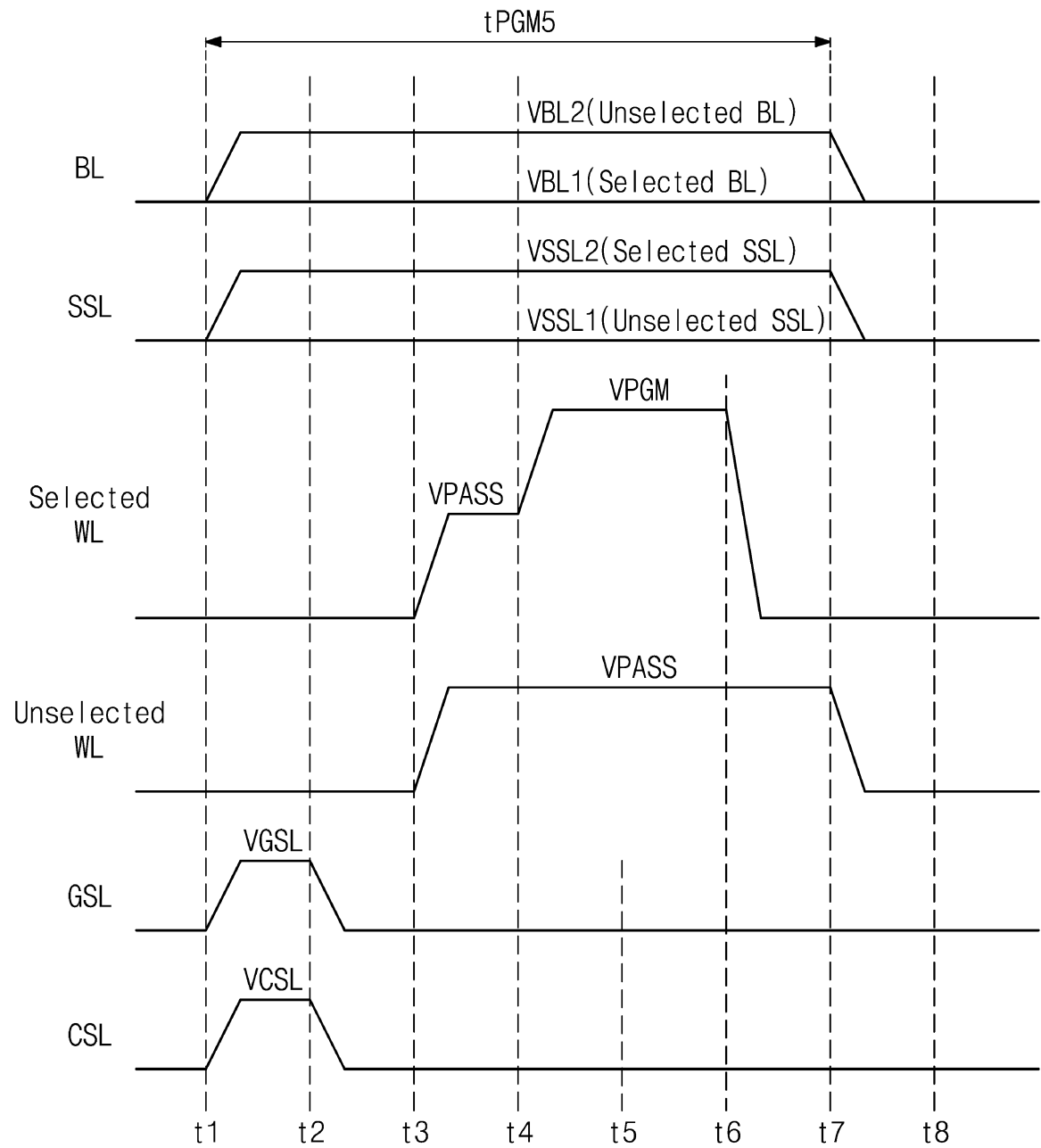
< Program Operation 3 >

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FIG. 8



< Program Operation 4 >

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< Program Operation 5 >

FIG. 10

Order of Program	ADDR Scramble 1	ADDR Scramble 2	ADDR Scramble 3	ADDR Scramble 4	ADDR Scramble 5	ADDR Scramble 6
WL1	Program 2 Operation 2	Program 1 Operation 1	Program 1 Operation 1	Program 2 Operation 2	Program 2 Operation 2	Program 2 Operation 2
WL2						
WL3						
• • •						
WLm-1						
WLm						
WLm+1						
• • •						
WLn-2			Program 1 Operation 1			
WLn-1						
WLn						

FIG. 11

Order of Program	ADDR Scramble 1	ADDR Scramble 2	ADDR Scramble 3	ADDR Scramble 4	ADDR Scramble 5	ADDR Scramble 6
WL1	Program Operation 2	Program Operation 1	Program Operation 1	Program Operation 2	Program Operation 2	Program Operation 2
WL2						
WL3						
•						
•						
•						
WLG-1						
WLG	Program Operation 3	Program Operation 1	Program Operation 2	Program Operation 3	Program Operation 3	
WLG+1						
•						
•						
•						
WLM-1						
WLM						
WLM+1	Program Operation 3	Program Operation 1	Program Operation 2	Program Operation 1	Program Operation 1	
•						
•						
•						
WLh-1						
WLh						
WLh+1						
•						
•						
•						
WLn-2						
WLn-1						
WLn						

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FIG. 12

Order of Program	ADDR Scramble 3	ADDR Scramble 4	ADDR Scramble 5
WL1	Bit Reduction Program Operation		
WL2	Program Operation 1	Program Operation 2	Program Operation 2
WL3			
⋮			
WLm-1			
WLm			
WLm+1	Program Operation 2	Program Operation 1	Program Operation 1
⋮			
WLn-2			
WLn-1			
WLn			

FIG. 13

Program Loop	ADDR Scramble 1	ADDR Scramble 3		ADDR Scramble 4		ADDR Scramble 6
L00P1	WL1~WLn	WL1~WLn	WLm+1~WLn	WL1~WLn	WLm+1~WLn	WL1~WLn
L00P2	Program Operation 2	Program Operation 1	Program Operation 2	Program Operation 2	Program Operation 1	Program Operation 2
L00P3						
• • •						
L00Pm-1	Program Operation 4	Program Operation 1	Program Operation 2	Program Operation 2	Program Operation 1	Program Operation 2
L00Pm						
L00Pm+1						
• • •	Program Operation 4	Program Operation 1	Program Operation 2	Program Operation 2	Program Operation 1	Program Operation 2
L00Pn-2						
L00Pn-1						
L00Pn						

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FIG. 15

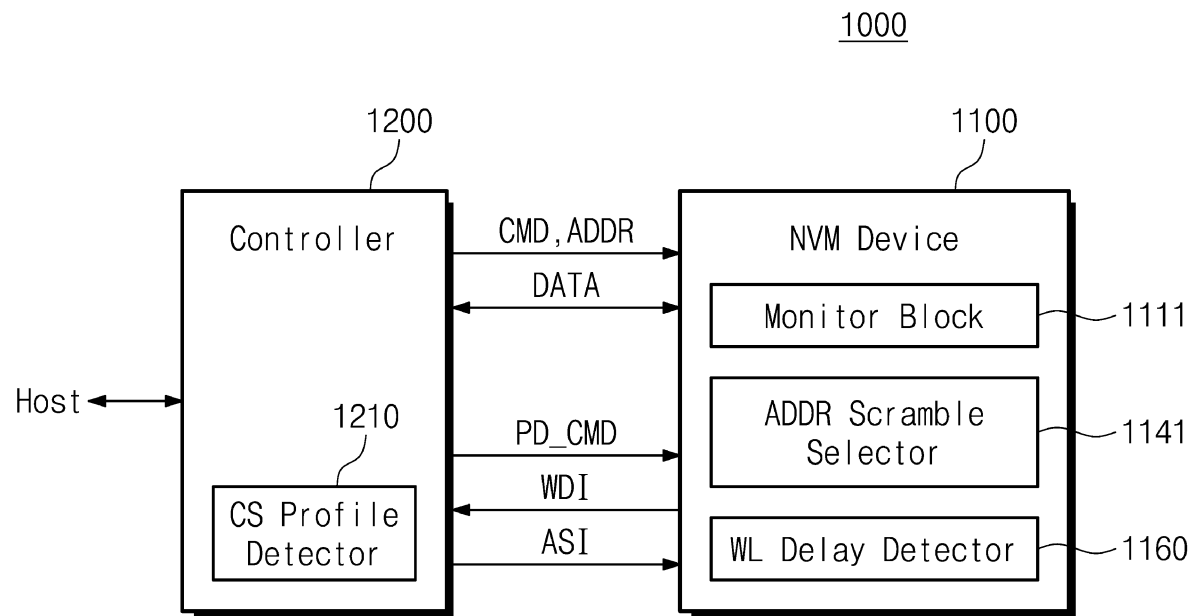
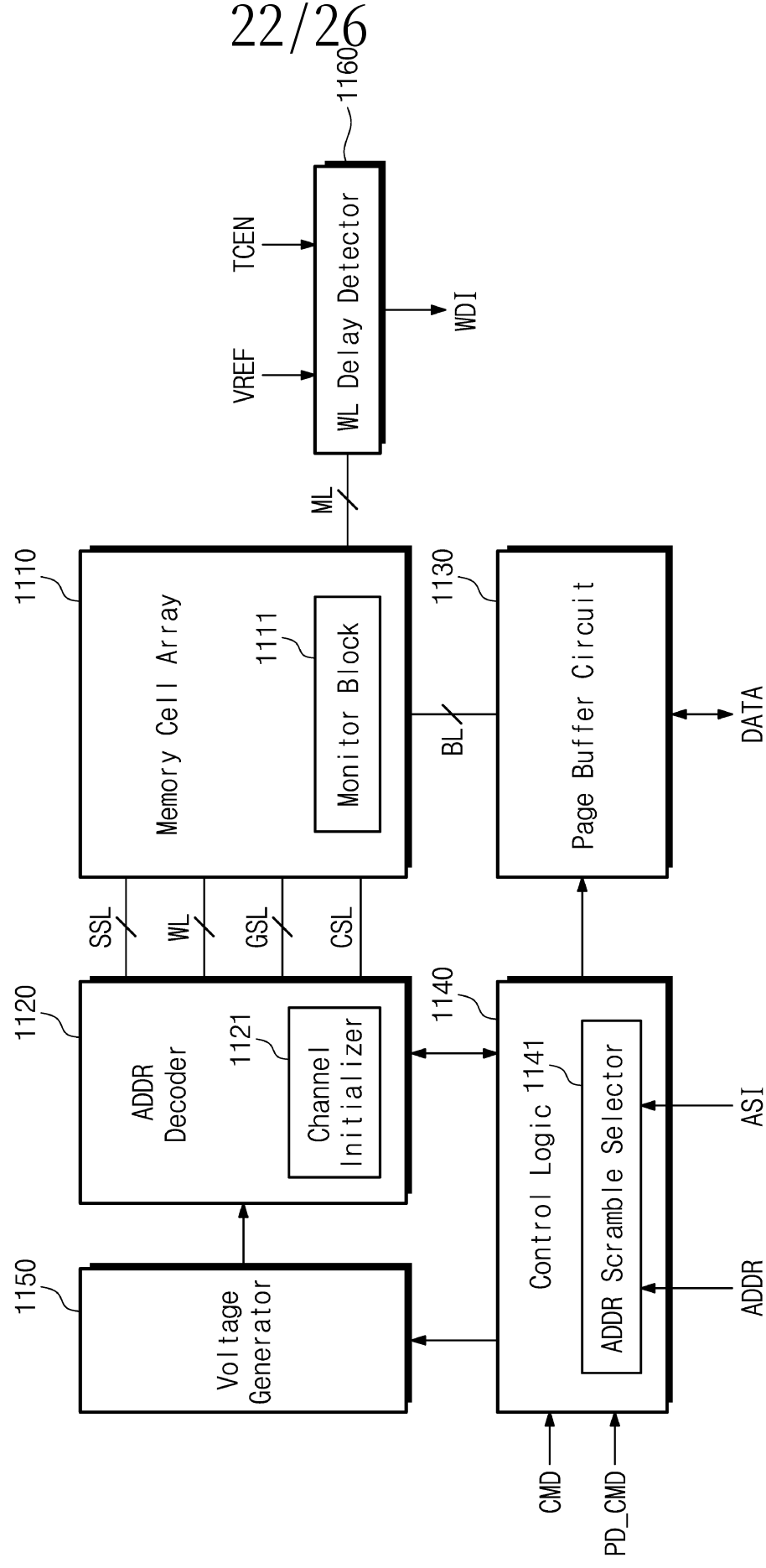
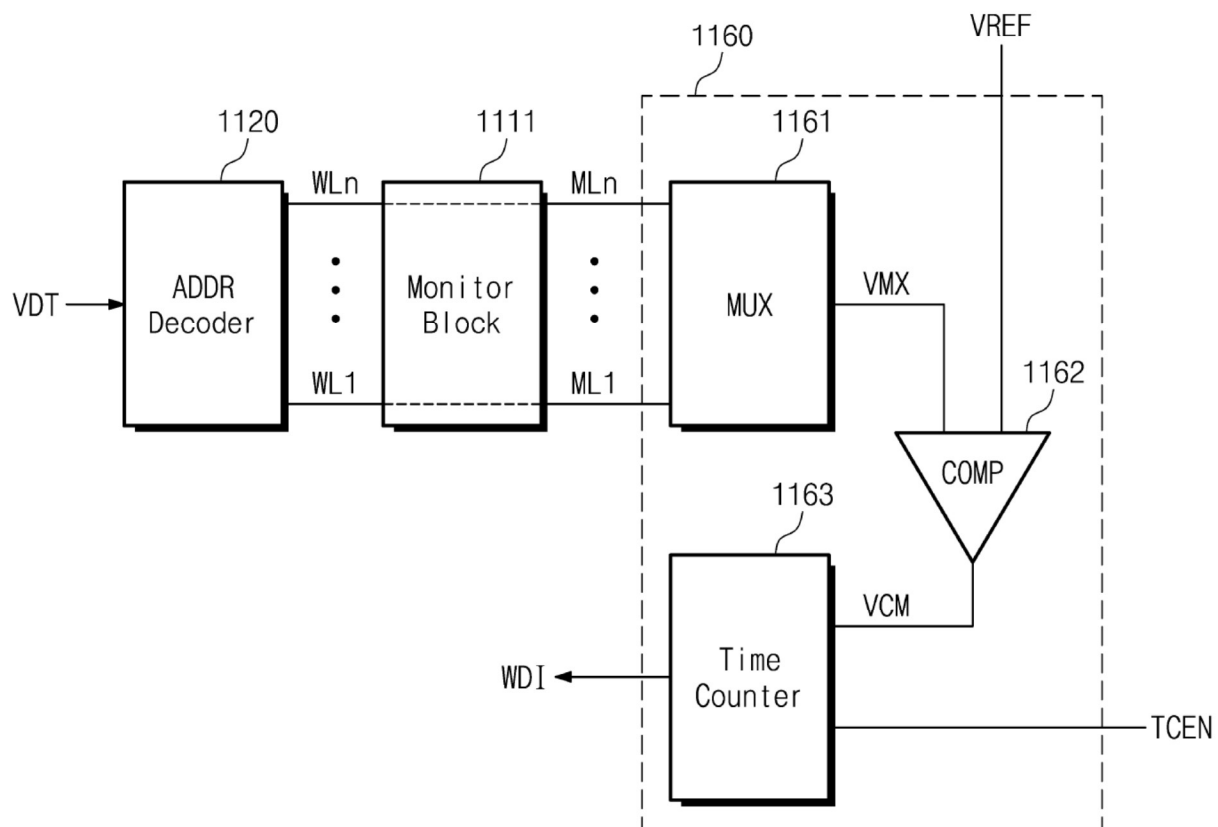


FIG. 16

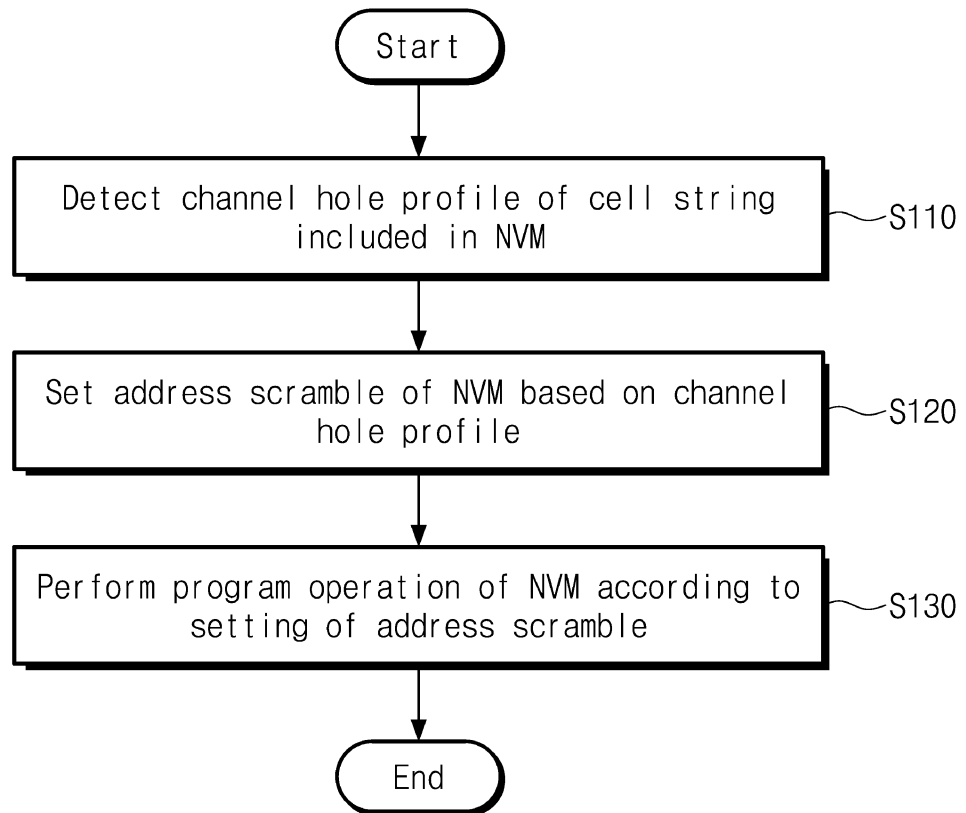
1100



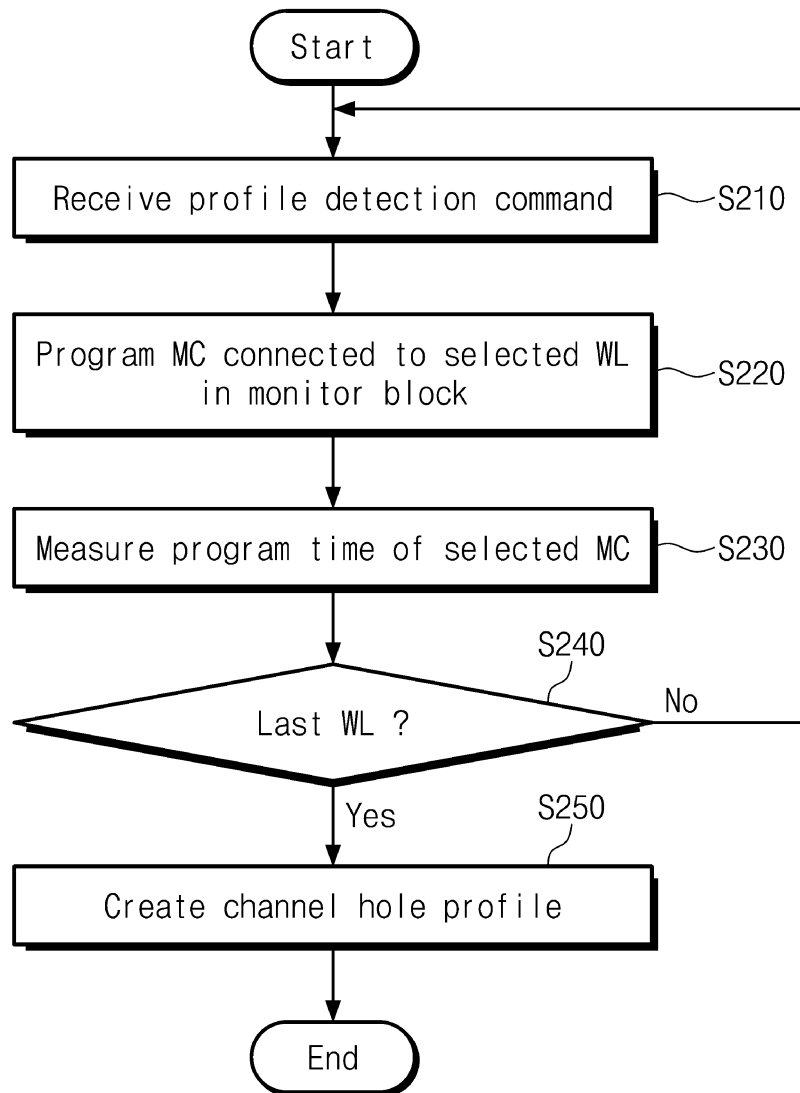
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FIG. 17



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FIG. 18



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FIG. 19



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FIG. 20

