

"MEMORY UNIT COMPRISING A MEMORY AND A PROTECTION UNIT"

The invention relates to a memory unit for use in a data processing system, said memory unit comprising a protection unit and a memory for the storage of at least one program comprising a plurality of program words, said memory having a port for the exchange of address words for corresponding program words.

Such a data processing system is described in the Dutch patent application nr. 82 01 847 laid open to public inspection on 01.12.1983. The protection unit of the memory unit protects the program words stored in the memory against illegal copying by unauthorised copiers.

Devices which are controlled by a data processor comprise a memory, for example a ROM or a PROM, in which programs and other information (termed software), are stored in the form of program words for the execution of data processor operations. The design of such software is time consuming and is also expensive. Therefore, it is important to prevent unauthorised copying of such software.

According to the present invention there is provided a memory unit for use in a data processing system, said memory unit comprising a protection unit and a memory for the storage of at least one program comprising a plurality of program words, said memory having a port for the exchange of address words for corresponding program words, said protection unit comprising:

- recognition means connected to said port and provided for recognizing out of the flow of program words at said port those which belong to a predetermined group, the program words of said predetermined group comprising an address part for addressing a further program word, said recognition means being further provided for generating a command signal in response to the recognition of a program word of said predetermined group;
- first modification means connected to said port and having a control input connected to said recognition means for receiving said command signal, said first modification means comprising an adder for forming a modified program word by

- adding, under control of a received command signal, a value to the address part of a received program word in respect of which that command signal was generated, said first modification means being connected to a data output of said memory unit for applying said modified program word to a data processor of the data processing system;
- 5
- second modification means connected to an address input of the memory unit for receiving address words from the data processor and having a control input connected to said recognition means for receiving said command signal, said
- 10
- second modification means comprising a subtracting circuit for forming a compensated address word by subtracting, under control of said command signal, said value from a received address word which was generated by said data processor upon
- 15
- reception of said modified program word so as to compensate for the addition performed for obtaining said modified program word, said second modification means being connected with said port for applying said compensated address word to the memory; and
- 20
- a random number generator having a control input connected to said recognition means for receiving said command signal and provided for generating said value under control of a received said command signal, said random number generator having an output connected with said first and second modification means
- 25
- for supplying said value thereto.

In a data processing system embodying a memory unit according to the invention, there is always some difference between the flow of information words at the port of the memory and the flow of data and address signals between the memory unit and the data processor, notwithstanding that a program is copied

30

or not. During a normal execution of a program, i.e. when the program is executed under control of the data processor and the instructions are executed according to the content of the program words, the second modification means will modify a

35

received address signal. This modification will compensate for the modification performed by the first modification means so

that the correct address word will be supplied to the port of the memory. The normal execution will thus not be perturbed. However when the program is copied, the modified program word, outputted at the data output of the memory unit, will be
5 included in the copied program, making the copied program useless.

A preferred embodiment of a memory unit according to the invention is characterised in that each of said program words of said predetermined group comprises an instruction which acts on
10 an equal-step progression of a program counter of the data processor. Instructions which act on an equal-step progression of the program counter are instructions which causes the program counter to increment (or decrement) with more than one unit step, such as for example JUMP or GO-TO instructions. Those
15 instructions have an address part which comprises information about the address of the subsequent program word to be addressed during the normal execution of the program. A modification of that address part applied by the first modification operation can efficiently disturb a copied program.

20 A further preferred embodiment of a memory unit according to the invention is characterised in that the program words of said predetermined group comprise an opcode part, said recognition means comprising an opcode decoder for decoding the opcode part of the program words.

25 Alternatively said recognition means may comprise an address decoder for decoding the address words which correspond to the program words which belong to said predetermined group.

Simple implementations of the recognition means are thus obtained.

30 A memory unit according to the invention may be constructed using an integrated circuit technique, with the memory and the protection unit being integrated on the same chip surface.

35 A memory unit according to the invention may be embodied in a video game module.

(B)

A data processing system embodying a memory unit according to the invention may comprise a data processor having a data input connected to the data output of the memory unit, an address output connected to the address input of the memory unit, and a program counter which is settable under the control of received data signals.

The invention will now be described in detail with reference to the accompanying drawing in which the sole Figure represents a simplified block diagram of a preferred embodiment of a data processing system embodying a memory unit according to the invention.

The data processing system illustrated in the Figure comprises a memory unit 10 and a data processor 14 for example a microprocessor. The memory unit comprises a memory 12, for example a ROM or a PROM, and a protection unit 24. The data processor and the memory unit are connected to each other by means of an address bus 11 and a data bus 13. The memory and the protection unit are connected to each other by means of an internal bus 23. The protection unit comprises recognition means 16 which have a first input connected to the internal bus. The protection unit also comprises first modification means 17 which have a second input connected to the internal bus 23 and a first data output connected to the data bus 13, and second modification means 15 which have an address input connected to the address bus 11 and an address output connected to the internal bus 23.

The memory 12 is used for the storage of at least one program which can be executed by the data processor. The program(s) comprises a plurality of program words. Each program word is generally composed of a number of binary bits. Each program word is stored at a respective memory location having its respective address. A port of the memory is connected to the internal bus for supplying address words to the memory in order to fetch the respective program words which belong to

that address word.

As suggested by its denomination the protection unit 24 serves to protect the program words, especially against illegal copying. Therefore the protection unit provides that for a number of program words outputted at the terminal of the memory, a modification operation is applied thereon.

Several implementations are possible for the protection unit. The operation of the data processing system will now be described with reference to a preferred embodiment for the protection unit. In this preferred embodiment of the protection unit, the recognition means 16 comprise a jump instruction decoder 18 and a random number generator 19. The first modification means 17 comprise an adder 25 and the second modification means 15 comprise a subtracting circuit 26. The random number generator has an output connected via a line 20 to an input of the adder and to an input of the subtracting circuit.

Among the program words stored in the memory there are the well known jump instructions which act on the equal-step progression of the program counter. These jump instructions are recognizable by their characteristic opcode (operational code) part. The jump instruction decoder 18, which is an opcode decoder, decodes the opcode parts of the program words outputted at the port of the memory and supplied to the internal bus 23. When a jump instruction is decoded, the jump instruction decoder generates a command signal which is supplied via line 21 to the random number generator 19, to the adder 25, and to the subtracting circuit 26. Thereupon the random number generator 19 generates a random number which is supplied via line 20 to the adder and the subtracting circuit. The adder, which is connected to the internal bus 23, has also received the program word which comprises the jump instruction. Under control of the command signal the adder will add the random number to the address part (indicating the address to which to jump) of that jump instruction and produces a pseudo-jump address.

The modified program word with the pseudo-jump address is now transmitted via the data bus 13 to the data processor 14. Thereupon the program counter will indicate the program word at that pseudo-address. When the data processor 14 thereafter addresses, via the address bus 11, the memory unit to acquire the program word at the pseudo-address, this address is transmitted to the subtracting circuit 26 of

the second modification means. After reception of the pseudo-address, the subtracting circuit subtracts the random number from the pseudo-address and transmits the thus obtained original address to the memory. The jump instruction is thus correctly executed.

5 Each subsequent program word outputted from the memory 12 which is not a jump instruction is transmitted through the adder 25 onto data bus 13 without alteration. Since the program counter of the data processor, however, has been stepped forward to the pseudo-address, the second modification means 15 retains the random number for subtraction from each of the addresses placed on address bus 11 by the
10 data processor before transmission to the memory.

 This continues until another jump instruction is provided on the port of the memory 12. When that occurs jump instruction decoder 18 again causes the random number generator 19 to operate to
15 place another random number in adder 25 and subtracting circuit 26. The adder 25 operates as previously to place a pseudo-jump address on the data bus 13. The second modification means 15 substitutes the new random number for the old random number in order to address the memory 12 properly when the data processor transmits the pseudo-jump address
20 to the memory unit 10. In this way a predetermined group of information words in the form of jump instructions stored in some of the memory locations of the memory 12 cause the first modification means 17 to change those jump addresses before transmission on the data bus 13.

 Suppose now that the program words stored in the memory 12
25 are copied. The pseudo-addresses supplied on data bus 13 will then be incorporated in the copied program, making that copied program useless, because a wrong location in the program will be addressed if the copied program is executed. Further if the copier addresses the memory unit after the output of the pseudo-address, the supplied
30 address will be modified by the second modification means. The copier will thus not know which location of the memory has been addressed. The copied program is thus totally useless.

 In one form of the invention each jump instruction transmitted from the memory would contain a binary 1 in one bit location. In all
35 other memory locations of the memory that bit location would contain a binary 0. In that embodiment the jump instruction decoder would take the form of a circuit which would respond to the binary 1 in the prescribed bit location and would consequently cause the generation of

the command signal as previously described.

In an alternative form, all jump instructions would be located in a particular section of the memory and the recognition means 16 would comprise a comparator which would respond to the addresses of the locations in that section and cause the random number generator 19 to operate as previously described. The comparator is then for example connected to a storage element where said addresses are stored as identifier information in order to enable the comparison. When all jump instructions are located in a particular section of the memory 12, then the recognition means could for example comprise an address decoder for decoding the addresses of that particular section. Other types of recognition means are also known to those skilled in the art and could be substituted for those disclosed.

The recognition means could also react on other instructions than only the jump instructions, such as for example GO-TO instructions or any other instructions which act on an equal step progression of the program counter.

It is understood that various modifications to the above described system of the invention will become apparent to those skilled in the art and that the arrangement described herein is for illustrative purposes and is not to be considered restrictive.

25

30

35

CLAIMS:-

1. A memory unit for use in a data processing system, said memory unit comprising a protection unit and a memory for the storage of at least one program comprising a plurality of program words, said memory having a port for the exchange of address words for corresponding program words, said protection unit comprising:
- recognition means coupled to said port and provided for recognizing out of the flow of program words at said port those which belong to a predetermined group, the program words of said predetermined group comprising an address part for addressing a further program word, said recognition means being further provided for generating a command signal in response to the recognition of a program word of said predetermined group;
 - first modification means coupled to said port and having a control input connected to said recognition means for receiving said command signal, said first modification means comprising an adder for forming a modified program word by adding, under control of a received command signal, a value to the address part of a received program word in respect of which that command signal was generated, said first modification means being connected to a data output of said memory unit for applying said modified program word to a data processor of the data processing system;
 - second modification means connected to an address input of the memory unit for receiving address words from the data processor and having a control input connected to said recognition means for receiving said command signal, said second modification means comprising a subtracting circuit for forming a compensated address word by subtracting, under control of said command signal, said value from a received address word which was generated by said data processor upon reception of said modified program word so as to compensate for the addition performed for obtaining said modified program word, said second modification means being coupled to said port for applying said compensated address word to the memory; and
 - a random number generator having a control input connected to said



* C L M S *

recognition means for receiving said command signal and provided for generating said value under control of a received said command signal, said random number generator having an output connected with said first and second modification means for supplying said value thereto.

2. A memory unit as claimed in Claim 1, characterized in that each of said program words of said predetermined group comprises an instruction for acting on an equal-step progression of a program counter of the data processor.

3. A memory unit as claimed in Claim 1 or Claim 2, characterized in that the program words of said predetermined group comprise an opcode part, said recognition means comprising an opcode decoder for decoding the opcode part of the program words.

4. A memory unit as claimed in Claim 1 or Claim 2, characterized in that said recognition means comprise an address decoder for decoding the address words which correspond to the program words which belong to said predetermined group.

5. A memory unit as claimed in Claim 1 or Claim 2, characterized in that said recognition means comprise a storage element for storing identifier information for each of the program words of said predetermined group, and a comparator having a first input connected to said storage element and a second input coupled to said port for comparing the identifier information with information words at said port and generating said command signal upon correspondence between said identifier information and a said information word.

6. A memory unit as claimed in any preceding Claim, characterized in that each program word of said predetermined group comprises a jump instruction and the address word of the program word to which the jump instruction pertains.

7. A memory unit as claimed in Claim 5, characterized in that said identifier information comprises at least a part of the content of the program words of said predetermined group.

8. A memory unit as claimed in Claim 5, characterized in that said identifier information comprises at least a part of the content



19

of the address words corresponding to the program words of said predetermined group.

9. A memory unit as claimed in any preceding Claim, characterized in that the memory unit is constructed using an integrated circuit technique, and that the memory and the protection unit are integrated on the same chip surface.

10. A memory unit as claimed in any preceding Claim, embodied in a video game module.

11. A memory unit as claimed in any of Claims 1 to 9, embodied in a data processing system comprising a data processor having a data input connected to the data output of the memory unit, an address output connected to the address input of the memory unit, and a program counter which is settable under the control of received data signals.

12. A memory unit for a data processing system, substantially as hereinbefore described with reference to the accompanying drawing.

13. A data processing system embodying a memory unit as claimed in Claim 12.



* C L M S *