

BIAS STABILIZING CIRCUIT

The present invention relates to bias stabilizing circuits, and is concerned particularly with circuits for receiving a message signal by stabilizing the bias of a paging receiver when periodically controlling a voltage source.

Generally, a paging receiver receives a radio frequency signal (hereinafter referred to as RF signal) transmitted by a paging system, and converts it into an intermediate frequency signal that is demodulated into the original logical data. The demodulated signal is an analog signal shaped into a digital waveform based on a reference signal and applied to a controller. The controller identifies the digital data as self-data (i.e. addressed to the correct paging receiver), then generates a calling sound signal through a speaker.

Such a paging receiver usually makes use of a small DC battery, and therefore the power consumption should be minimized so as to lengthen the life of the battery. To this end, the power supplying of the RF components is controlled so as to reduce the power consumption of the battery. The RF components include RF receiver, demodulator and waveform shaping circuit that are the main cause of most of the power consumption.

The RF signal transmitted by the paging system is of a given data form. Assuming the RF signal is in the form of POCSAG codes (Post Office Code Standardization Advisory Group), the signal comprises a preamble part, word sync and frame data. The controller periodically supplies power to the RF components in order to search the preamble part (Preamble Search Mode). If

the preamble part is detected, the controller keeps on supplying power and searches the word sync. If the word sync is detected, the controller stops supplying the power, and thereafter resupplies the power in the self-frame period (Address Search Mode).

5

However, in such a conventional paging receiver, since all the RF components should be supplied with power in the preamble search mode, there occurs a large power consumption. The reason is that the power should be supplied to the RF components before receiving substantial message data, so as to establish a reference signal voltage.

10

In view of the above fact, there is disclosed an apparatus for saving power by sequentially supplying power to the RF components in the U.S. Patent No.4,479,261 issued to Japanese Nippon Electric Co., Ltd. on October 23, 1984, as shown in Figures 1-3 of the accompanying diagrammatic drawings attached to the present application. In this case, generating a voltage source control signal with period J through first and second timers 34 and 35 provided in a controller 13, first and second switch circuits 16 and 17 are sequentially switched on so as to supply the power of a battery 15 to a waveform reshaping circuit 12 and receiver 11.

20

Specifically, if the first timer 34 generates a voltage source control signal as shown in Figure 3B at the time point D1, the first circuit switch 16 is on to apply power to the waveform reshaping circuit 12. Then the output voltage of a low pass filter 21 of the waveform reshaping circuit 12 is supplied as a reference signal to a capacitor 24 connected in parallel to a reference terminal (-) of a voltage comparator 25. Thereafter, if the second timer 35 generates a voltage source control signal as shown in Figure 3C with period

25

K at the time point D2, the second switch circuit 17 is on to supply power to the receiver 11 that converts and demodulates the RF signal received through an antenna 10. Thus the power supply to the waveform reshaping circuit 12 and receiver 11 is controlled with period K, reducing the power consumption
5 of the receiver 11.

In such controlling of the power, the reference voltage charged in the capacitor 24 at the time point D2 when the receiver 11 works to receive does not effectively serve to determine the logical state of the data output from the
10 receiver 11. The reason is that if the receiver 11 works to receive the RF signal after the time point D2, the level of the reference voltage is increased by a resistor 23 and capacitor 24 according to the logical state of the received data, and at the time point D3 the reference voltage is changed to the average voltage of the substantial data.

15 Thus the charged voltage of the capacitor 24 that serves as the reference signal is delayed by periods J and K after generation of the voltage source control signal, and thereby stabilized. Therefore, data received in the period K may suffer a duty change due to an unstable reference voltage, so that there
20 may occur a data receiving error. In order to prevent such error, the reference voltage must be stabilized by sequentially driving the first and second switch circuits 16 and 17 prior to the data receiving. Such stabilizing apparatus is disclosed in U.S. Patent No. 4,631,737 issued to the Motorola Company of the U.S.A. on December 23, 1986.

25 This bias stabilizing apparatus is briefly described with reference to Figures 4-7 of the accompanying diagrammatic drawings. The RF signal received through an antenna 40 is converted and demodulated in a receiver 41.

The demodulated signal output from the receiver 41 has a voltage corresponding to its logical state, and is applied to the comparing terminal of a limiter 44. The demodulated signal is also applied to a peak detector 45 and a valley detector 47. The peak detector 45 holds the peak value of the received data as shown in Figure 7B, while the valley detector 47 holds the valley value of the received data as shown in Figure 7C. The peak and valley values are averaged and applied to the limiter 44 as a reference voltage. Thus, the limiter 44 receives as the reference signal the voltage averaged according to the logical state of the received data, and therefore determines the logical state of the demodulated signal input through the comparing terminal, applying it to the controller.

Figures 5 and 6 are respectively the circuits of the peak and valley detectors. When so detecting the peak and valley values, there occurs a delay time caused by each component. As shown in Figure 7, period d1-d3 is the delay time that is the charging time of a capacitor 56. Only by charging the capacitor 56 can transistors 54 and 74 be operated, which transistors are respectively the static current sources of the peak and valley detectors 45 and 47. After the time point d3, there is needed the period d3-d4 in order to charge a capacitor 60 to the peak value and to discharge it to the valley value. Consequently it is the time point d4 when the limiter 44 works to determine the data with the substantially stabilized bias.

Such bias stabilizing apparatus, using the average of the peak and valley values of the received data, needs all the RF components (RF receiver, demodulator, waveform reshaping circuit) to be provided with the voltage source, thus increasing the power consumption.

Preferred embodiments of the present invention aim to provide a paging receiver for accurately receiving a message signal by quickly stabilizing the bias.

5 Another aim is to provide a circuit for stabilizing the bias of a paging receiver that may supply a signal having the center frequency of an RF modulated signal so as to generate a reference voltage to determine the logical state of data according to the characteristics of a demodulator.

10 Another aim is to provide a circuit for reducing power consumption by supplying the power to RF components in a receiving period after bias stabilization.

15 According to a first aspect of the present invention, there is provided a circuit for stabilizing the bias of a paging receiver for processing a message signal, the circuit comprising:

20 a voltage source switch means for periodically supplying voltage to RF components of the paging receiver during first and second periods;

 a controller for generating an oscillation control signal during said first period;

25 an oscillator means for generating a given frequency signal in response to said oscillation control signal;

a demodulation means for receiving the output signal of said oscillator means during said first period to generate a demodulated signal having the voltage of said bias; and

- 5 a waveform reshaping means for receiving the output signal of said demodulation means during said first period to stabilize said bias.

Preferably, said oscillator means comprises an oscillator for generating a signal having the center frequency of a received modulated signal, said oscillator being supplied with a voltage of said voltage source via said voltage source switch means, and an oscillation switch having an input and output respectively connected to said oscillator means and demodulation means for applying the output signal of said oscillation means to said demodulation means by being switched on by said oscillation control signal during said first period.

Preferably, said demodulation means demodulates the output signal of said oscillator means so as to produce a bias level signal during said first period, said bias level having the intermediate voltage of said message signal, and produces a demodulated signal according to the logical state of an RF modulated signal received during said second period.

Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by receiving the demodulated signal from said demodulation means during said first period and to produce digital data in reference to said bias by receiving the demodulated

signal from said demodulation means through said message signal input during said second period.

5 Preferably, said oscillator means comprises an oscillator for providing a center frequency signal to said demodulation means during said first period, and an oscillator switch for connecting said demodulation means and oscillator in response to said oscillation control signal.

10 Preferably, said demodulation means demodulates the output signal of said oscillator so as to produce a demodulated signal for said bias having the intermediate voltage of said message signal during said first period, and then produces a demodulated signal according to the logical state of an RF modulated signal received during said second period.

15 Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by receiving the demodulated signal from said demodulation means during said first period and to produce digital data in reference to said bias by receiving the demodulated
20 signal from said demodulation means through said message signal input during said second period.

According to a second aspect of the present invention, there is provided a circuit for stabilizing the bias of a paging receiver for processing a message
25 signal, the circuit comprising:

a controller for generating a voltage source control signal during first and second periods, and an oscillation control signal during the first period;

a voltage source switch means for connecting RF components of the paging receiver and a voltage source in response to said voltage source control signal;

5 an oscillator means for generating a given frequency signal in response to said oscillation control signal;

an RF receiver for converting an RF modulated signal into an intermediate frequency signal;

10

a demodulation means for demodulating the output signal of said oscillator produced during said first period so as to produce a demodulated signal for said bias having a reference voltage, and then producing a demodulated signal according to the logical state of said intermediate
15 frequency signal received during said second period; and

20

a waveform reshaping means for stabilizing said bias by receiving the demodulated signal from said demodulation means during said first period and for identifying the logical state of the demodulated signal produced during said second period in reference to said bias.

25

Preferably, said oscillator means comprises an oscillator for generating the center frequency signal of said RF modulated signal, said oscillator being connected to said voltage source via said voltage source switch means, and an oscillator switch for connecting said demodulation means and oscillator in response to said oscillation control signal during said first period.

Preferably, said demodulation means demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the logical state of a demodulated signal of said first or third voltage received during said second period.

Preferably, said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal during said first period, and an oscillator switch for connecting said oscillator and demodulation means in response to said oscillation control signal.

Preferably, said demodulation means demodulates the intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the

logical state of a demodulated signal of said first or third voltage received during said second period.

According to a third aspect of the present invention, there is provided
5 a circuit for stabilizing the bias of a paging receiver for processing a message signal, the circuit comprising:

a controller for generating a first voltage source control signal and an oscillation control signal during a first period, and said first voltage source
10 control signal and a second voltage source control signal during a second period;

a voltage source switch means consisting of first and second voltage source switches to connect RF components of the paging receiver and a
15 voltage source in response to said first or second voltage source control signal;

an oscillator means for generating a given frequency signal in response to said oscillation control signal;

20 an RF receiver connected to said second voltage source switch for converting an RF modulated signal into an intermediate frequency signal;

a demodulation means connected to said first voltage source switch for demodulating the output signal of said oscillator means produced during said
25 first period so as to produce a demodulated signal for said bias having a reference voltage, and then producing a demodulated signal according to the logical state of the modulated signal produced by said RF receiver during said second period; and

a waveform reshaping means connected to said first voltage source switch for stabilizing said bias by receiving the demodulated signal from said demodulation means during said first period and for identifying the logical state of the demodulated signal produced during said second period in
5 reference to said bias.

Preferably, said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal, and an oscillator switch for connecting said oscillator and demodulation means in response to
10 said oscillation control signal.

Preferably, said demodulation means demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said
15 RF receiver during said second period into a first or third voltage according to its logical state.

Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged
20 to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the logical state of a demodulated signal of the first or third voltage received during said second period.

Preferably, said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal during said first period, and an oscillator switch for connecting said oscillator and demodulation means in response to said oscillation control signal.

5

Preferably, said demodulation means demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

10

Preferably, said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the logical state of a demodulated signal of the first or third voltage received during said second period.

15

The invention extends to a paging receiver incorporating a circuit according to any of the preceding aspects of the invention.

20

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 8 to 14 of the accompanying diagrammatic drawings, in which:

25

Figure 8 is a block diagram of one example of a paging receiver embodying the present invention;

Figure 9 illustrates characteristics of a demodulation circuit of the circuit of Figure 8;

5 Figure 10 is one example of a more detailed circuit diagram of a paging receiver as shown in Figure 8;

Figure 11 illustrates examples of waveforms of the circuit of Figure 10;

10 Figure 12 is another example of a more detailed circuit diagram of a second paging receiver as shown in Figure 8;

Figure 13 illustrates examples of waveforms of the circuit of Figure 12; and

15 Figure 14 is a block diagram of another example of a paging receiver embodying the present invention.

In the figures, like reference numerals denote like or corresponding parts.

20

Referring to Figure 8, an RF receiver 101 amplifies an RF modulated signal of VHF or UHF band received through an antenna 100, and converts it into an intermediate frequency signal (IF signal) having the logical value of the received data. A demodulation circuit 102 demodulates the IF signal received during a bias stabilization period into a second voltage V2, and the IF data output from the RF receiver 101 during a data receiving period into a first or third voltage V1 or V3 according to the logical state of the data. A waveform reshaping circuit 103 takes as a stabilized reference bias the

demodulated signal of the second voltage V2 output from the demodulation circuit 102 during the bias stabilization period, and shapes the demodulated signal of the first or third voltage V1 or V3 received during the data receiving period into digital data of digital logic in reference to the bias.

5

A controller 104 periodically generates a voltage source control signal, as well as an oscillation control signal during the bias stabilization period, and processes the data output from the waveform reshaping circuit 103 during the data receiving period so as to perform the paging function. A voltage source
10 switch circuit 105 is switched on in response to the voltage source control signal so as to connect a voltage source 106 to the RF receiver 101, demodulator 102 and waveform reshaping circuit 103. An oscillation circuit 108 generates the IF signal. An oscillator switch 107 with an input connected to the oscillation circuit 108 is switched on in response to the oscillation
15 control signal so as to generate the IF signal to the demodulation circuit 102. Hereinafter, the bias stabilization period is referred to as a first period, and the data receiving period as a second period.

Referring to Figure 9A for illustrating the characteristics of the
20 intermediate frequency band, IF represents the intermediate frequency signal output from the oscillator 108, $IF + \Delta f$ the data of the logic value "1" output from the RF receiver 101, and $IF - \Delta f$ the data of the logic value "0" output from the RF receiver 101. (In this example, $\Delta f = 4.5$ kHz). Hence, the IF signal has the center frequency of the data signals output from the RF receiver
25 101.

Referring to Figure 9B, the demodulation circuit 102 demodulates the IF signal into the second voltage V_2 , $IF - \Delta f$ into the first voltage V_1 , and $IF + \Delta f$ into the third voltage V_3 .

5 Referring again to Figure 8, the controller 104 controls the power supplied to the RF receiver 101, demodulation circuit 102, and waveform reshaping circuit 103 so as to prolong the life of the voltage source 106. If the controller 104 periodically generates the voltage source control signal in order to search the RF signal, the voltage source switch circuit 105 is
10 switched on so as to connect the voltage source 106 to the RF components. Also, the controller 104 generates an oscillation control signal during the first period of stabilizing the reference voltage of the waveform reshaping circuit 103. At this time, the RF components are operated as well as the oscillation circuit 108 by the voltage source 106. Then the oscillator switch 107 is
15 switched on in response to the oscillation control signal so as to apply the IF signal output from the oscillation circuit 108 to the demodulation circuit 102 during the first period.

The demodulation circuit 102, working as shown in Figure 9B,
20 demodulates the IF signal as shown in Figure 9A into a signal of the second voltage V_2 according to the demodulation characteristics as shown in Figure 9B. The waveform reshaping circuit 103 receives the output signal of the demodulation circuit 102 so as to stabilize the reference bias signal into the second voltage V_2 . The bias stabilization period is determined by finding the
25 time during which the reference bias signal of the waveform reshaping circuit 103 finally takes the second voltage V_2 .

The bias stabilization period completed, the controller 104 stops the generation of the oscillation control signal. Then the oscillator switch 107 is switched off, so as to block the output of the oscillation circuit 108 applied to the demodulation circuit 102.

5

Thereafter, the RF receiver 101 converts the received RF modulated signal into a signal of the IF band. The output signal of the RF receiver 101 is offset from the IF by a frequency deviation Δf , having the logic value "1" or "0". The demodulation circuit 102 demodulates the output signal of the RF receiver 101 as shown in Figure 9B, in which demodulation the signal $IF + \Delta f$ of the logic value "1" generates the third voltage V3, and the signal $IF - \Delta f$ of the logic value "0" the first value V1.

The waveform reshaping circuit holds the bias as the second voltage V2 during the bias stabilization period. Hence, the demodulated signal of the first or third voltage V1 or V3 output from the demodulation circuit 102 during the second period is compared with the bias of the second voltage V2 and shaped into a digital square wave in the waveform reshaping circuit 103, applied to the controller 104. Since the bias of the waveform reshaping circuit 103 has the center value of the demodulated signals having the logical states "1" or "0", the duty ratio of the shaped data may remain exactly at 50%.

Two methods may generally be used for the controller 104 to provide the voltage source to RF components. One is to simultaneously connect the voltage source to the RF receiver 101, demodulation circuit 102 and waveform reshaping circuit 103, which is illustrated as a first embodiment in Figure 10. The other is to firstly connect the voltage source to the demodulation circuit 102 and waveform reshaping circuit 103 during the first

period, and then to the RF receiver 101 during the second period, which is illustrated as a second embodiment in Figure 12.

Referring to Figure 10, the controller 104 periodically generates the voltage source control signal as shown in Figure 11B, and also the oscillation control signal having a first period X1 as shown in Figure 11C. The first period X1 is the bias stabilization period that is determined by finding the time during which the bias of voltage comparator 216 finally takes the second voltage V2.

10

Hence, if there are generated the voltage source control signal and oscillation control signal at the time point T1, transistor 222 is switched on in response to the voltage control signal as shown in Figure 11B so as to connect the voltage source to the RF receiver 101, demodulation circuit 102 and waveform reshaping circuit 103 as well as to the oscillation circuit 108.

15

In addition, if the oscillator switch 107 is switched on in response to the oscillation control signal as shown in Figure 11C, the oscillation circuit 108 applies the IF signal to the demodulation circuit 102. The RF receiver 101 driven by the voltage source control signal as shown in Figure 11B converts the RF modulated signal received through the antenna 100 into a signal of the IF band at the time point T1.

20

The demodulation circuit 102 receives the outputs of the RF receiver 101 and oscillation circuit 108 during the first period after the time point T1. Demodulator 201 performs demodulation by multiplying the IF signal that is received through capacitor 202 and frequency discriminator 203 and whose

25

phase is delayed by 90° , and the IF signal output from the oscillation circuit 108 (differential amplifying).

Thus the demodulation circuit 102 demodulates the IF signal into a demodulated signal of the second voltage V2, which signal is rectified through a low pass filter 211 to the second voltage V2 supplied to resistor 214 and capacitor 215. Hence the voltage of node 217 begins to increase, and serves as the bias of comparator 216. As a result, the reference input terminal of the waveform reshaping circuit 103 is biased with the second voltage V2 prior to the second period of data receiving.

At the first period X1 of bias stabilization, since the demodulation circuit 102 demodulates the IF signal output from the oscillation circuit 108 into a demodulated signal of the second voltage V2, the node 217 of the reference input terminal of the waveform reshaping circuit 103 is promptly charged with the second voltage V2. From the time constant of the resistor 214 and capacitor 215, there may be determined the time taken to bias the node 217 with the second voltage V2. The controller 104 generates the oscillation control signal during the determined time, and the period of the oscillation control signal is the bias stabilization period X1.

The controller 104 switches off the oscillation control signal at the time point T2, when the bias stabilization period is completed, as shown in Figure 11C. Then the oscillator switch 107 is off so as to block the output of the oscillation circuit 108 from being applied to the demodulation circuit 102. Then the output of the RF receiver 101 is applied to the demodulation circuit 102. The RF receiver 101 converts the received RF modulated signal into a signal of the IF band, so that the output signal of the RF receiver is offset

from the IF by a frequency deviation Δf according to the logical state thereof, i.e. "1" or "0" as shown in Figure 9A.

Consequently, the demodulation circuit 102 generates a demodulated
5 signal of the first or third voltage V1 or V3 according to the logical state of the received data. The demodulated signal is rectified through low pass filter 211, and applied to the voltage comparator 216. The voltage comparator 216 compares the demodulated signal of the first or third voltage V1 or V3 with
10 the bias of the second voltage V2 already established at the node 217 so as to generate a digital data signal of a constant duty ratio during the second period X2 of data receiving. This operation is only kept on in response to the voltage source control signal output from the controller 104 during the self-frame data receiving period X2.

15 Hence, there are simultaneously generated the voltage source control signal and oscillation control signal at the time point T1 for periodically providing the voltage source, as shown in Figures 11B and 11C. In this case, since the first period X1 of bias stabilization is the time for the node 217 to finally take the second voltage V2, the time point T1 must precede the data
20 receiving period by the bias stabilization period X1.

Since the oscillation control signal is off at the time point T2 of data receiving as shown in Figure 11C, the demodulation circuit 102 demodulates
25 the received RF modulated signal into a signal having the logical level of the original data, which is shaped by the waveform reshaping circuit 103 into a digital signal with a constant duty ratio based on the stabilized bias signal. The self-data receiving period for the operation being terminated, the voltage source control signal becomes off, to reduce the power consumption.

The embodiment of Figure 12 will now be described. In the embodiment of Figure 10, the controller 104 generates the voltage source control signal so as to simultaneously connect the voltage source to all the RF components. Meanwhile, the bias stabilization period X1 is established prior to the time point T2 of self-data receiving, and therefore the RF receiver 101 unnecessarily consumes power during the bias stabilization period X1. Namely, the RF receiver 101 makes a large power consumption in order to amplify a small RF modulated signal converted into the IF signal. However, in the second embodiment of Figure 12, the RF receiver 101 is not connected to the voltage source during the first period X1 of bias stabilization that is achieved by the output of the oscillation circuit 108. Namely, the first voltage source control signal and oscillation control signal are generated at the time point T1 as shown in Figures 13B and 13C. Then, the voltage source 106 is connected to the demodulation circuit 102, waveform reshaping circuit 103 and oscillation circuit 108, and the oscillator switch 107 is switched on. At this time, since the voltage source is not connected to the RF receiver 101, the demodulation circuit 102 demodulates the IF signal output from the oscillation circuit 108 into a signal of the second voltage V2. Thus the node 217 for the reference signal is charged with the demodulated signal of the second voltage V2 during the first period X1.

The first period X1 of bias stabilization being terminated, the controller 104 turns off the oscillation control signal at the time point T2 as shown in Figure 13C, and simultaneously turns on the second voltage source control signal as shown in Figure 13D. At this time, the first voltage source control signal is kept on as shown in Figure 13B. Hence, transistor 226 is turned on to connect the voltage source to the RF receiver 101 from the time point T2. Thus the RF receiver 101 converts the received RF modulated signal into a

signal of the IF band. The demodulation circuit 102 demodulates the signal of the IF band into a signal of the first or third voltage V1 or V3 according to the logical state thereof. The waveform reshaping circuit 103 compares the demodulated signal of the first or third voltage V1 or V3 of the demodulation circuit 102 with the bias already stabilized into the second voltage V2 during the first period X1, so as to generate a digital signal having a duty ratio of 50% according to the logical state of the demodulated signal.

By way of example, in the above described embodiments, the RF receiver 101 converts the RF modulated signal of UHF or VHF band into a signal of the IF band offset by 4.5KHz from the center frequency 455KHz according to the logical state thereof. Namely, the modulated signal of the logical state "1" output from the RF receiver 101 has the frequency of $455\text{KHz} + 4.5\text{KHz}$, while the modulated signal of the logical state "0" has the frequency of $455\text{KHz} - 4.5\text{KHz}$. Meanwhile, the oscillation circuit 108 generates a signal of 455KHz that is the center frequency of the IF band signal output from the RF receiver 101. In this case, there may be used CSB 455J (ceramic resonator of the Murata Company) as oscillator 234, and TC 4S69F of the Toshiba Company as inverters 231, 232. Capacitors 235 and 236 may have a capacitance of 100PF, and resistor 233 may be of $1\text{M}\Omega$. The oscillator switch 107 may be an analog switch with + and - polarities, for which TC4S66F of the Toshiba Company may be used.

Referring to Figure 14 for illustrating a modified embodiment of the invention, the output of the voltage source switch circuit 105 is connected to the input of the oscillator switch 107 whose output is connected to the voltage source input of the oscillation circuit 108 whose output is connected to the input of the demodulation circuit 102. The other parts have the same

construction as those of Figure 8. The controller 104 simultaneously generates the voltage source control signal and oscillation control signal during the first period X1 of bias stabilization. Then the voltage source switch circuit 105 is turned on so as to connect the voltage source 106 to the RF components and to the input of the oscillator switch 107. The oscillator switch 107 receives the oscillation control signal through the control terminal so as to connect the voltage source to the voltage source input of the oscillation circuit 108. Then the oscillation circuit 108 generates the IF signal to the demodulation circuit 102. The demodulation circuit 102 demodulates the output signal of the oscillation circuit 108 into a signal of the second voltage V2 applied to the waveform reshaping circuit 103 to stabilize the bias into the level of the second voltage V2.

The first period X1 being terminated, the controller 104 turns off the oscillation control signal. Then the oscillator switch 107 is switched off, so that the oscillation circuit 108 is disconnected from the voltage source, stopping the oscillation. Then the demodulation circuit 102 demodulates the modulated signal of the IF band output from the RF receiver 101 during the second period X2. The waveform reshaping circuit 103 compares the demodulated signal with the bias already established so as to generate a digital signal.

Hence, the oscillation circuit 108 is only supplied with power during the first period X1, and therefore does not perform unnecessary oscillation, thus saving power.

The bias stabilization circuit of Figure 14 may comprise the circuit of the embodiment of Figure 10 wherein the voltage source is simultaneously

connected to the RF receiver 101, demodulation circuit 102 and waveform
reshaping circuit 103, or the circuit of the embodiment of Figure 12 wherein
the voltage source is firstly connected to the demodulation circuit 102 and
waveform reshaping circuit 103, and then secondly to the RF receiver 101
5 during the second period X2. Moreover, in the embodiment of Figure 14, the
oscillator switch 107 controls the path of the voltage source, and therefore may
consist of a conventional switching element instead of an analog switch.

CLAIMS

1. A circuit for stabilizing the bias of a paging receiver for processing a message signal, the circuit comprising:

5

a voltage source switch means for periodically supplying voltage to RF components of the paging receiver during first and second periods;

10 a controller for generating an oscillation control signal during said first period;

an oscillator means for generating a given frequency signal in response to said oscillation control signal;

15 a demodulation means for receiving the output signal of said oscillator means during said first period to generate a demodulated signal having the voltage of said bias; and

20 a waveform reshaping means for receiving the output signal of said demodulation means during said first period to stabilize said bias.

2. A circuit according to Claim 1, wherein said oscillator means comprises an oscillator for generating a signal having the center frequency of a received modulated signal, said oscillator being supplied with a voltage of
25 said voltage source via said voltage source switch means, and an oscillation switch having an input and output respectively connected to said oscillator means and demodulation means for applying the output signal of said



oscillation means to said demodulation means by being switched on by said oscillation control signal during said first period.

3. A circuit according to Claim 1 or 2, wherein said demodulation means
5 demodulates the output signal of said oscillator means so as to produce a bias level signal during said first period, said bias level having the intermediate voltage of said message signal, and produces a demodulated signal according to the logical state of an RF modulated signal received during said second period.

10

4. A circuit according to Claim 1, 2 or 3, wherein said waveform
reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference
15 signal input by receiving the demodulated signal from said demodulation means during said first period and to produce digital data in reference to said bias by receiving the demodulated signal from said demodulation means through said message signal input during said second period.

5. A circuit according to Claim 1, wherein said oscillator means
20 comprises an oscillator for providing a center frequency signal to said demodulation means during said first period, and an oscillator switch for connecting said demodulation means and oscillator in response to said oscillation control signal.

25 6. A circuit according to Claim 5, wherein said demodulation means demodulates the output signal of said oscillator so as to produce a demodulated signal for said bias having the intermediate voltage of said message signal during said first period, and then produces a demodulated



signal according to the logical state of an RF modulated signal received during said second period.

7. A circuit according to Claim 5 or 6, wherein said waveform reshaping
5 means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by receiving the demodulated signal from said demodulation means during said first period and to produce digital data in reference to said bias by receiving the demodulated signal from said demodulation means through said
10 message signal input during said second period.

8. A circuit for stabilizing the bias of a paging receiver for processing a message signal, the circuit comprising:

15 a controller for generating a voltage source control signal during first and second periods, and an oscillation control signal during the first period;

a voltage source switch means for connecting RF components of the
paging receiver and a voltage source in response to said voltage source control
20 signal;

an oscillator means for generating a given frequency signal in response to said oscillation control signal;

25 an RF receiver for converting an RF modulated signal into an intermediate frequency signal;



a demodulation means for demodulating the output signal of said oscillator produced during said first period so as to produce a demodulated signal for said bias having a reference voltage, and then producing a demodulated signal according to the logical state of said intermediate
5 frequency signal received during said second period; and

a waveform reshaping means for stabilizing said bias by receiving the demodulated signal from said demodulation means during said first period and for identifying the logical state of the demodulated signal produced during
10 said second period in reference to said bias.

9. A circuit according to claim 8, wherein said oscillator means comprises an oscillator for generating the center frequency signal of said RF modulated signal, said oscillator being connected to said voltage source via said voltage
15 source switch means, and an oscillator switch for connecting said demodulation means and oscillator in response to said oscillation control signal during said first period.

10. A circuit according to Claim 9, wherein said demodulation means
20 demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

25 11. A circuit according to Claim 10, wherein said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to



produce digital data based on the logical state of a demodulated signal of said first or third voltage received during said second period.

5 12. A circuit according to Claim 8, wherein said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal during said first period, and an oscillator switch for connecting said oscillator and demodulation means in response to said oscillation control signal.

10 13. A circuit according to Claim 12, wherein said demodulation means demodulates the intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

15 14. A circuit according to Claim 13, wherein said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to
20 produce digital data based on the logical state of a demodulated signal of said first or third voltage received during said second period.

15. A circuit for stabilizing the bias of a paging receiver for processing a message signal, the circuit comprising:

25

a controller for generating a first voltage source control signal and an oscillation control signal during a first period, and said first voltage source



control signal and a second voltage source control signal during a second period;

5 a voltage source switch means consisting of first and second voltage source switches to connect RF components of the paging receiver and a voltage source in response to said first or second voltage source control signal;

10 an oscillator means for generating a given frequency signal in response to said oscillation control signal;

an RF receiver connected to said second voltage source switch for converting an RF modulated signal into an intermediate frequency signal;

15 a demodulation means connected to said first voltage source switch for demodulating the output signal of said oscillator means produced during said first period so as to produce a demodulated signal for said bias having a reference voltage, and then producing a demodulated signal according to the logical state of the modulated signal produced by said RF receiver during said second period; and

20 a waveform reshaping means connected to said first voltage source switch for stabilizing said bias by receiving the demodulated signal from said demodulation means during said first period and for identifying the logical state of the demodulated signal produced during said second period in
25 reference to said bias.

16. A circuit according to Claim 15, wherein said oscillator means comprises an oscillator for generating the center frequency of said intermediate



16. A circuit according to Claim 15, wherein said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal, and an oscillator switch for connecting said oscillator and demodulation means in response to said oscillation control signal.

17. A circuit according to Claim 16, wherein said demodulation means demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

18. A circuit according to Claim 17, wherein said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the logical state of a demodulated signal of the first or third voltage received during said second period.

19. A circuit according to Claim 15, wherein said oscillator means comprises an oscillator for generating the center frequency of said intermediate frequency signal during said first period, and an oscillator switch for connecting said oscillator and demodulation means in response to said oscillation control signal.

20. A circuit according to Claim 19, wherein said demodulation means demodulates an intermediate frequency signal produced by said oscillator during said first period into a second voltage which is a reference voltage, and



the signal produced by said RF receiver during said second period into a first or third voltage according to its logical state.

- 5 21. A circuit according to Claim 20, wherein said waveform reshaping means comprises a differential amplifier with a message signal input and a reference signal input, arranged to stabilize the bias of said reference signal input by the second voltage received during said first period, and then to produce digital data based on the logical state of a demodulated signal of the first or third voltage received during said second period.
- 10 22. A bias stabilizing circuit substantially as hereinbefore described with reference to Figure 8 or 14 of the accompanying drawings.
- 15 23. A circuit according to Claim 22 and substantially as hereinbefore described with reference to Figure 10 or 12 of the accompanying drawings.
24. A paging receiver incorporating a circuit according to any of the preceding claims.

